Webinar and Demo: The GTSOC for Black-Box Control Integration with the RTDS Simulator

Wednesday, November 23, 2022

Questions and Answers

Q1: Will the webinar recording and slides be made available?

Yes. The webinar recording and slides are available to all registrants. A link has been included with this document in the post-webinar email. If you would like to refer a colleague to this webinar, it can be accessed later On Demand, after having been aired.

Q2: Does the .a application require a specific solution time step on the real-time simulator or are there ways to synchronize/downsample I/O between them?

There is no specific simulation time step required. The GTSOC and RTDS can run in either asynchronous mode or synchronous mode. You would specify the controller sampling time step. When it's time to sample, it will read the latest available data. What is important is if the GTSOC can complete all the calculations within the sampling time.

Q3: Does the firmware upgrade tool allow you to download firmware from different vendors to each ARM core, i.e. if you want to use one arm core to test vendor A's controls and another ARM core to simultaneously test Vendor B's controls?

Each GTSOC will run one firmware at a time. You can have different vendors on the same firmware when developing the wrapper (one wrapper would be developed for each vendor's controls, which are then all included in one firmware). However that might need a third party to be involved to coordinate and integrate the wrappers. Note when creating the wrapper, vendor IP is protected as their source code is included as a .a file.

Q4: Why should I go with GTSOC - compared to asking an inverter manufacturer for a control board with documentation on how to connect it to a real-time simulator?

Such boards normally are not available from OEMS. The amount of support is simply too high and if OEMs would have to put a price tag on such offerings it would be not reasonable. Maybe it is possible for smaller controllers, but a Central inverter system has a lot of interfaces, plus to suit the hardware-in the-loop environment, there are custom changes that would need to be made, e.g. change voltage dividers for measurements and other things. It

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is much more straightforward to use the GTSOC approach when it comes to complex inverter controls.

Q5: Does the user have the ability to change the control parameters or settings?

Yes. This was shown in the demo today and we consider it an important capability. When changing control parameters, the code does not have to be recompiled / a new firmware does not need to be generated.

Q6: RSCAD has CBuilder which allows new models to be created for the RTDS Simulator using C code. So why is the GTSOC needed – why can't the vendors use CBuilder instead?

The main advantage to use the GTSOC instead of the CBuilder is that the GTSOC allows the vendor to use their original code base without modification. CBuilder requires a certain code structure which would likely require significant modifications to the original code in the case of something complex like an inverter controller.
Another advantage of GTSOC is its asynchronous mode. This will not require NovaCor and the vendor's controller to run at the same time step. GTSOC is used to mimic vendor's real controller.

Q7: The Xilinx VITIS software requires considerable memory and processor capacity – is this true? Are there any alternatives to do it via ad-hoc or Windows applications in future releases of GTSOC Interface?

Yes, the Xilinx VITIS software is required to generate the GTSOC firmware, and it does have high memory/processing requirements. We are looking for alternative possibilities in the future development of the GTSOC interface tool.

Q8: Is it possible to have multiple GTSOC units running in parallel for a single simulation case?

Yes, it is possible to have multiple GTSOCs running in parallel in the same simulation case. Also, a GTSOC can simulate several instances of a controller. The limit is a maximum of 5 GTSOCs in one chassis.

Q9: It appears that each GTSOC has four ARM cores and four fibre optic cable connections are needed between GTSOC and NovaCor. Why there are additional fibre ports available on the GTSOC front panel? Is that because each GTSOC core can simulate multiple inverter controller instances?

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The daughter card used in the GTSOC comes with 8 ports. GTSOC only uses 4 of them. The other 4 ports are not used but potentially could be used in the future.

Currently, each ARM core requires one fibre optic connection (i.e. one port). Each fibre connection handles the data for up to 5 .a instances running on that ARM core.

Q10: It seems that the GTSOC can be used to represent generic controllers. Could you please confirm if we can compile .a code of a complex control from Simulink to run in GTSOC? For example, a controller with neuro-fuzzy inference system and state flow in Simulink.

Yes, you are correct. You can develop a model in Simulink, use Matlab and Simulink embedded coder to generate the C code, and use the interface tool the generate the .a file and the firmware.

Q11: Is there a way to check if the control complexity exceeds the capability of an ARM core on the GTSOC? Or it has to be a trial and error approach?

The execution time of the control code running on a core can be measured. From this information, it can be determined if it can meet the sampling time requirements.

Q12: Will the vendor models be available to all RTDS users?

The expectation is the distribution of the vendor model will be done by the OEM. It would be up to the OEM how they make the model available.

Q13: In the demonstration, is power control grid connected mode? What is the difference between stop and inverter standby?

In the Sunny Central Storage inverter the control mode “power control” refers to a grid following mode that follows active and reactive power references. In “Stop” the power conversion unit is fully stopped and disconnected from DC sources and the AC grid. In “Standby” just the firing pulses are blocked but the inverter remains connected to AC and DC.

Q14: Have you done comparisons between the GTSOC and PSCAD DLL model or even an actual hardware installation?

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We are currently performing comparison tests between GTSOC and PSCAD DLL for the SMA model. We also plan on comparing results with the SMA GTSOC setup with a HIL setup with the SMA controller hardware

Q15: With an increasing complexity of DER control algorithms, can the 4 ARM cores (20 DOTA components) be utilized collectively to execute a complex control if needed?
If the controller code is separated into different .a files, the control code could be distributed onto several ARM cores each running a different application representing a different part of the controller. Each ARM core can also sample at different rates. In the future, we can also look at a single application running on all 4 ARM cores.

Q16: The average model of the inverter is demonstrated here. Is there a development plan to support the firing algorithm on GTSOC?

To generate firing from the GTSOC output, it would require the GTSOC to update its outputs at a sufficient rate (in the range of several usec). It is unlikely the full controller will be able to complete the execution of the code to update the output this frequently. This is why it is recommended for the .a code to only generate the modulation waveforms and for the firing pulses to be generated within NovaCor if a switching model is required. Generating the firing pulses on NovaCor can also utilize the improved firing algorithm for the UCM model for more accurate results.

If you have any further questions, please contact marketing@rtds.com.

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