2023 North American
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Inverter-Based Resources Model Development and Validation Using PSCAD-RTDS Co-Simulation

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Presentation Outline

- Introduction
- RTDS IBR Model Development
- RTDS IBR Model Validation
- PSCAD-RTDS Co-Simulation Model Validation Results
- Conclusion

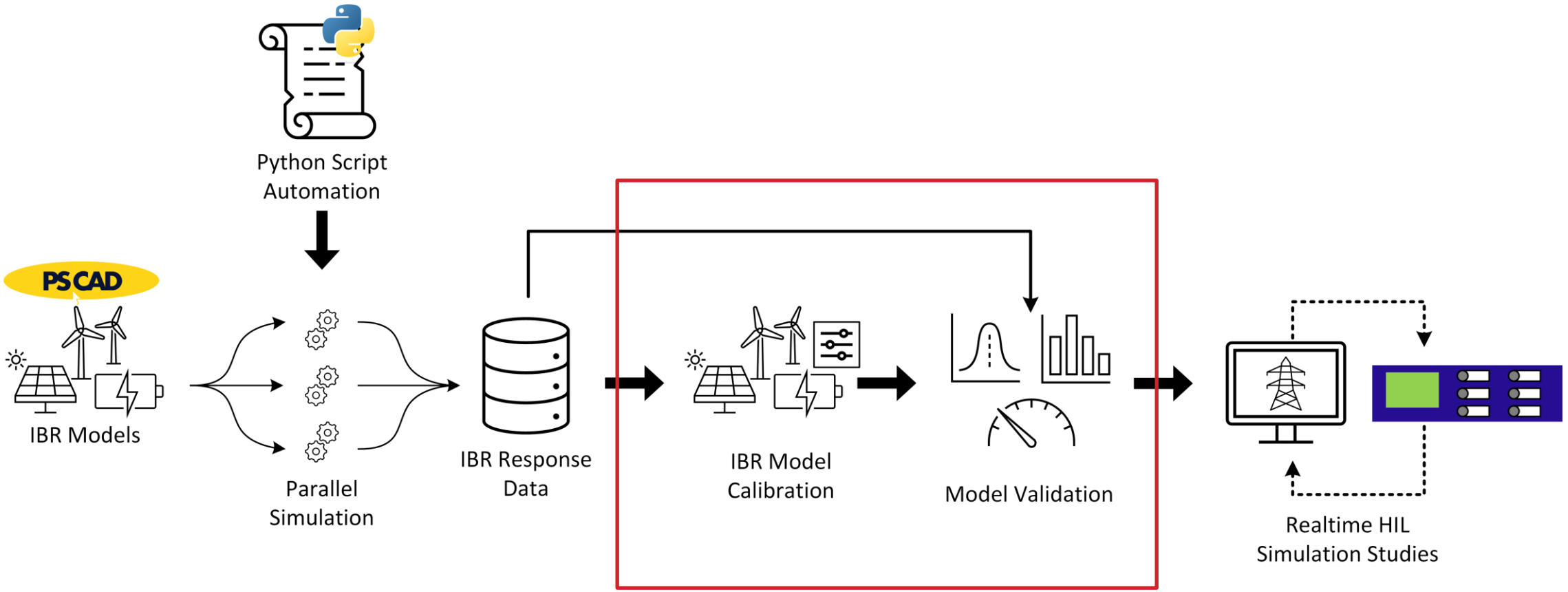
Introduction

Real-time IBR HIL Testing – Modeling Challenge

- Data Source
  - PSCAD model with compiled IBR model in the format of DLL (Dynamic link library)
  - Typically, black-box, based on actual inverter controls or real-code

- Challenges
  - Hidden inverter parameters
  - Hidden protection logics, e.g., collector protection and plant protection
  - Third party software may be required package to simulate plant PSCAD model

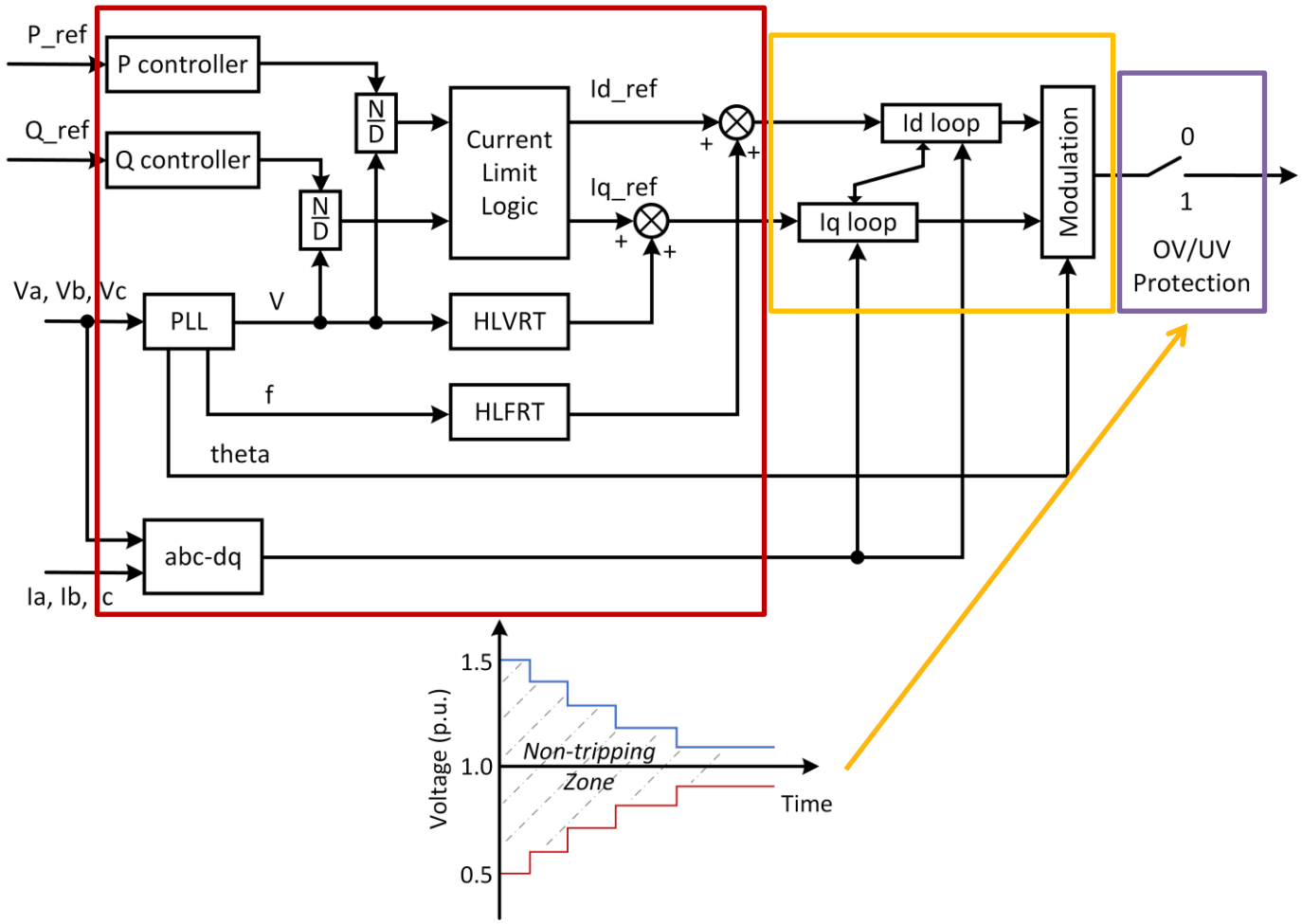
Overall Workflow



RTDS IBR Model Development

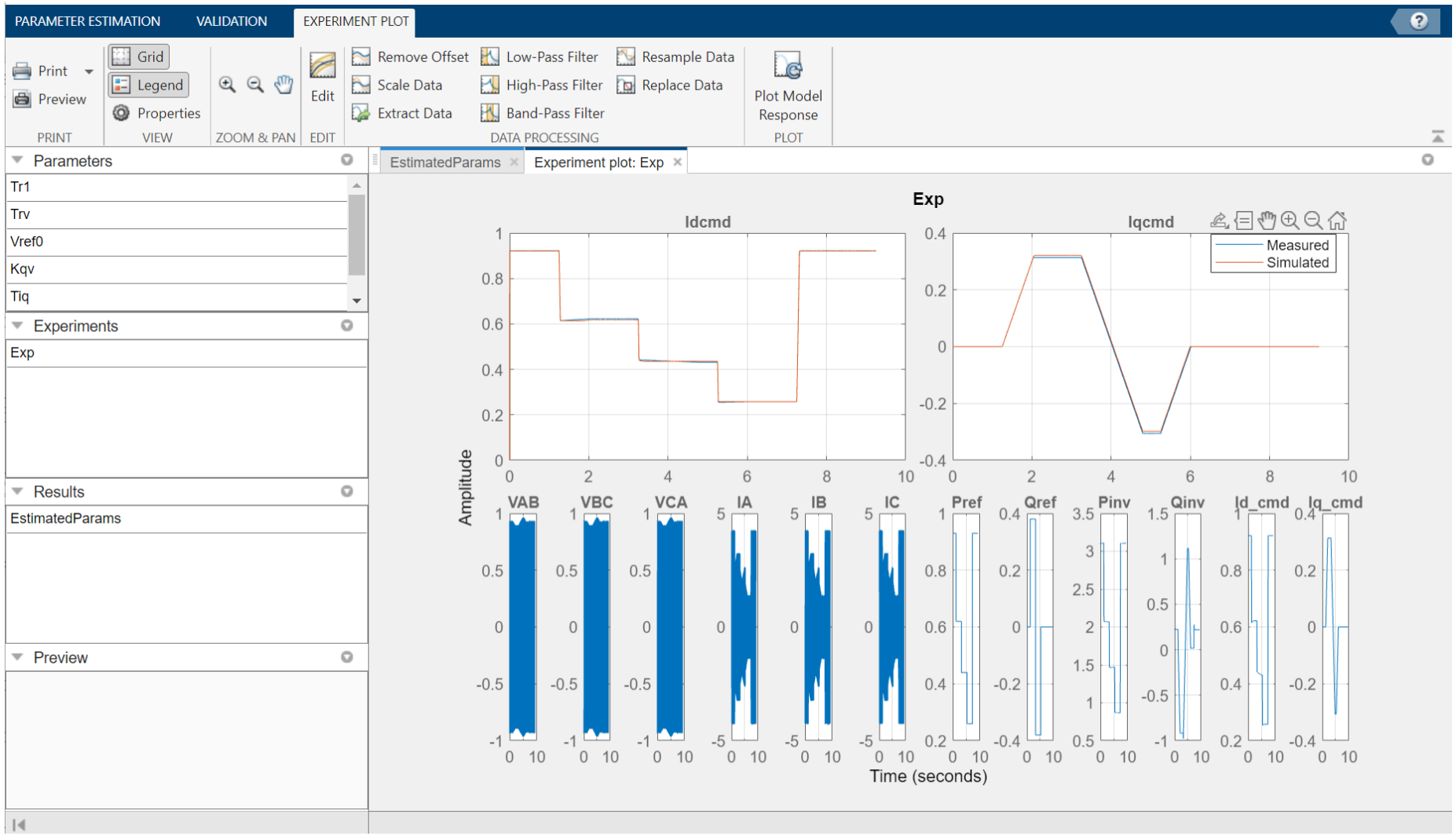
Systematic Model Tuning and Validation

- Quasi-steady-state response matching
  - Focus on filter time constants, PID gains, voltage-dependent current limits, ramp rates, etc.
- Fault transient response matching
  - Focus on HLVRT, fault, protection functions, etc. (red box)
  - Inner loop control and modulation (yellow box)
  - Tripping logic. (purple box)
- System interactions matching
  - Connect to developed IEEE-14 bus systems and focus on internal and external fault responses.



Automated Model Parameter Estimation

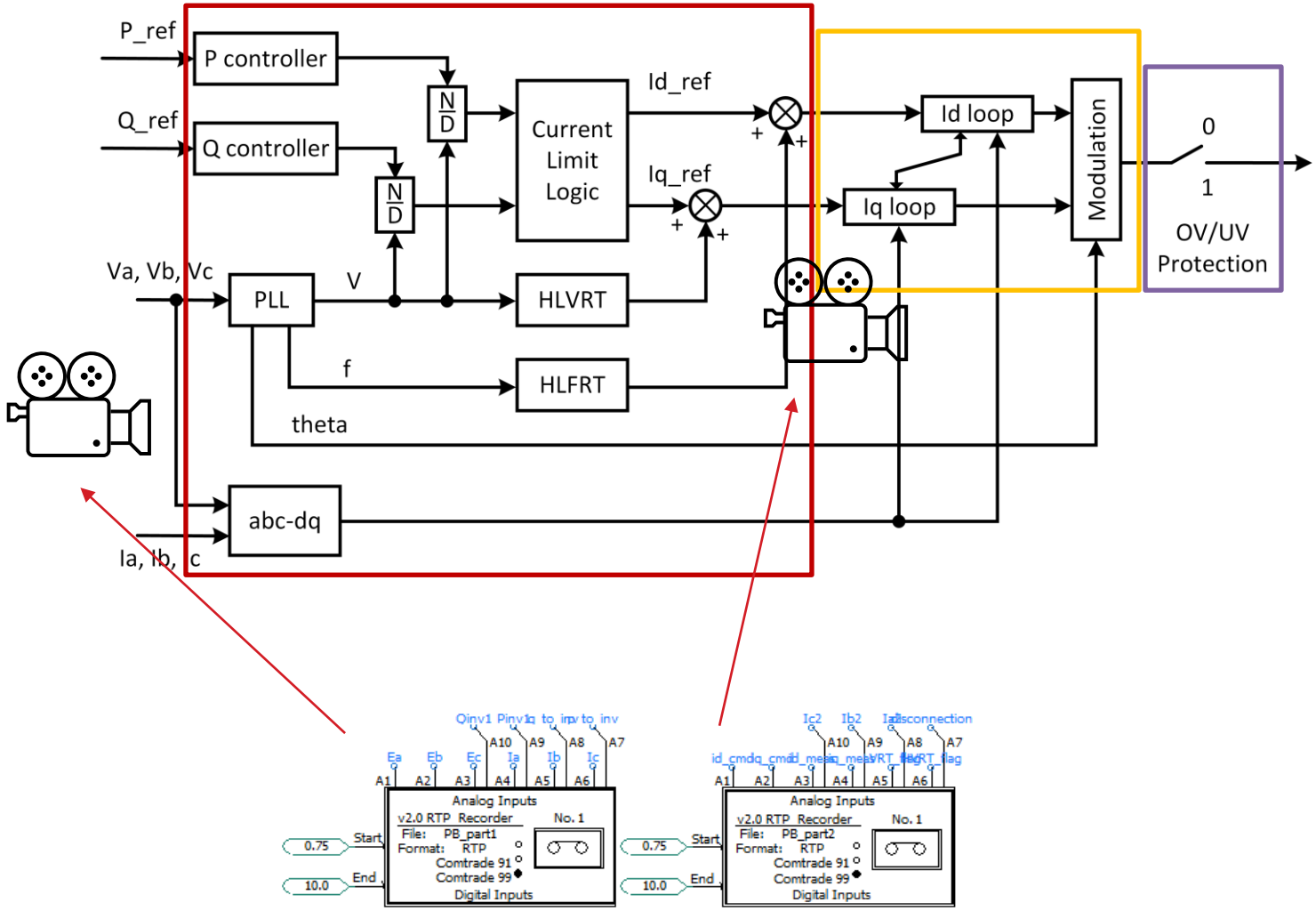
- MATLAB parameter estimation tool



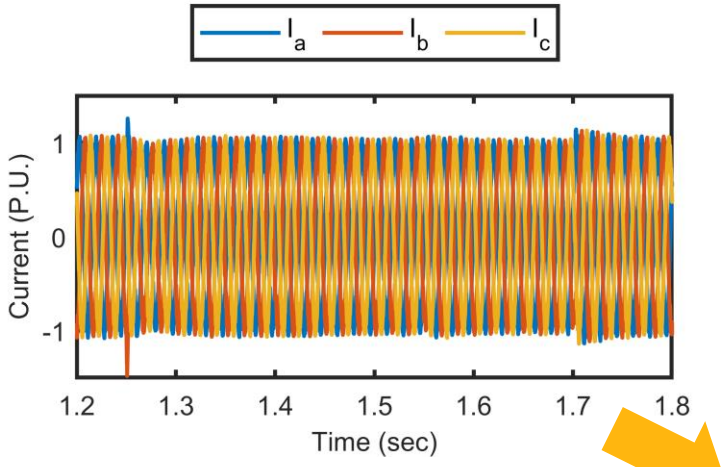
IBR Outer Loop Response Matching

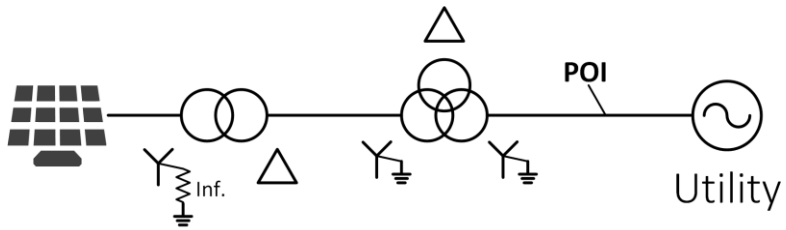
IBR Vendor Models Matching - Recap

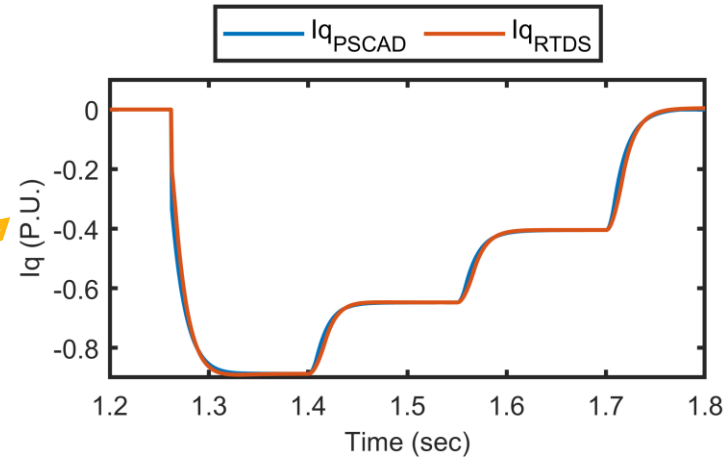
- 2-step matching process
  - Outer control loop (red)
    - Inputs: Pref, Qref, Vabc
    - Outputs: Id_ref, Iq_ref
  - Inner control loop (yellow)
    - Inputs: Id_ref, Iq_ref, Iabc, Theta
    - Outputs: IGBT gate drive signals



Low Voltage Ride Through Test







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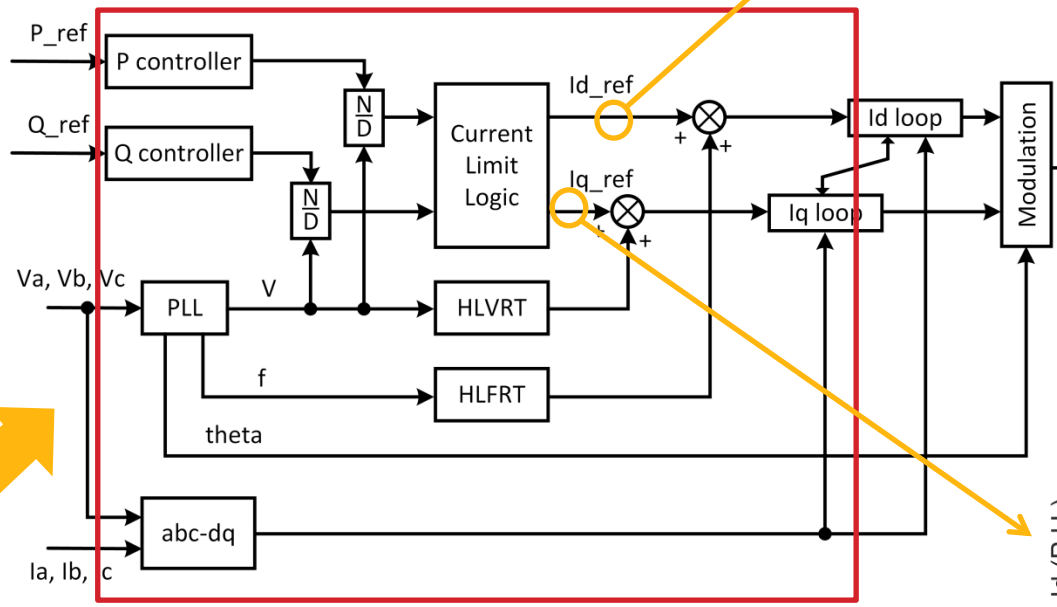
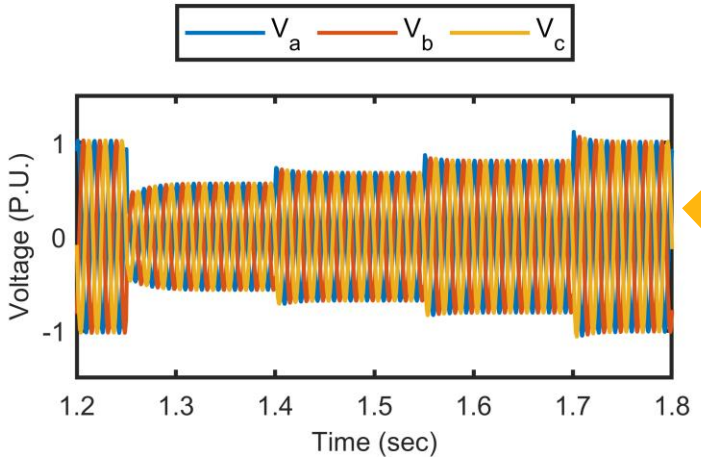
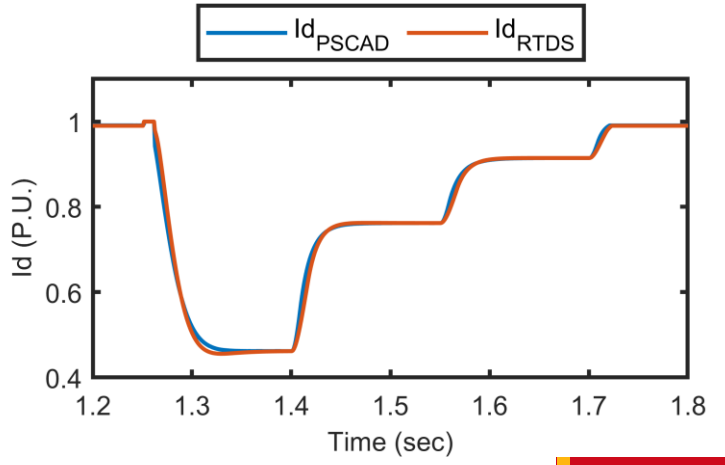
$Q_{\text{ref}} = 0$

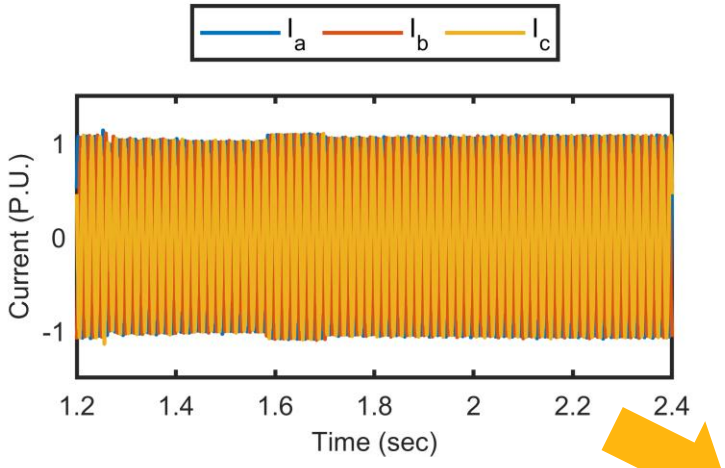


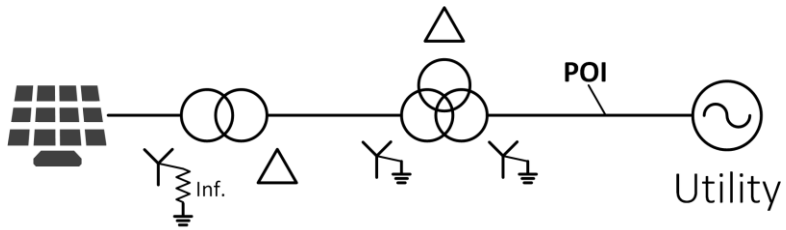


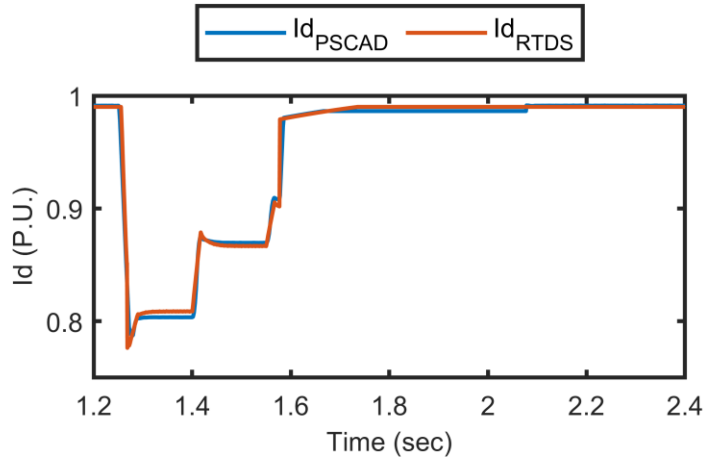
$\text{MAE}_{I_d} = 0.0051$ p. u.
$\text{MAE}_{I_q} = 0.0071$ p. u.



High Voltage Ride Through Test







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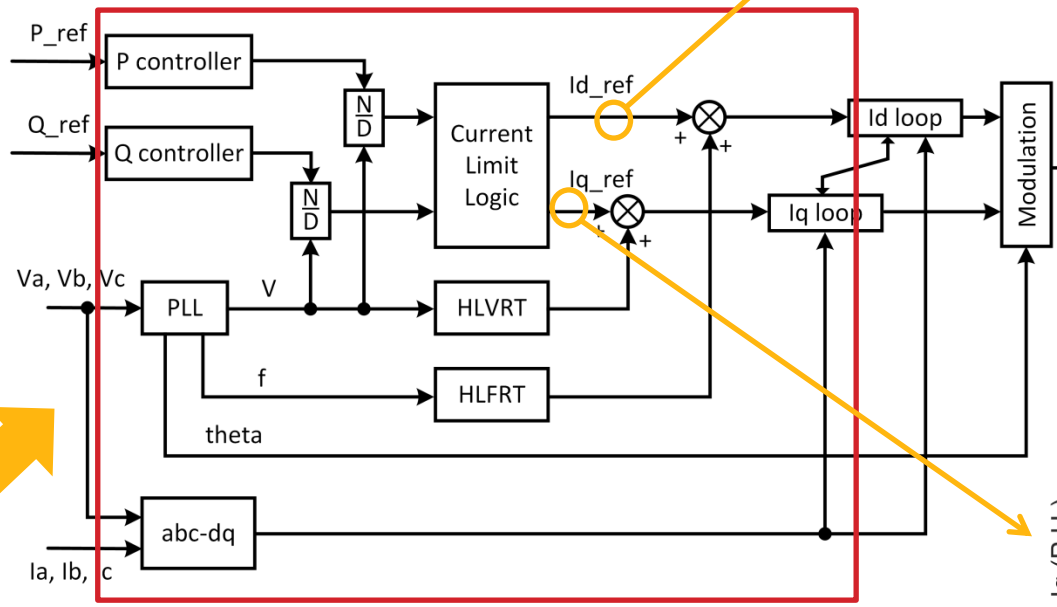

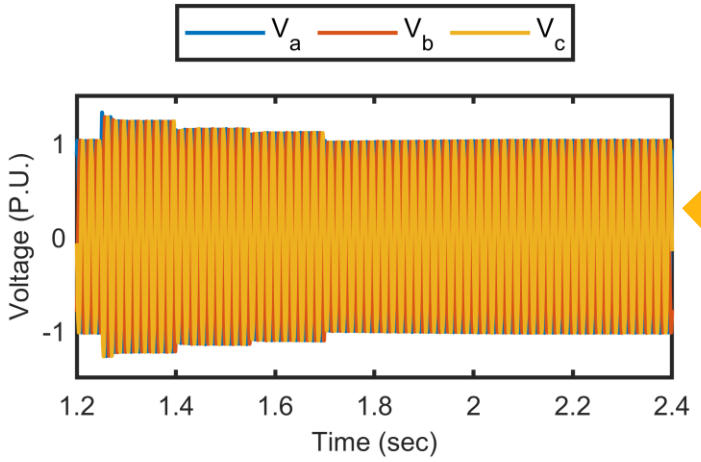

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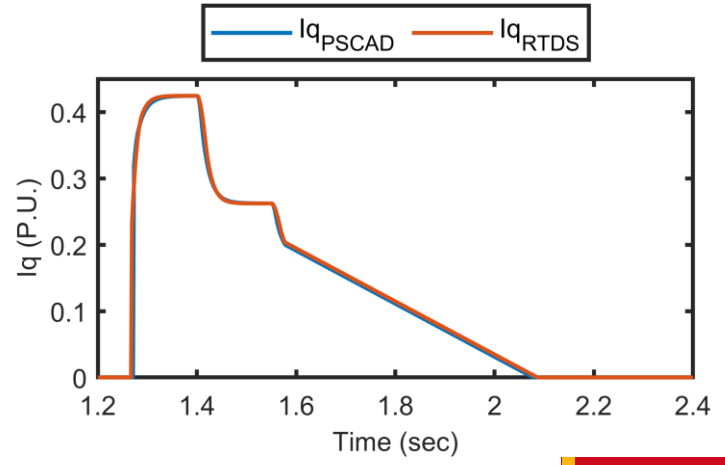
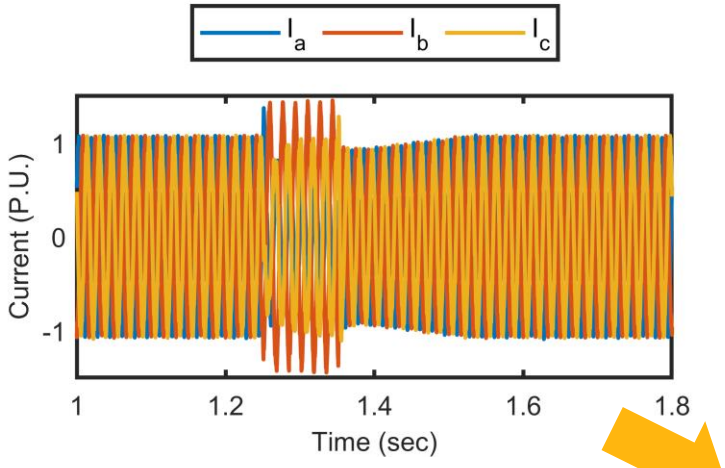
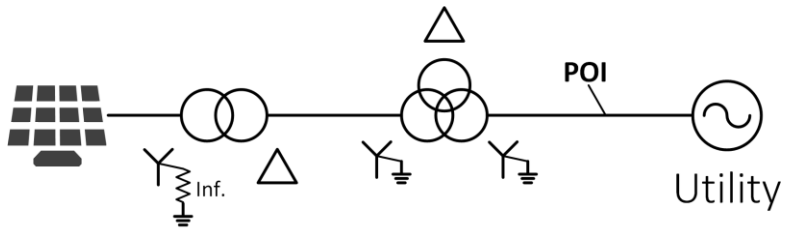
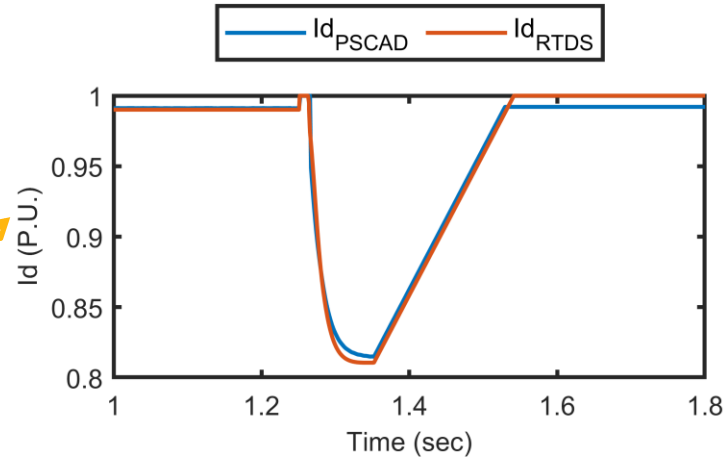


AB Fault at POI – 100 ms







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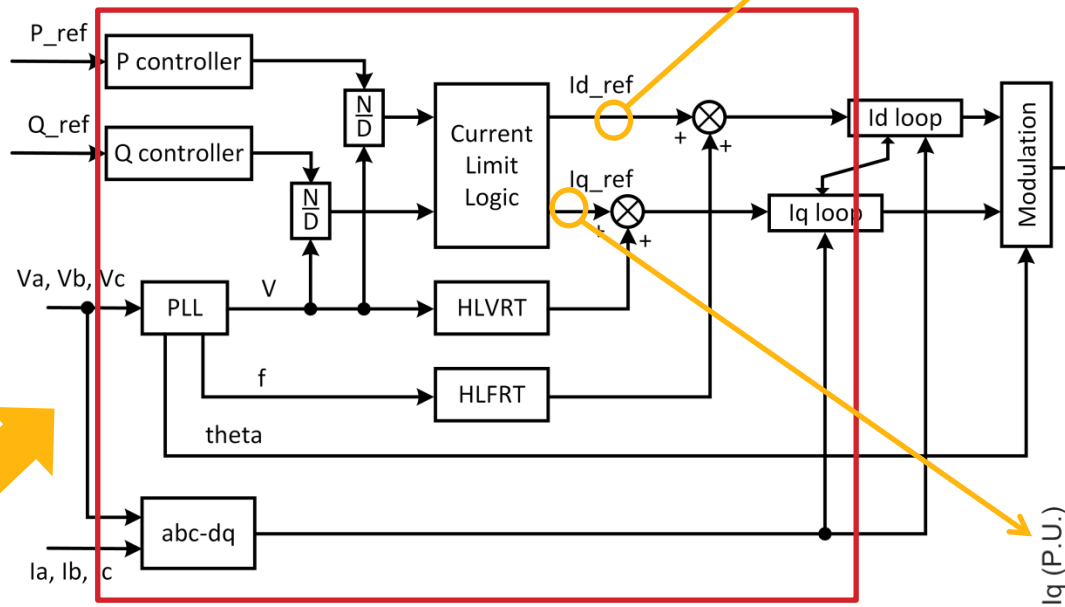
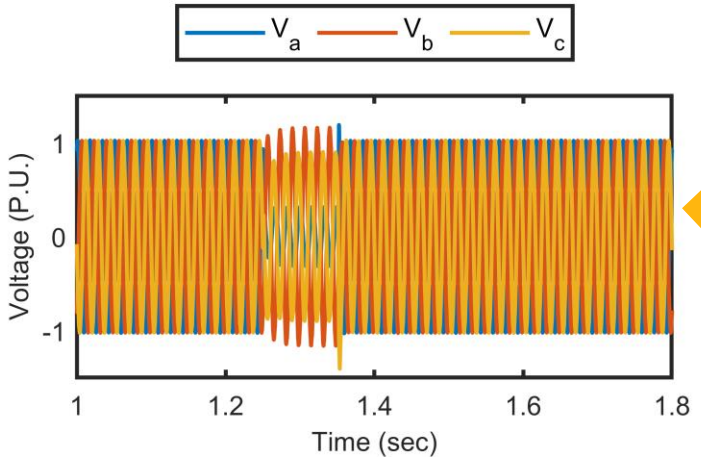
$Q_{\text{ref}} = 0$





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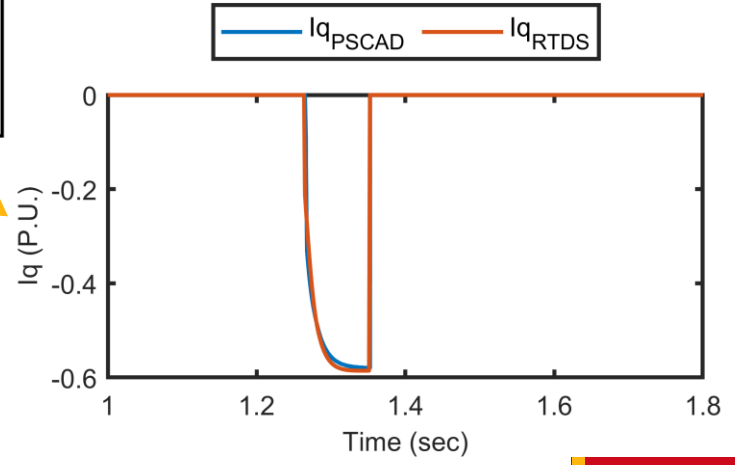
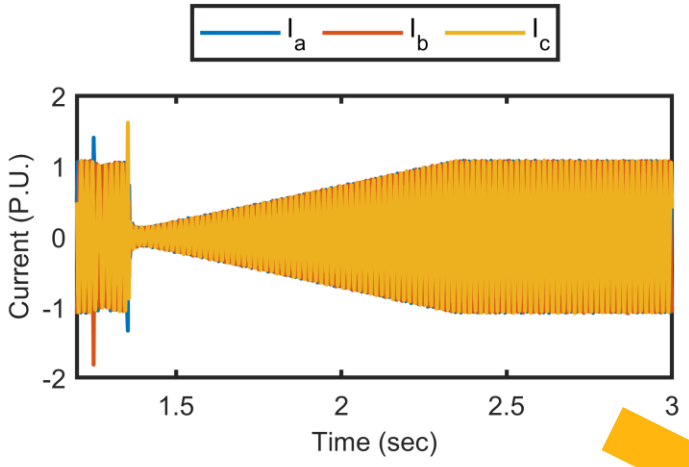
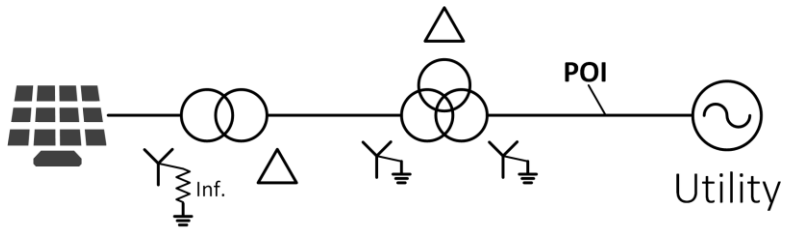
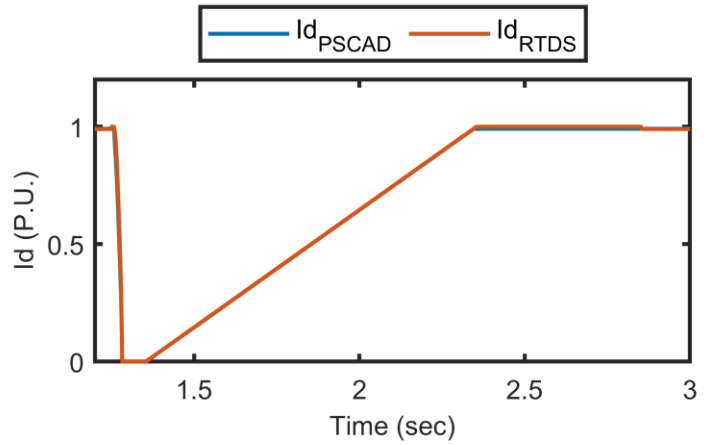
$\text{MAE}_{I_q} = 0.0021$ p. u.



ABC Fault at POI – 100 ms







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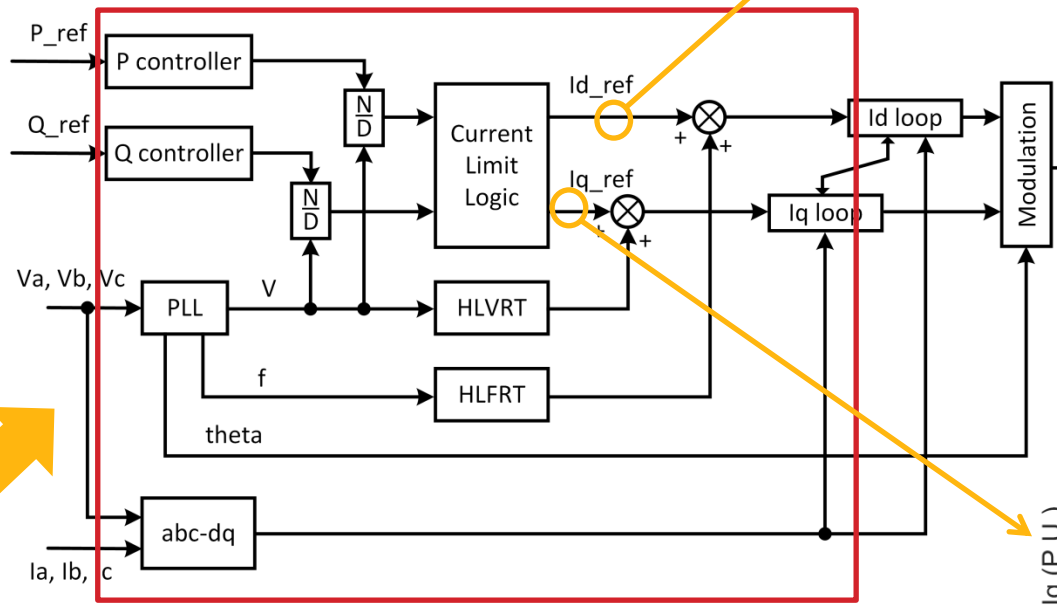
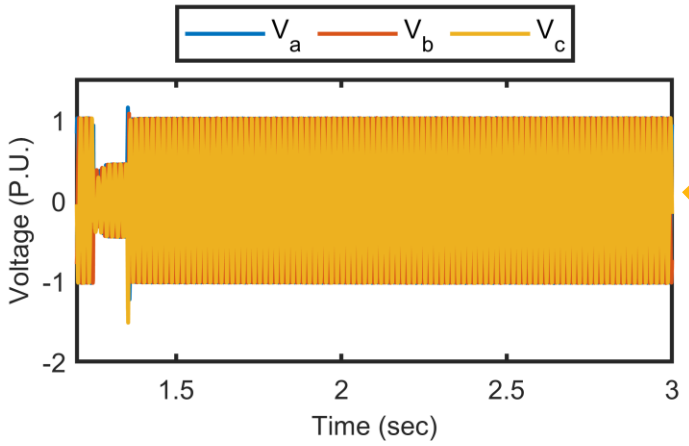
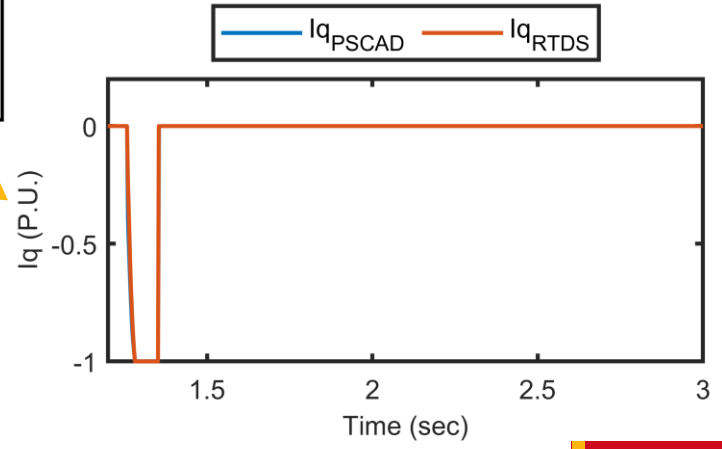
$Q_{\text{ref}} = 0$

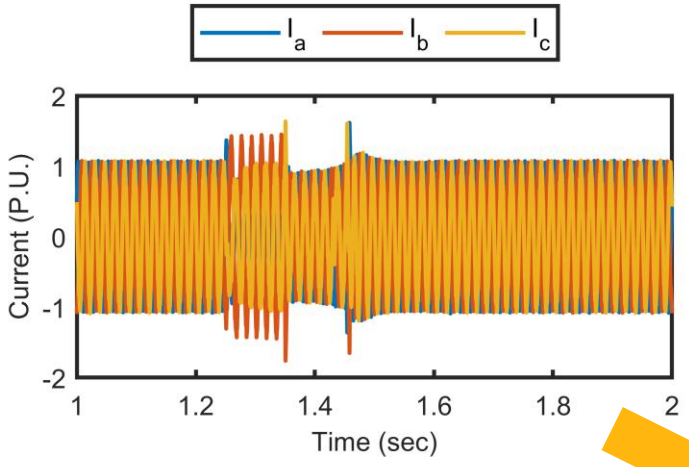


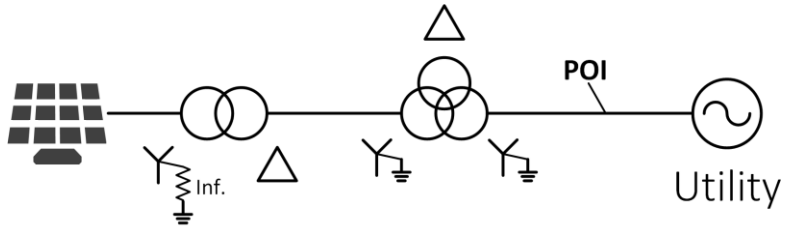


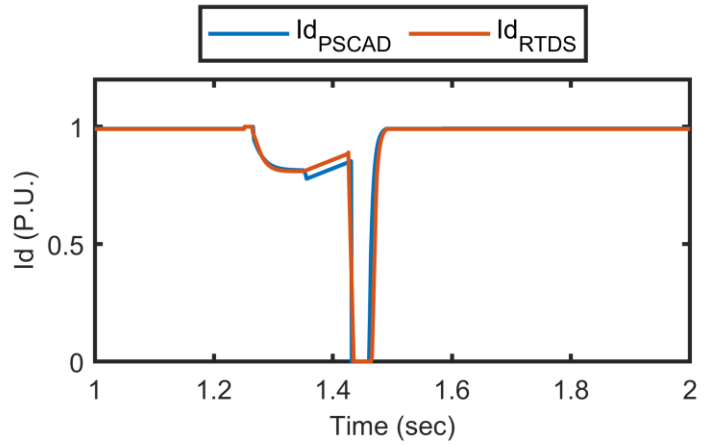
$\text{MAE}_{I_d} = 0.0036$ p. u.
$\text{MAE}_{I_q} = 0.0012$ p. u.



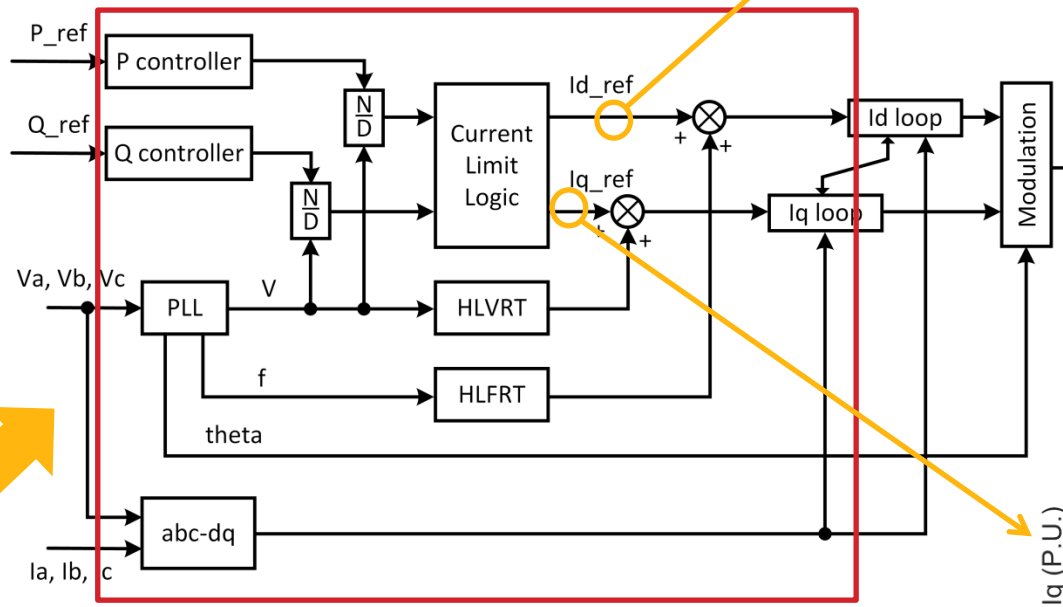
Evolving Fault AB-ABC Fault at POI – 200 ms

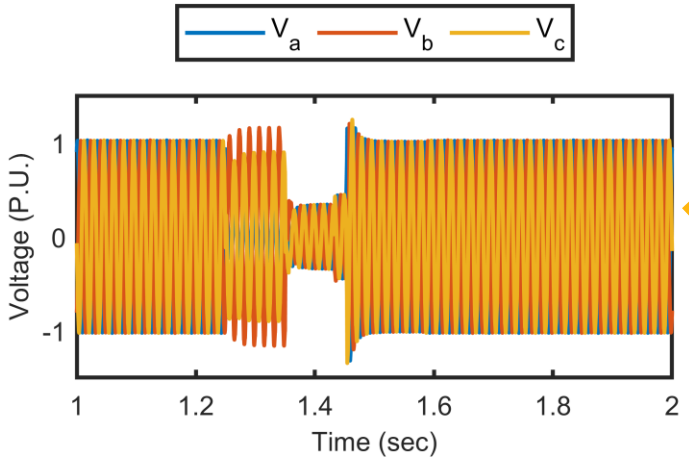




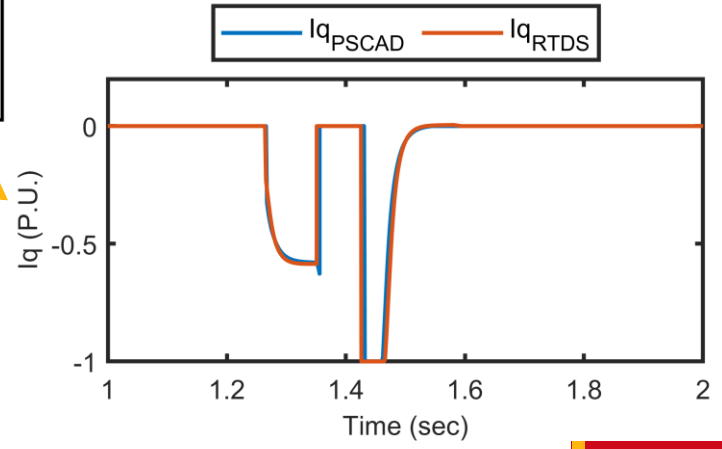


$$P_{\text{ref}} = 1$$
$$Q_{\text{ref}} = 0$$

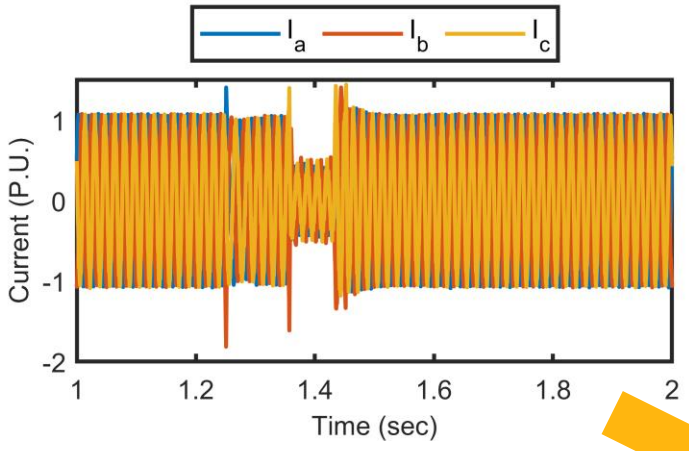


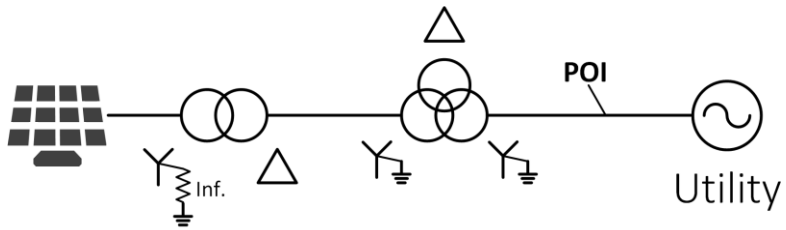


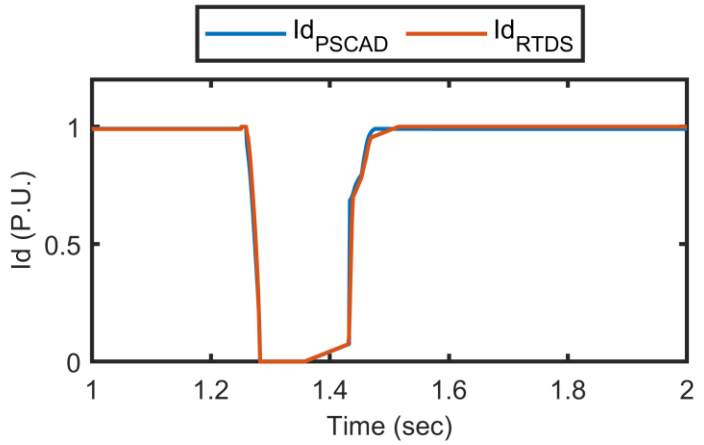
$$\text{MAE}_{I_d} = 0.0113 \text{ p. u.}$$
$$\text{MAE}_{I_q} = 0.0136 \text{ p. u.}$$



Evolving Fault ABC-BC Fault at POI – 200 ms







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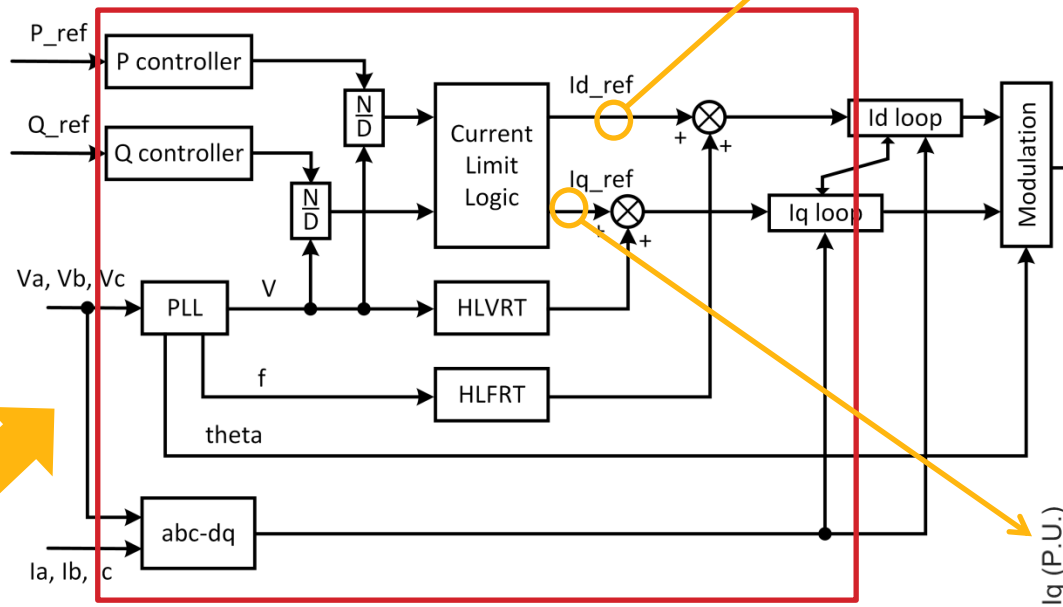
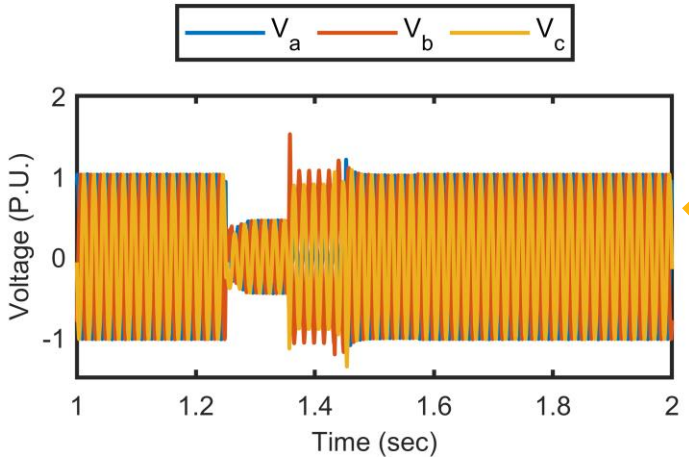
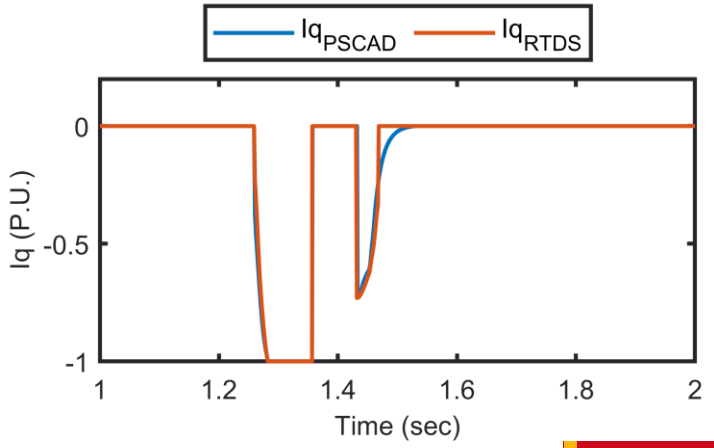
$Q_{\text{ref}} = 0$

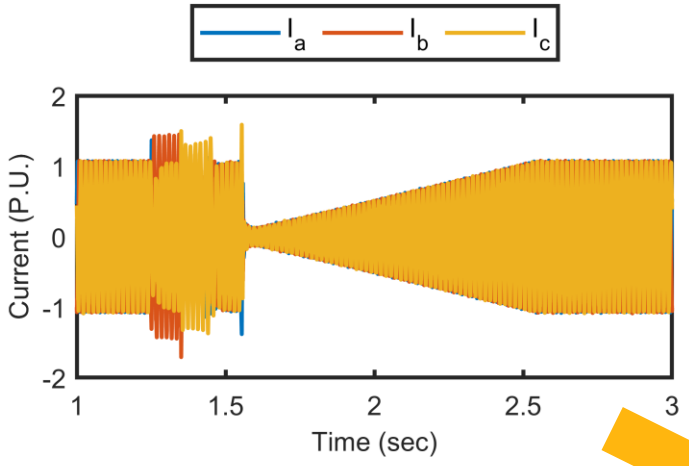


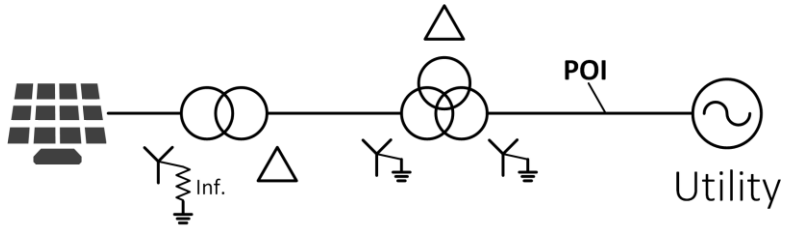


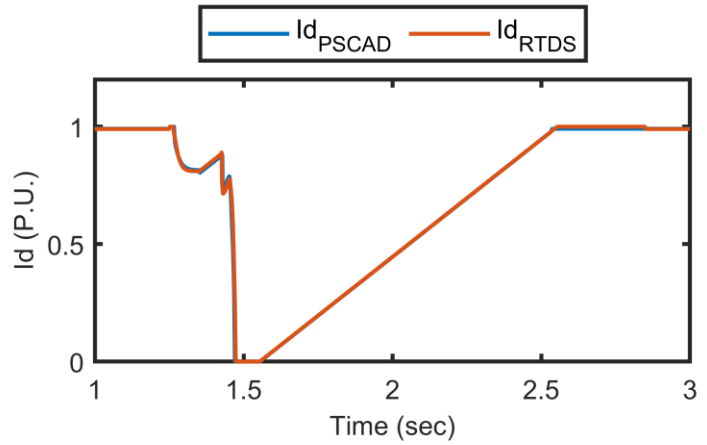
$\text{MAE}_{I_d} = 0.0091$ p. u.
$\text{MAE}_{I_q} = 0.0072$ p. u.



Evolving Fault AB-BC-ABC Fault at POI – 300 ms







$P_{\text{ref}} = 1$
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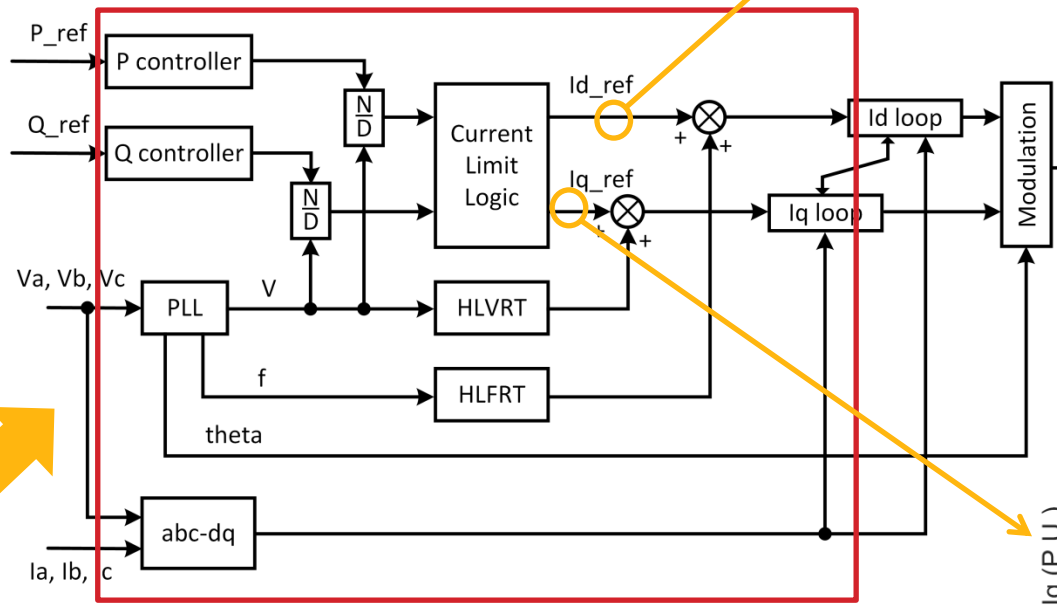
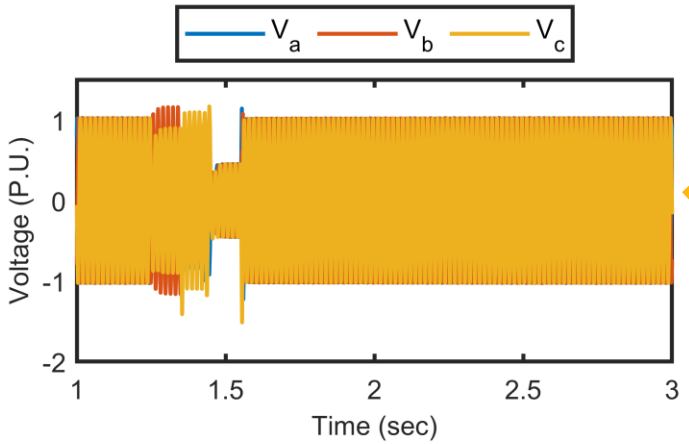
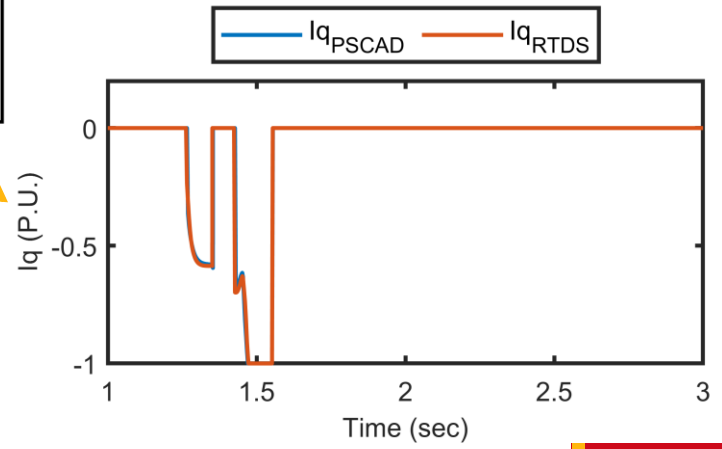
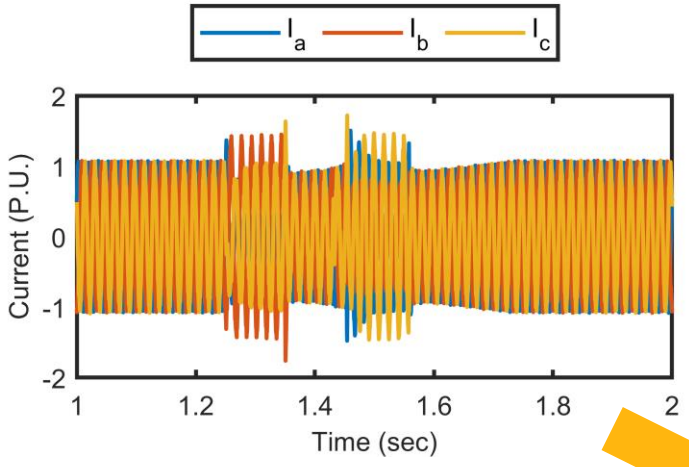


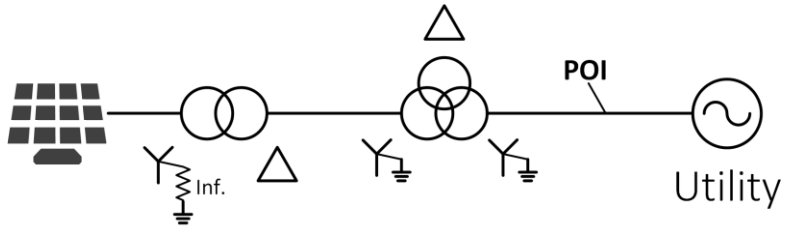
$\text{MAE}_{I_d} = 0.0036$ p. u.
$\text{MAE}_{I_q} = 0.0031$ p. u.

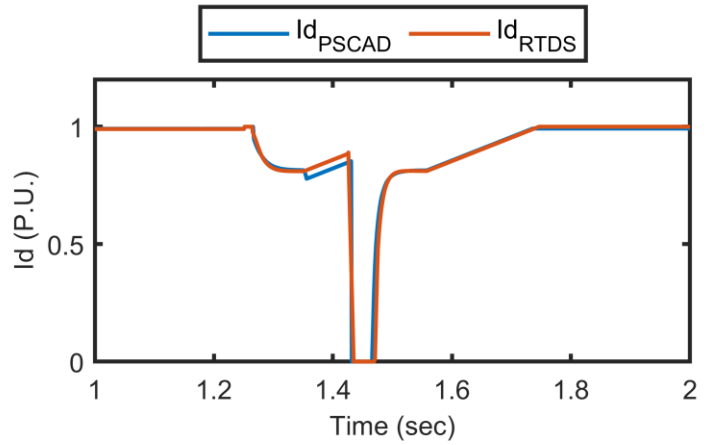




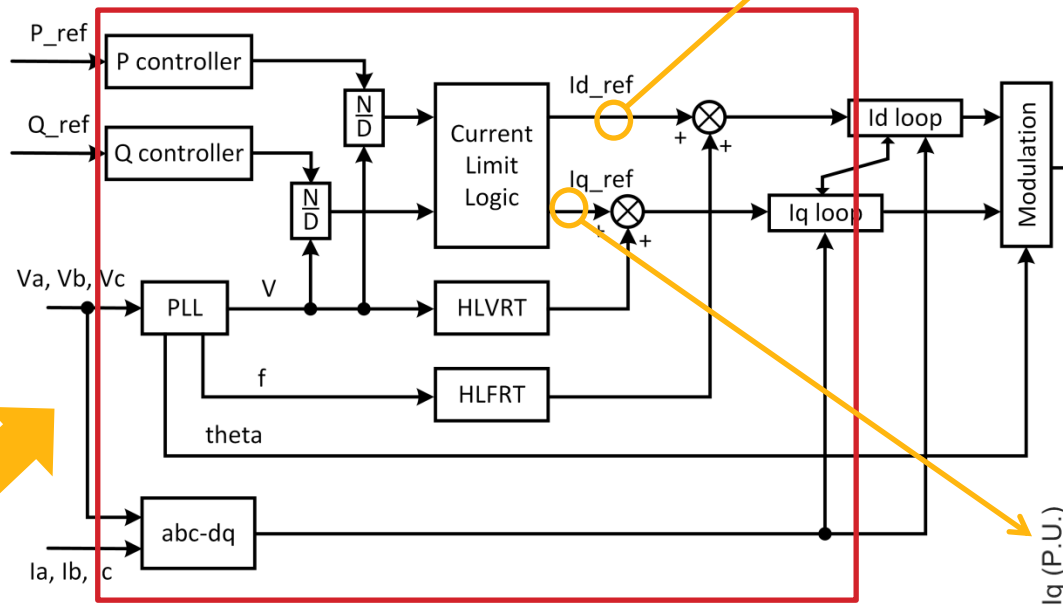
Evolving Fault AB-ABC-BC Fault at POI – 300 ms



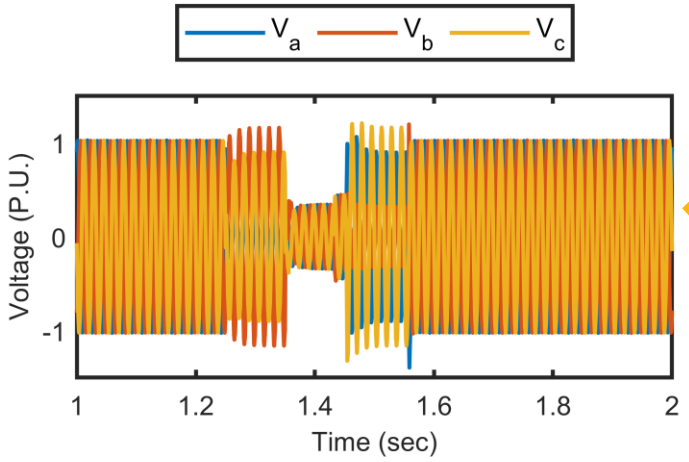


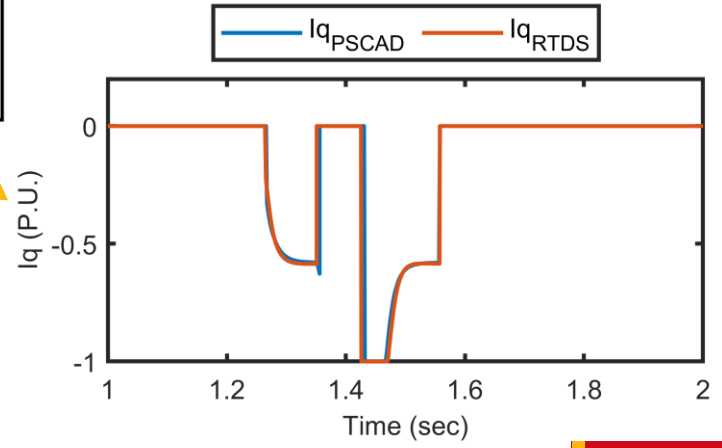


$P_{\text{ref}} = 1$
$Q_{\text{ref}} = 0$



$\text{MAE}_{I_d} = 0.0108$ p. u.
$\text{MAE}_{I_q} = 0.0111$ p. u.



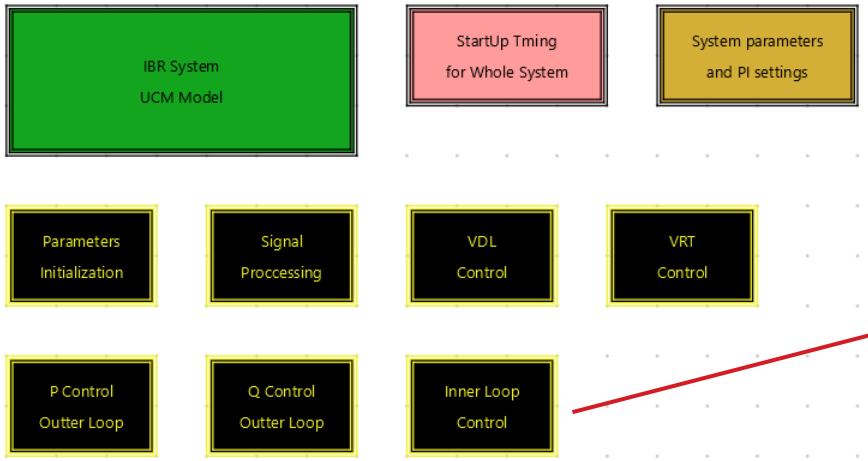


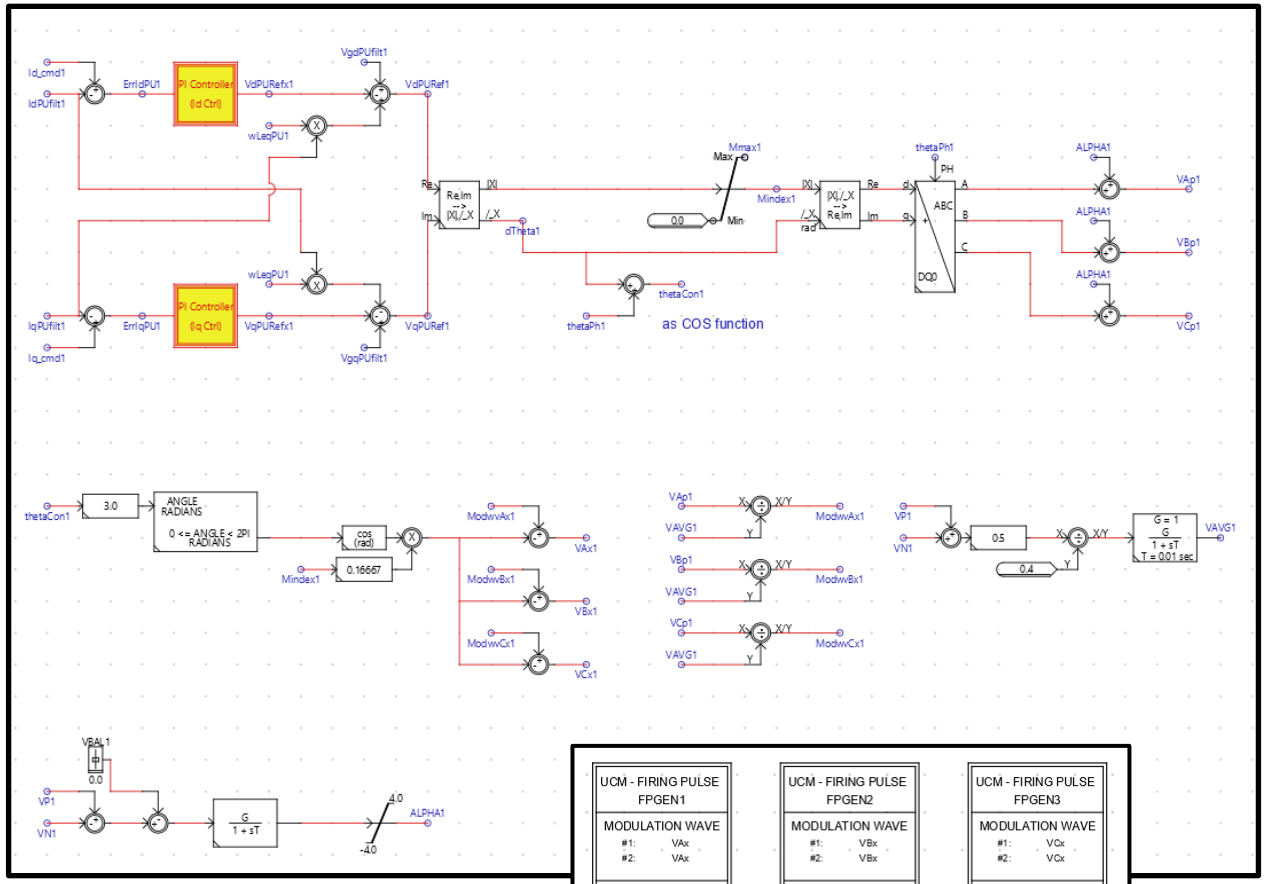
IBR Outer & Inner Loop Response Matching

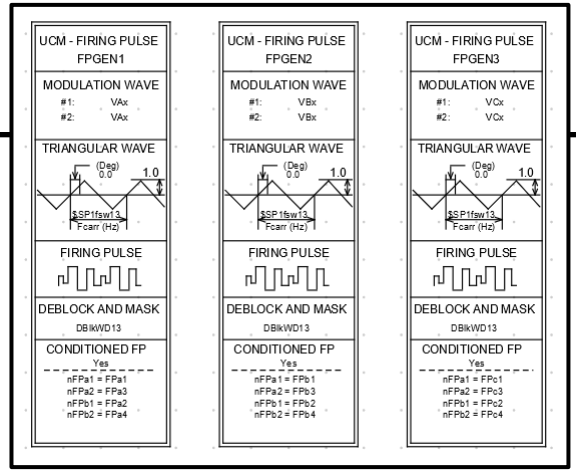
IBR Model Development: Inner Control Loop

- IBR Model
  - Modular format

- New control development
  - Developed an inner loop control
  - SPWM modulation

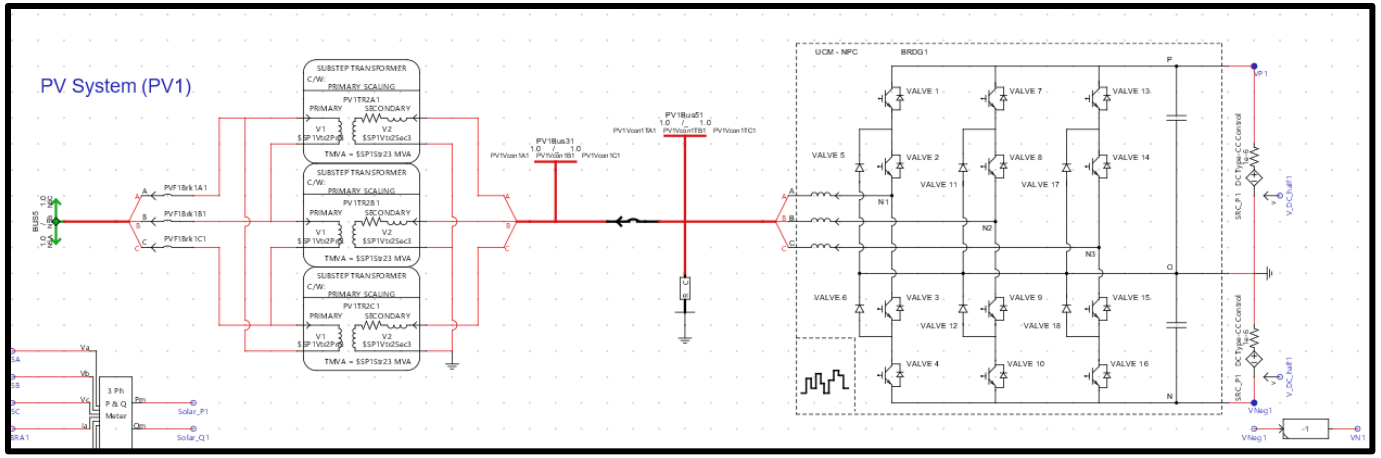


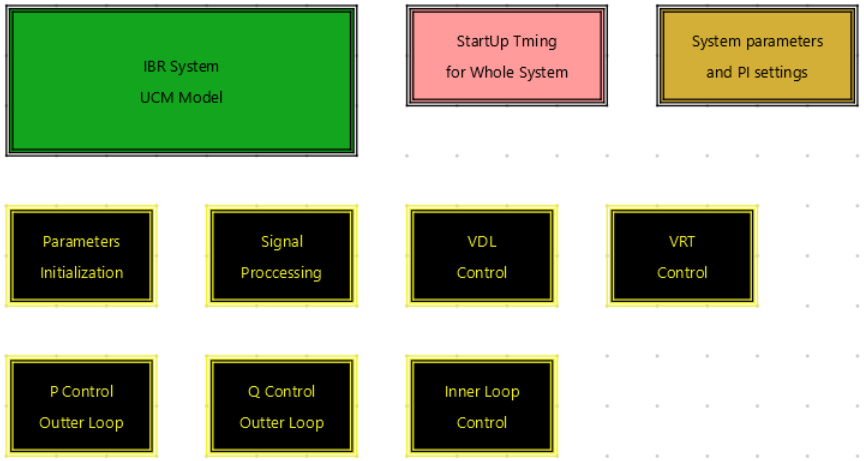


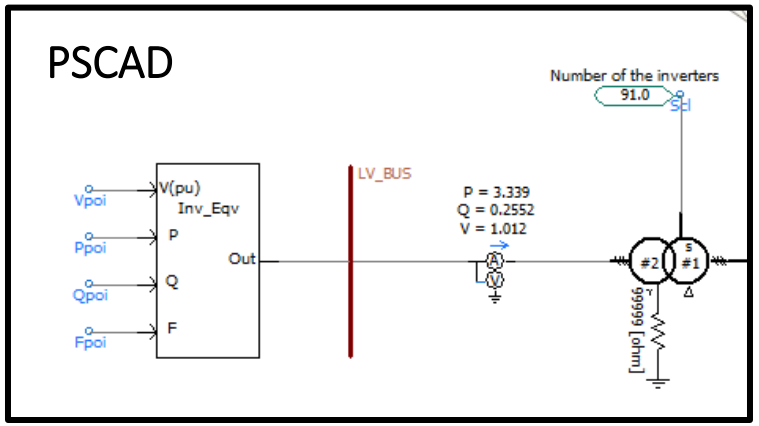


IBR Model Development: power electronics

- New development
  - Included power electronics switches
  - Inverter output filter
  - GSU transformer with scaling factor

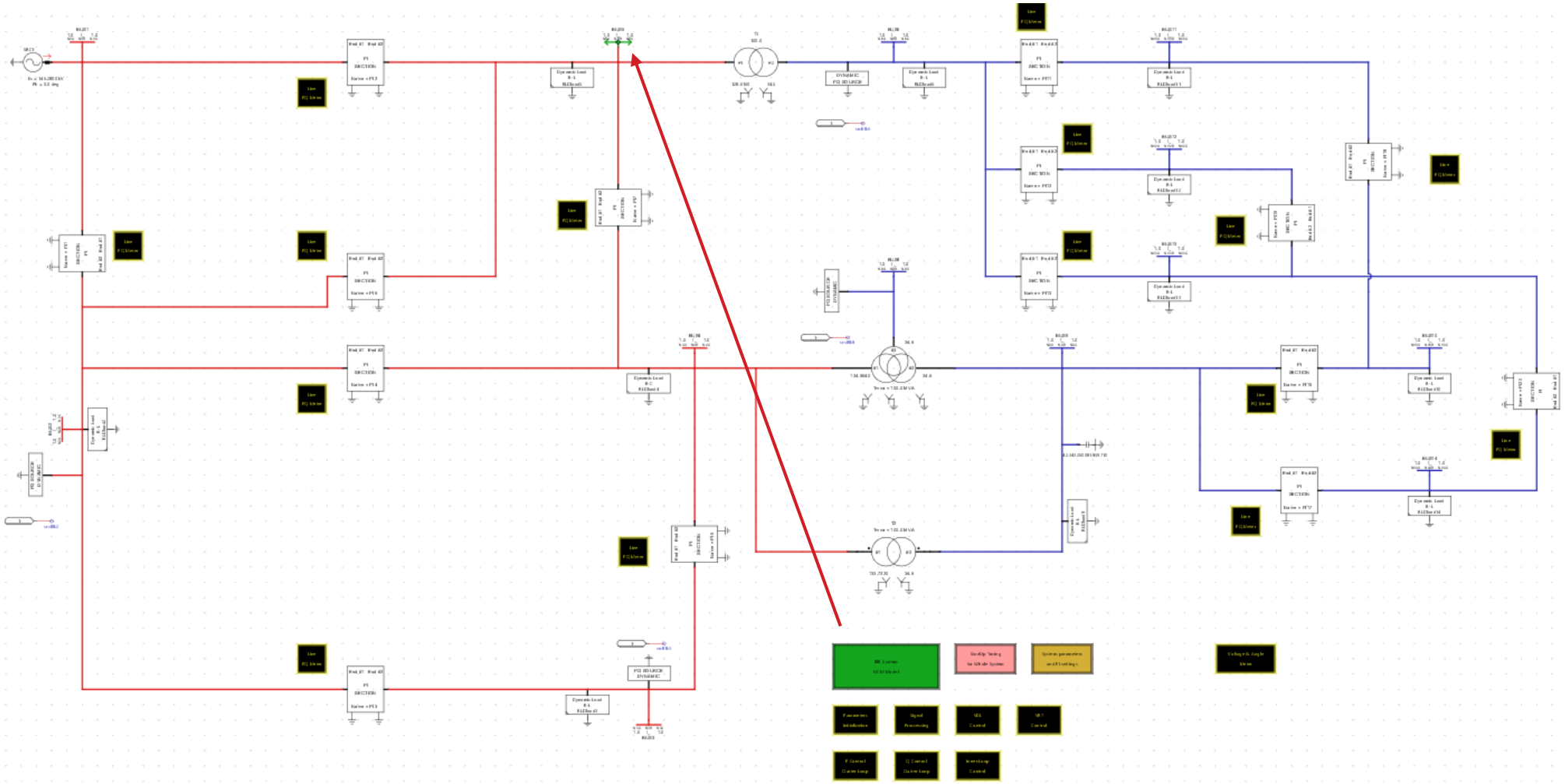






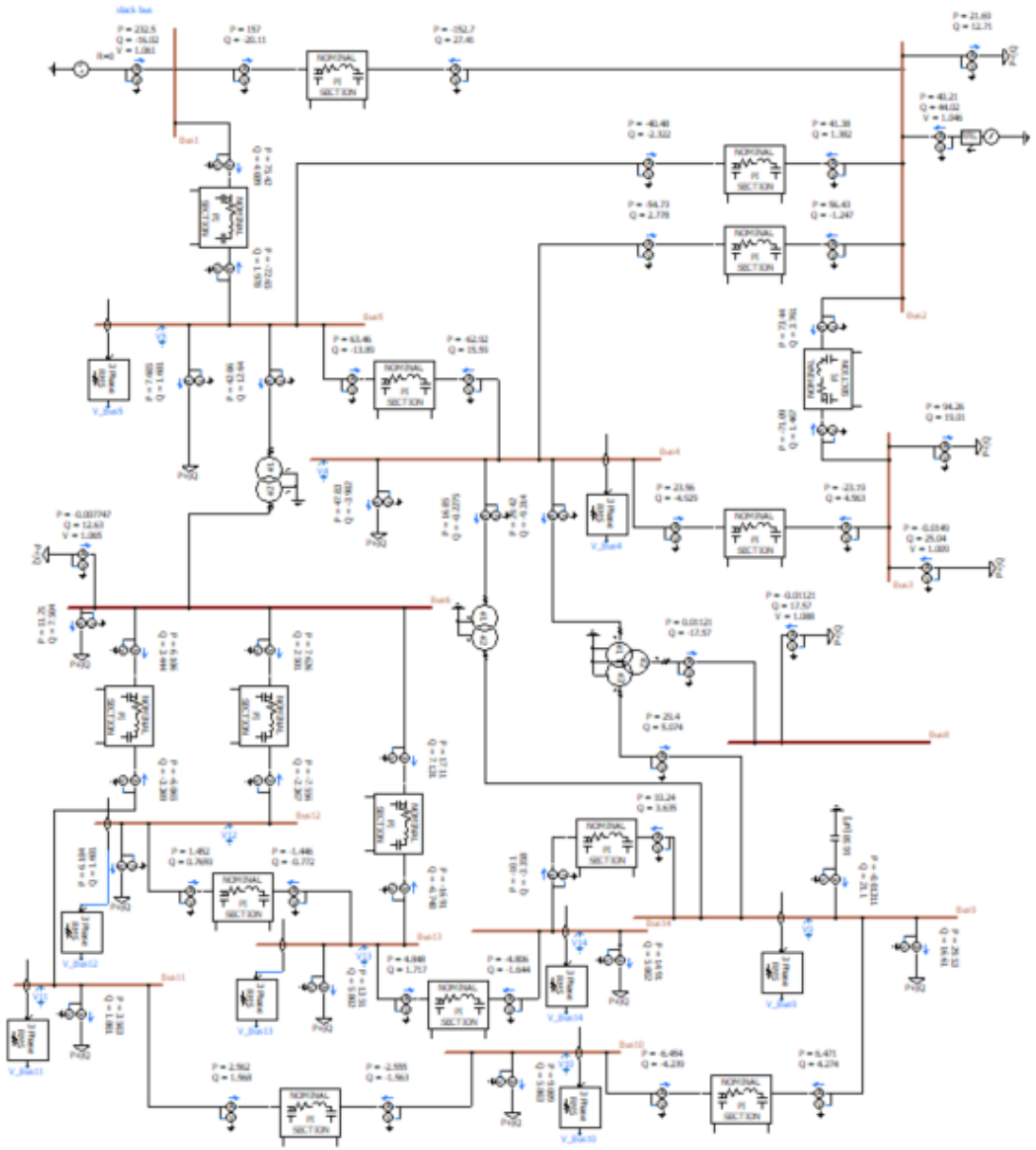
IBR Model Development: System integration

- New development
  - IEEE 14 bus integration – Bus 5



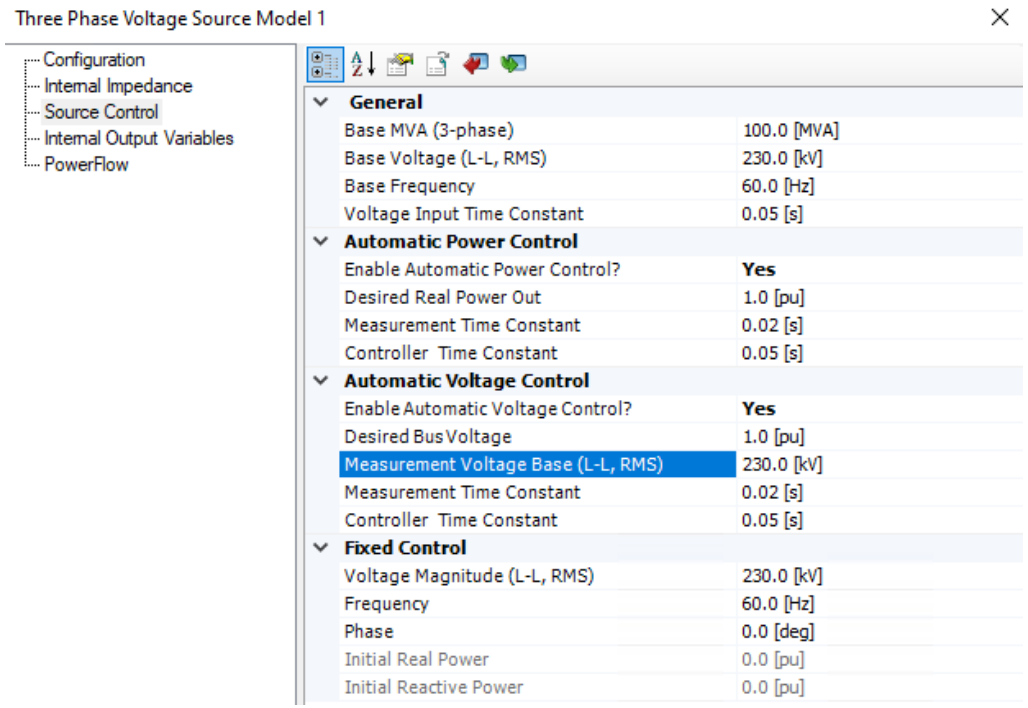
Task 3 Progress Review and Discussion – Matching Models on PSCAD and RTDS

- Build PSCAD model from scratch based on original IEEE 14 bus data
  - PSCAD library does not have the same components as RSCAD library – causes model matching challenges.

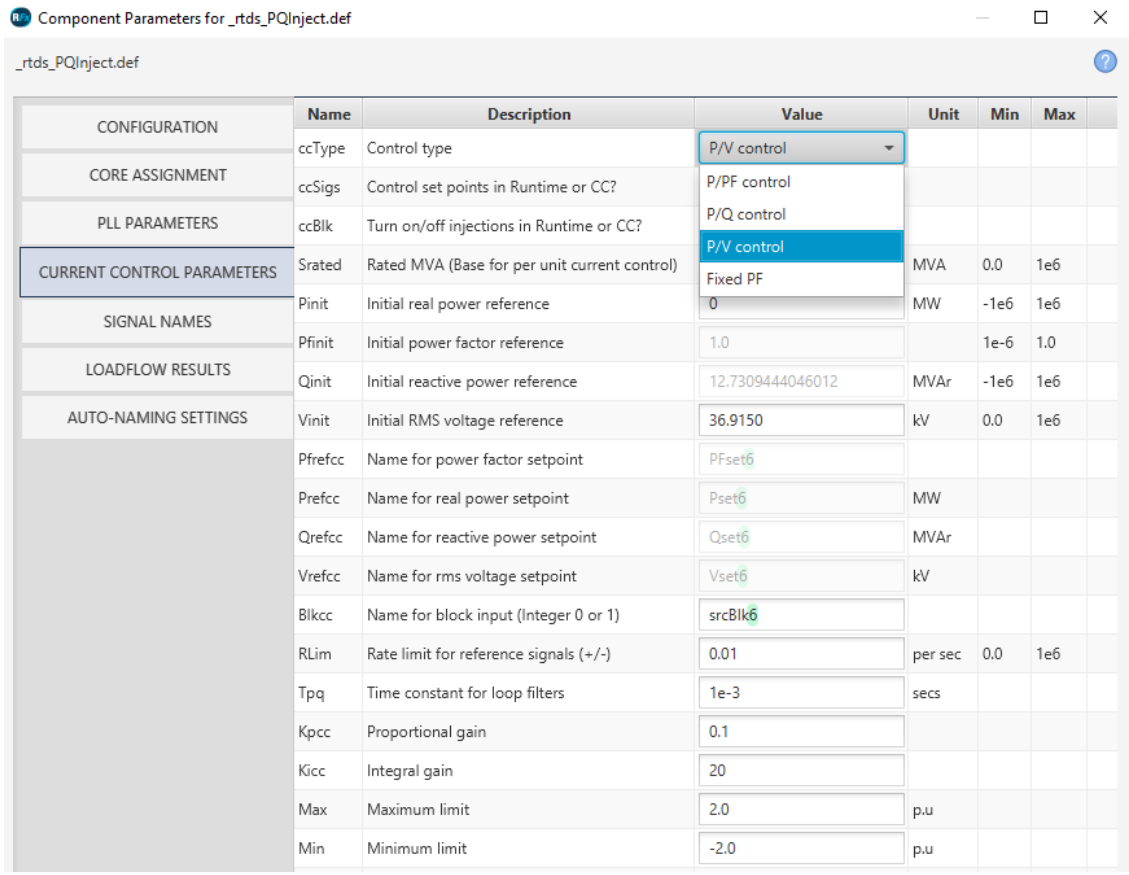


Source Model Differences between PSCAD and RSCAD

- Dynamic PQ and PV sources in PSCAD
  - No limits on the fault current magnitudes
  - PI controller becomes unstable when fault stays on for a long time



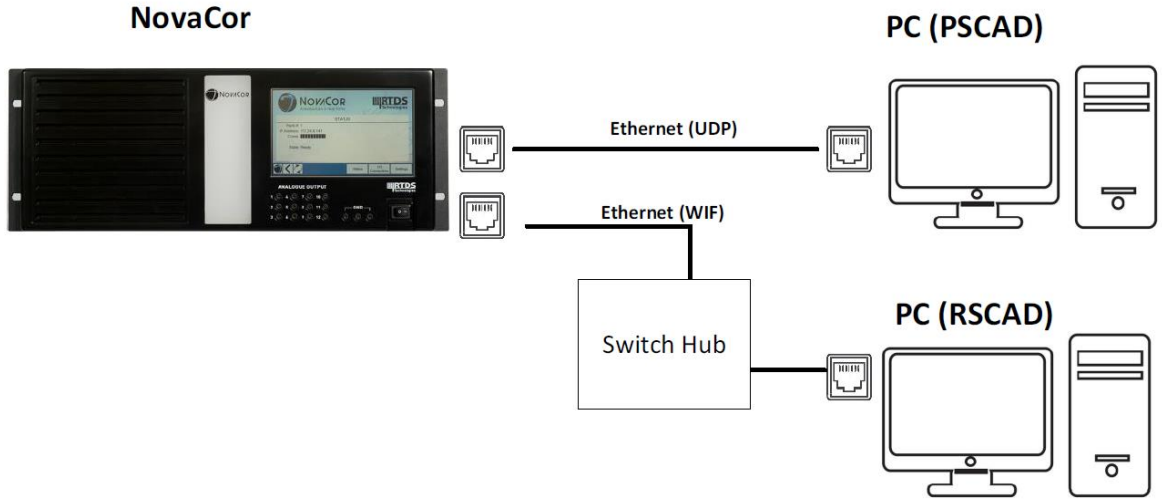
- Dynamic PQ and PV sources in RSCAD
  - Controlled current source
    - Uses PLL to track POI voltage

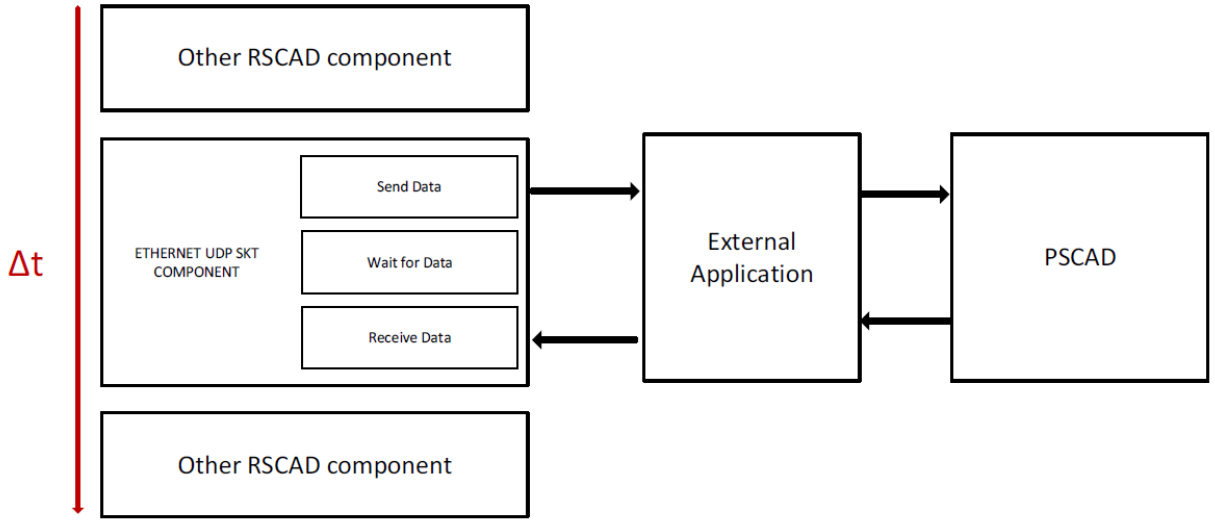


PSCAD-RTDS Co-Simulation Model Validation Results

PSCAD and RSCAD Co-Simulation

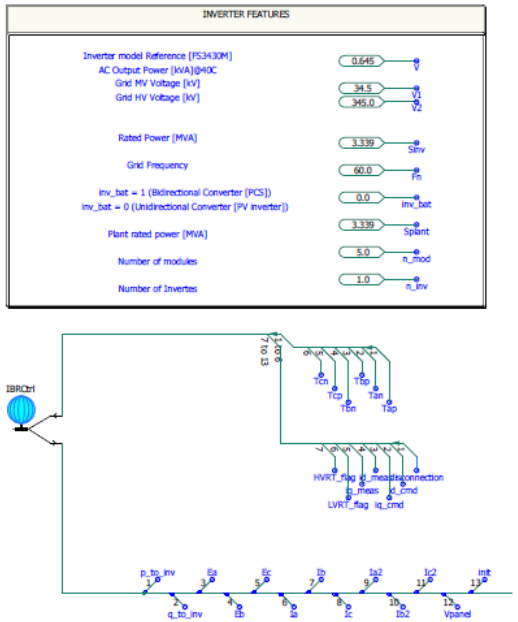
- To save time and avoid subtle model differences, the team decided to pursue RSCAD-PSCAD co-simulation approach.
  - Simulate power system and inverter hardware in RSCAD
  - Simulate IBR vendor black box controller in PSCAD
  - UDP interface exchanges analog measurements and control outputs between two platforms.
  - Limitations:
    - Does not support real-time co-simulation
    - RSCAD side only allow control inputs

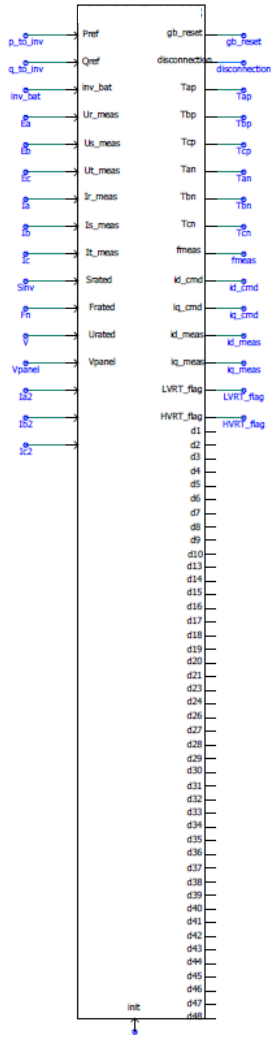




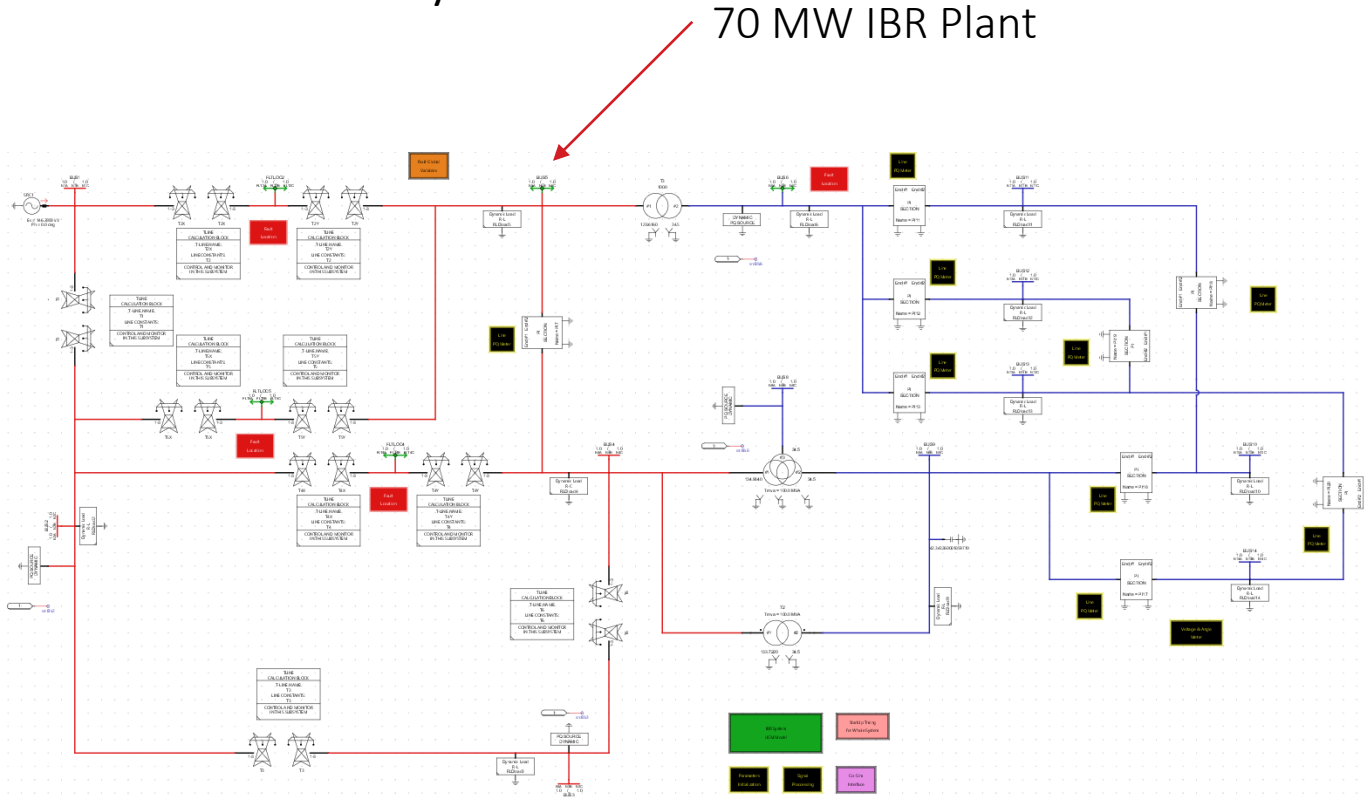
Co-Simulation Setup

- PSCAD
  - Inverter controller in the loop



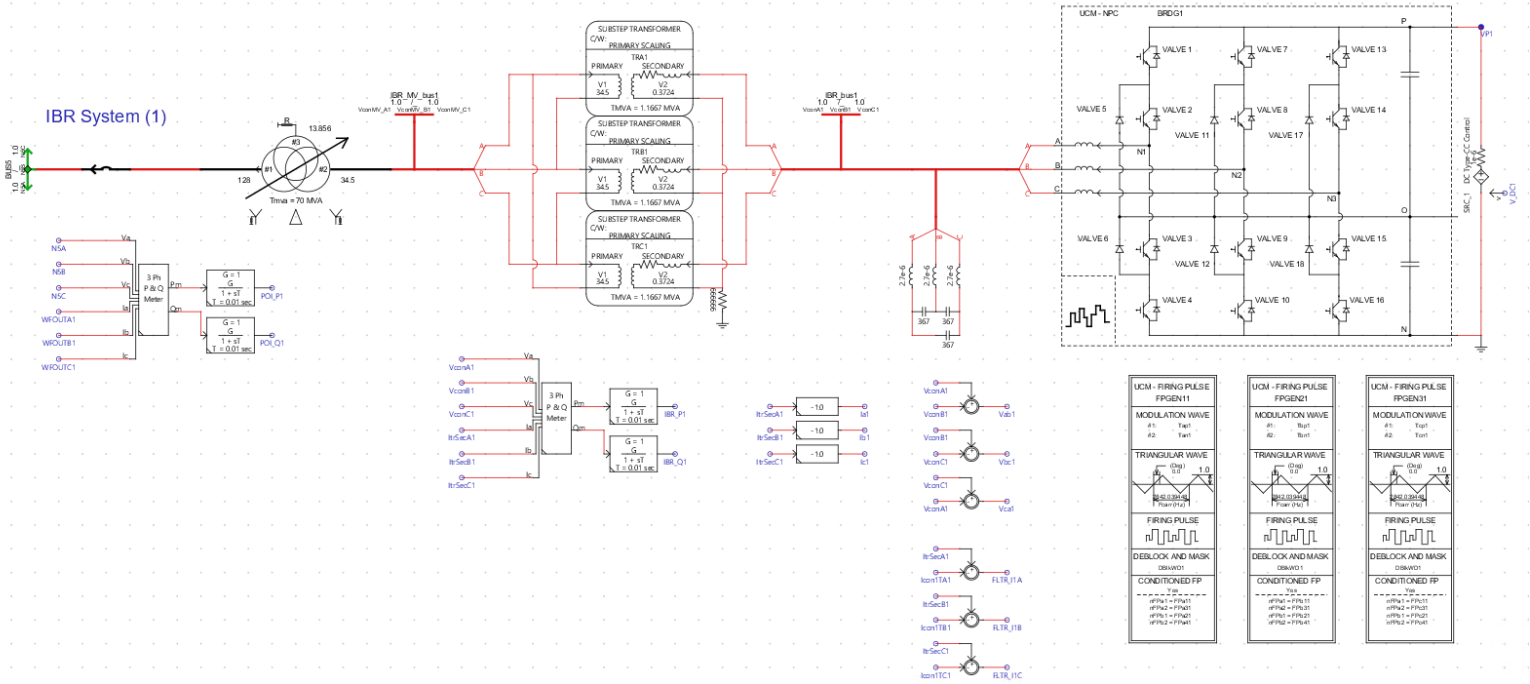


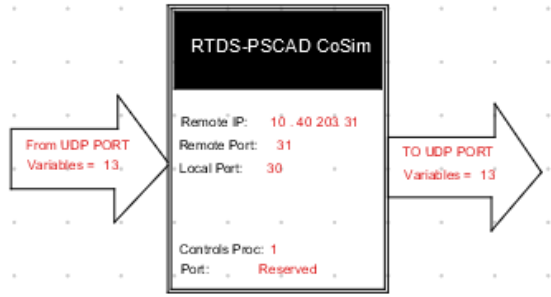
- RSCAD
  - Power system

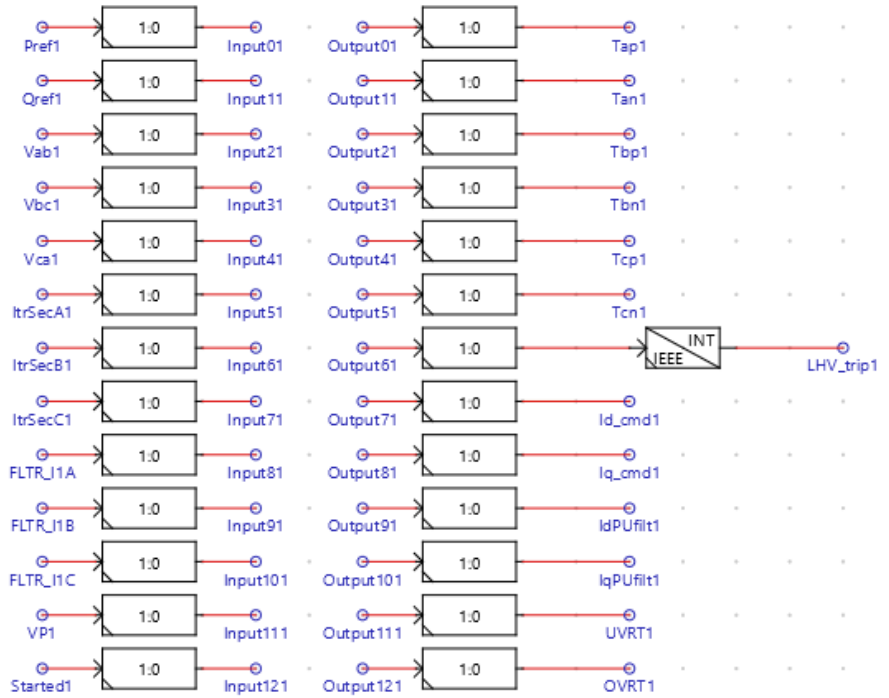


Co-Simulation Interface

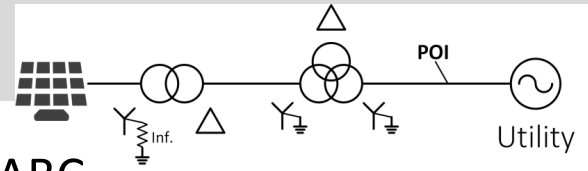
- RSCAD only has the inverter hardware
  - Controller inputs are sent from PSCAD



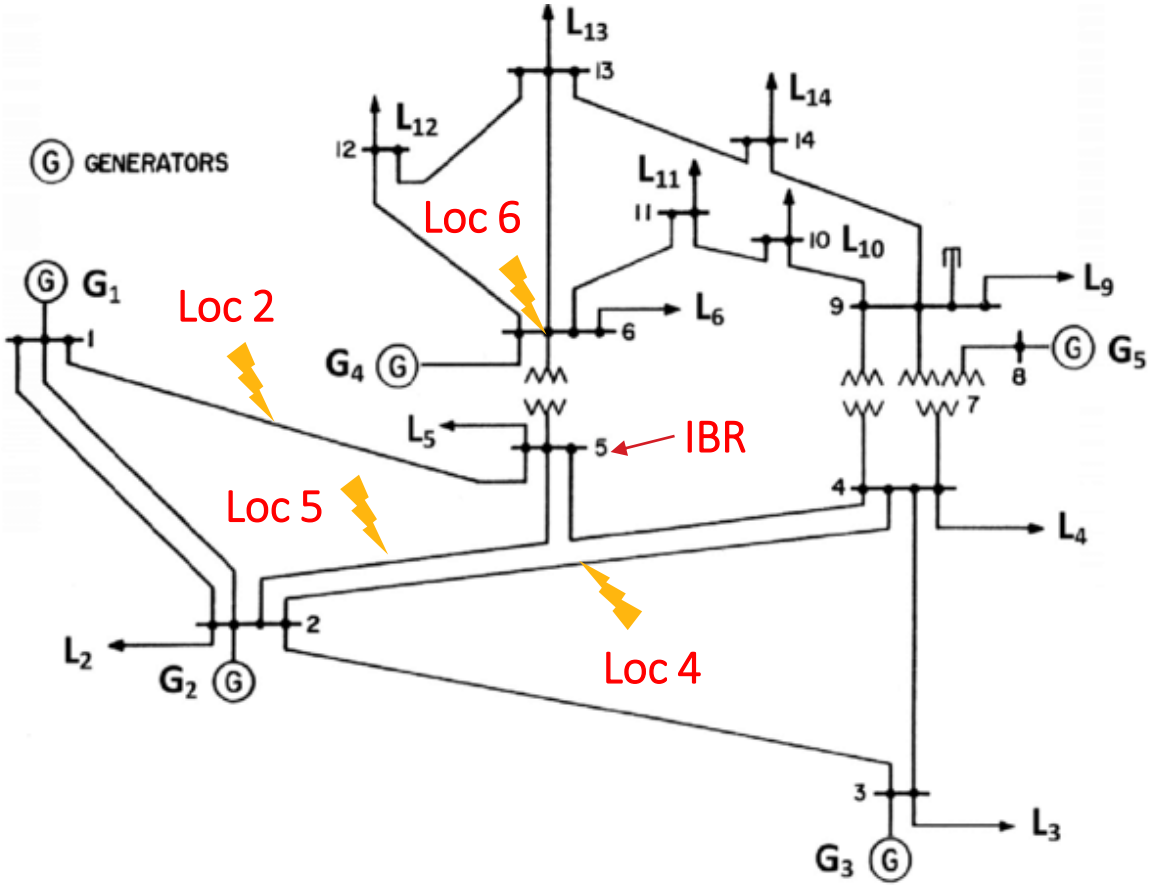




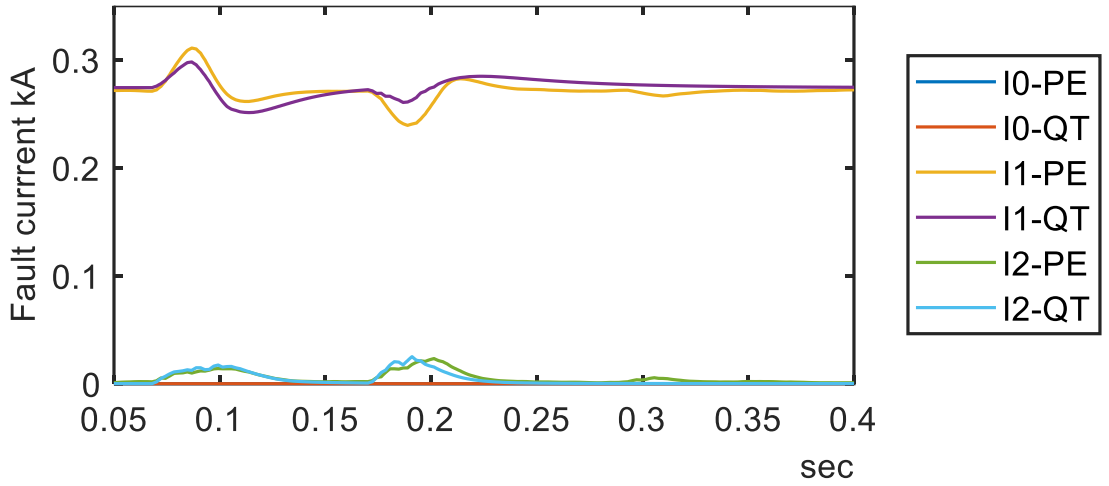
Fault Test Cases



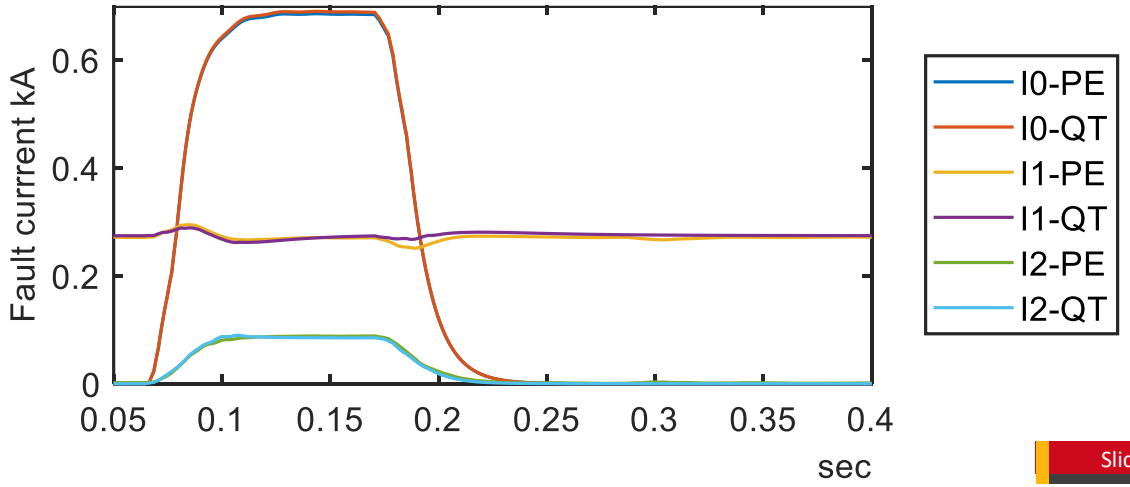
- IEEE 14 bus system
  - IBR connected to Bus 5
  - Loc 2 & 5 are internal faults
  - Loc 4 & 6 are external faults



- Fault current at POI: Loc 2 ABC



- Fault current at POI: Loc 2 ABG



IBR Fault Current Validation

- The overall Mean Absolute Error (MAE) is 0.0031 kA
- The maximum error is 0.0085 kA

Fault Cases	I0 MAE	I1 MAE	I2 MAE
FLTLOC_2_AB	0.0000	0.0051	0.0026
FLTLOC_2_ABC	0.0000	0.0070	0.0020
FLTLOC_2_ABG	0.0011	0.0053	0.0022
FLTLOC_2_AG	0.0016	0.0056	0.0021
FLTLOC_4_AB	0.0000	0.0049	0.0025
FLTLOC_4_ABC	0.0000	0.0071	0.0023
FLTLOC_4_ABG	0.0017	0.0055	0.0024
FLTLOC_4_AG	0.0015	0.0063	0.0022
FLTLOC_5_AB	0.0000	0.0054	0.0022
FLTLOC_5_ABC	0.0000	0.0085	0.0025
FLTLOC_5_ABG	0.0023	0.0059	0.0025
FLTLOC_5_AG	0.0026	0.0065	0.0023
FLTLOC_6_AB	0.0000	0.0067	0.0019
FLTLOC_6_ABC	0.0000	0.0055	0.0012
FLTLOC_6_ABG	0.0032	0.0049	0.0021
FLTLOC_6_AG	0.0017	0.0070	0.0020

Conclusions

- Best practices in matching black-box vendor models of IBRs in RSCAD
  - Quasi steady-state response matching
    - Focus on filter time constants, PID gains, voltage-dependent current limits, ramp rates, etc.
  - Fault transient response matching
    - Focus on HLVRT, protection functions, etc.
  - System interactions matching
    - Connect to developed IEEE-14 bus systems and focus on internal and external fault responses.
- Synchronous generator model parameter estimation tools can be applied for IBR model development.
- PSCAD-RTDS co-simulation feature is a powerful way to perform IBR software controller-in-the-loop simulation.
- IBR model validation can be done accurately using PSCAD-RTDS co-simulation.