The CHILplug

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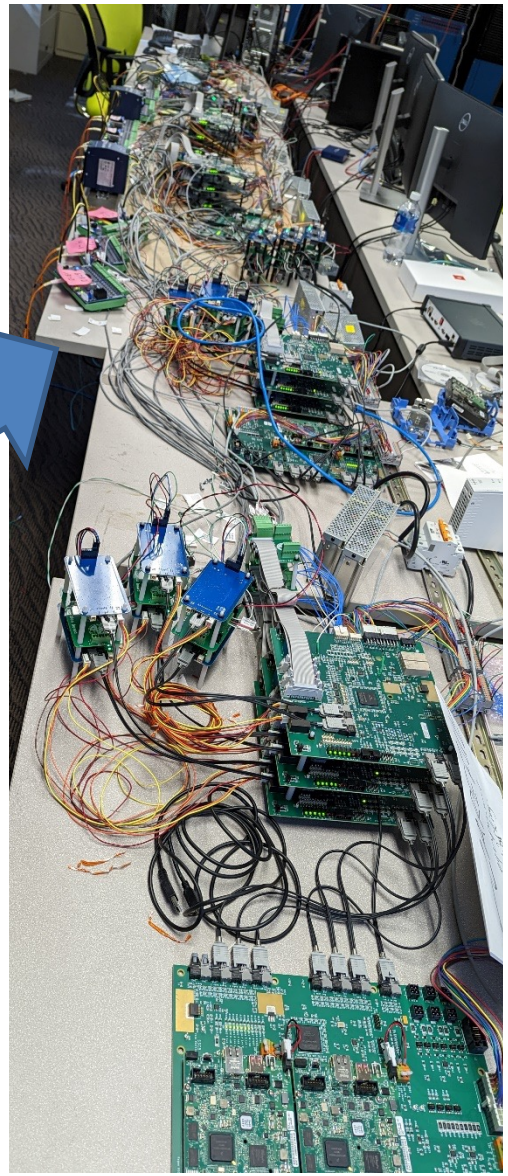
TECO CHIL Installation

CHIL

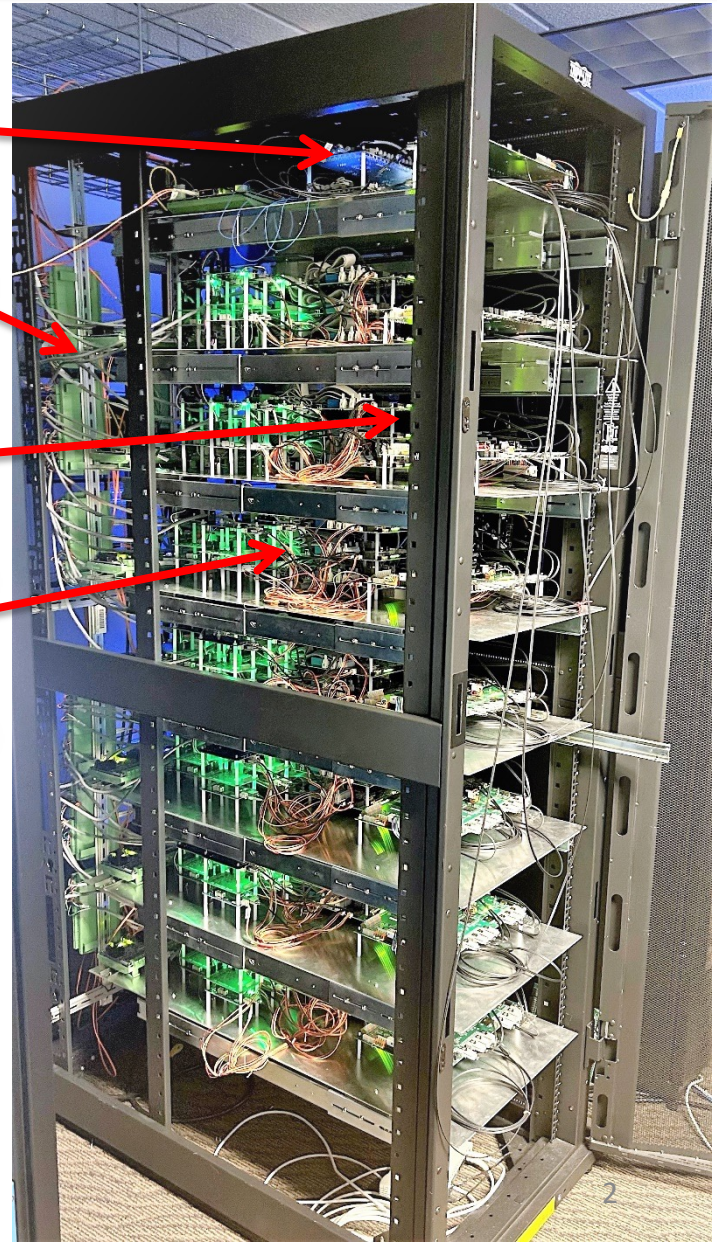


Master/Mains Controllers Shelf

RTDS Interface Cards

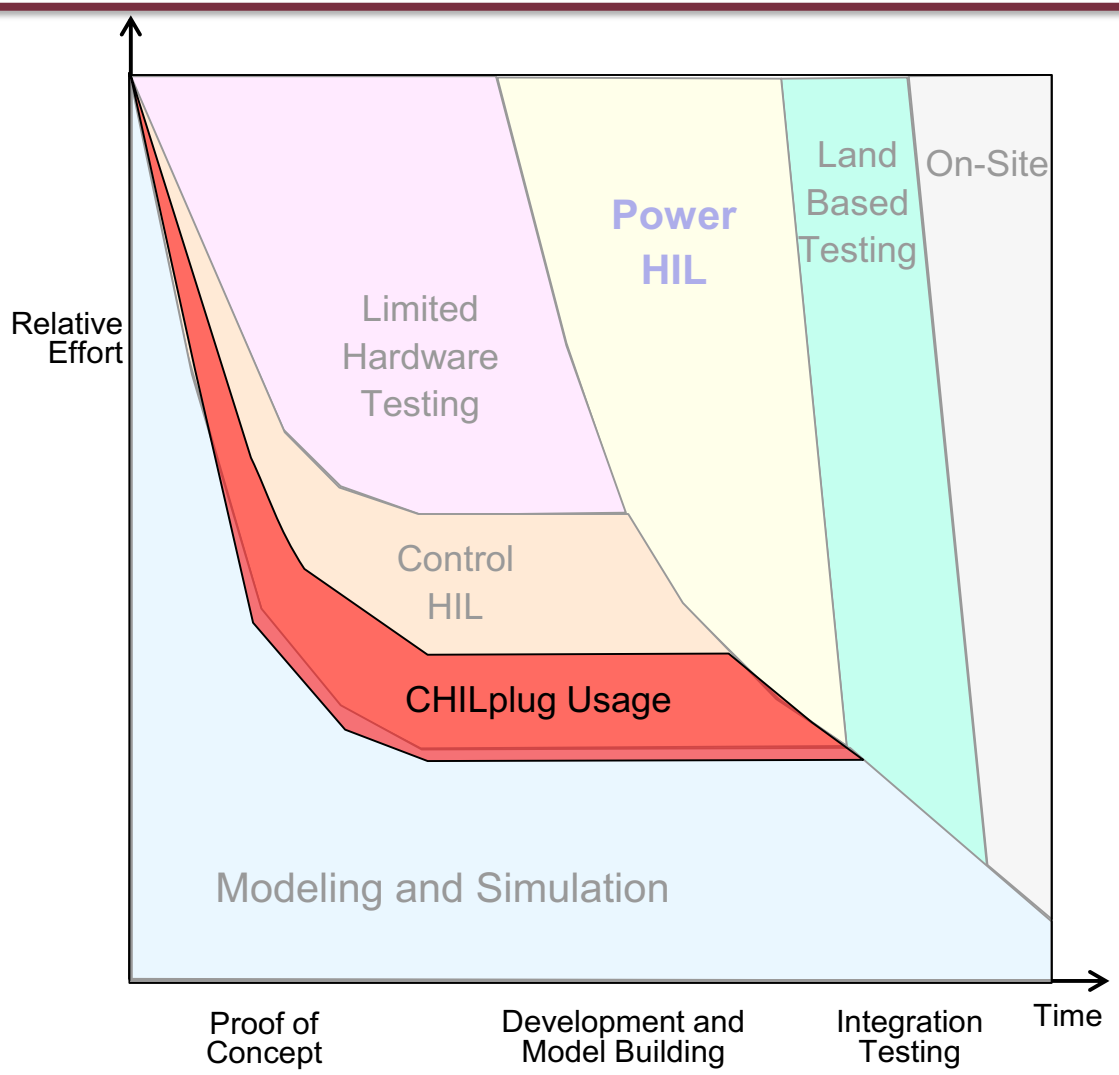
Slice Controller

Cube Controllers



Introduction

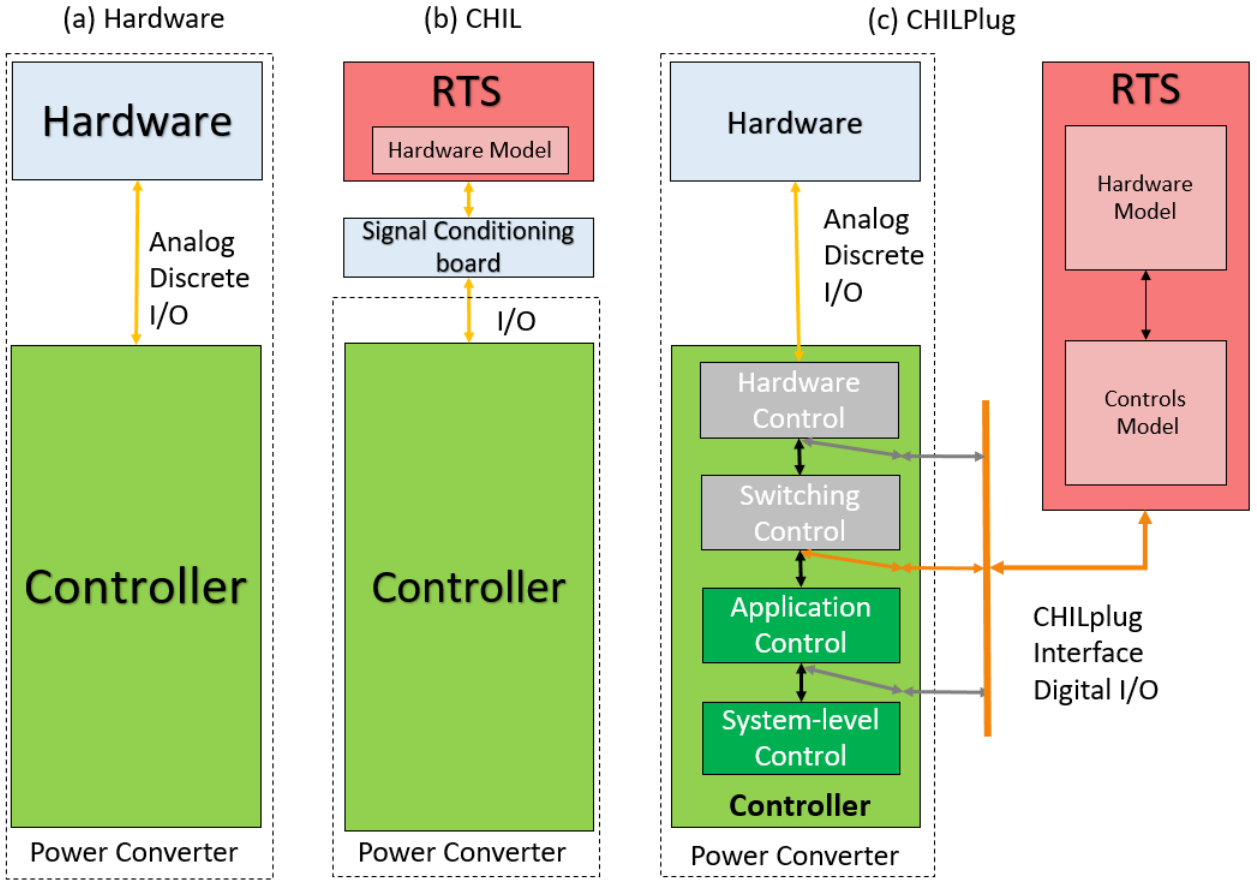
- Power electronic converter (PEC) controllers
- Controller-hardware-in-the-loop (CHIL) test
- CHIL challenges
- A need for…
  - CHIL interface (the CHILplug) integrated with PEC controller
  - Facilitates development and testing of controller over PEC lifetime



Potential CHILplug usage during the design and development process [1]

The CHILplug concept

- Traditional CHIL
  - Modifies PEC
- The CHILplug concept
  - Dedicated computer network to/from RTS
- Testing with the CHILplug
  - Software plug between PEC controller layers

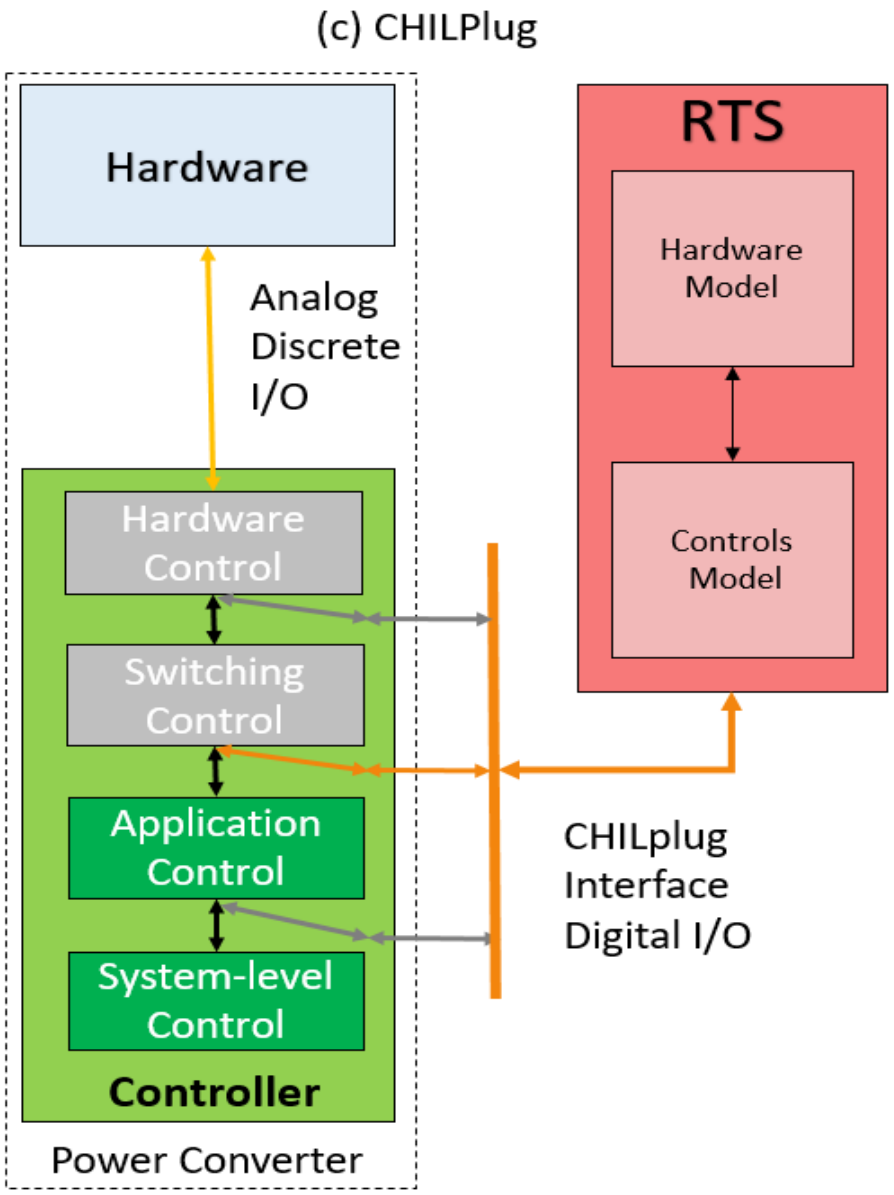


The CHILplug concept [1]

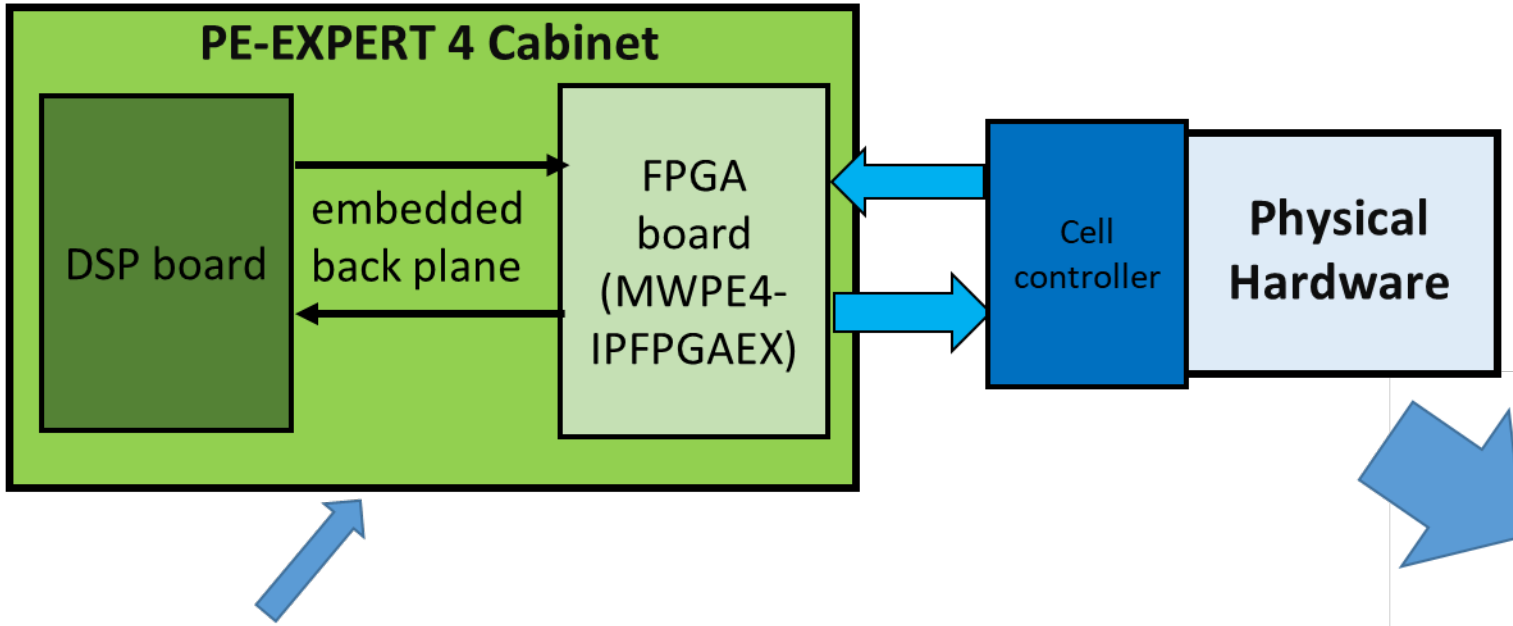
Steurer, M., Schoder K., Stanovich M., LåΩangston J., *Interface for power systems,* U.S. Patent 11,016,452 B2 , May 25, 2021. https://patents.google.com/patent/US11016452B2/en?oq=11016452

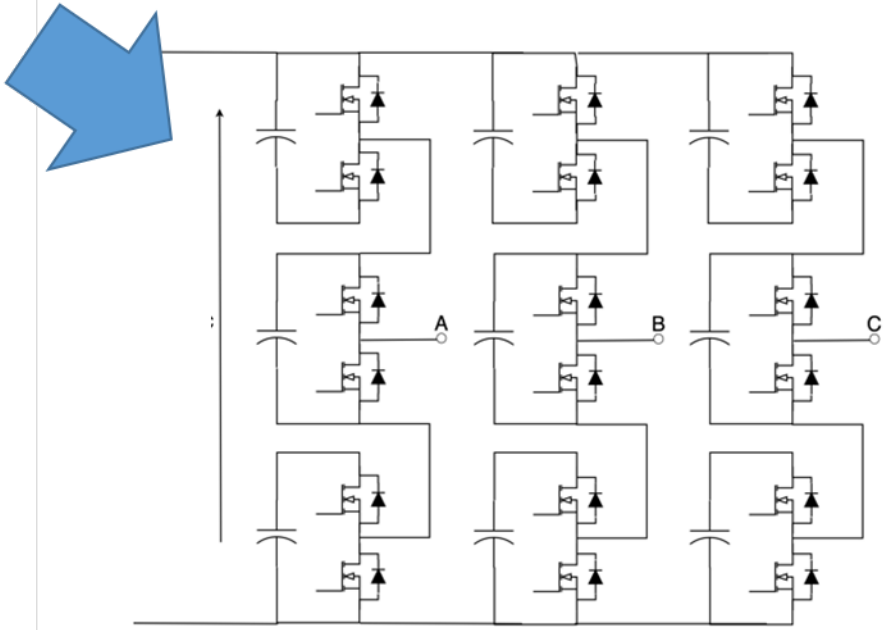
The CHILplug

- Controller internal signals can be exchanged with RTS
- Allows for incremental development and testing of controllers with an RTS
- Simplified connection between RTS and controller



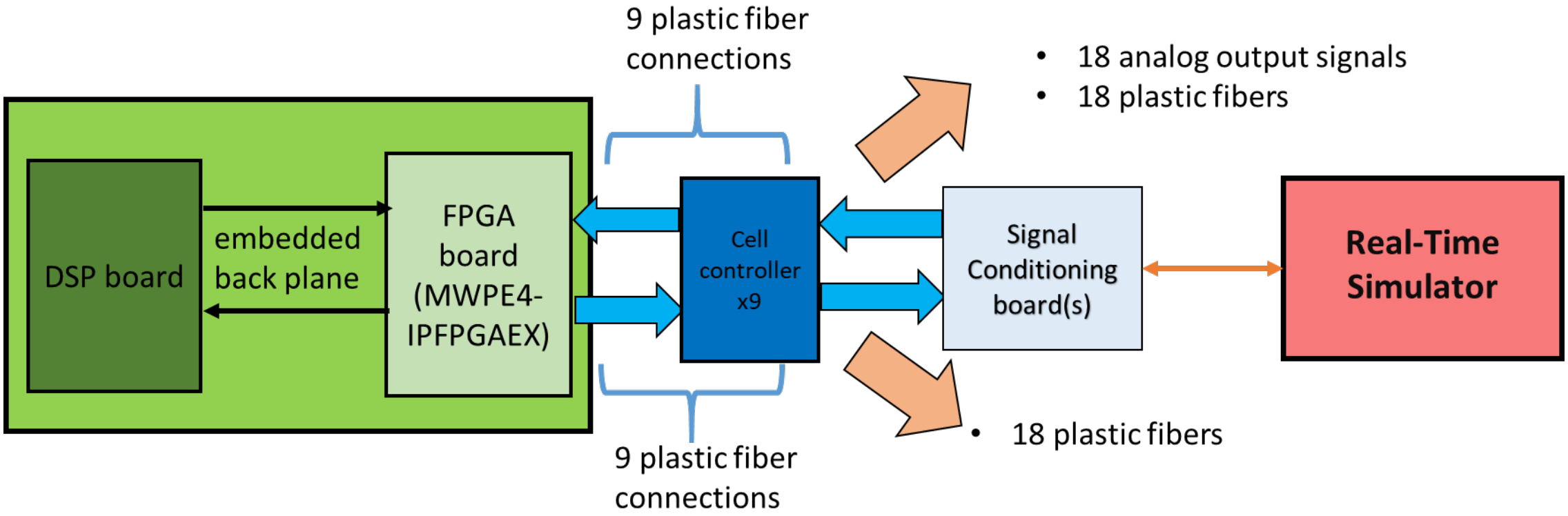
SC-MMC Application





SC-MMC application diagram

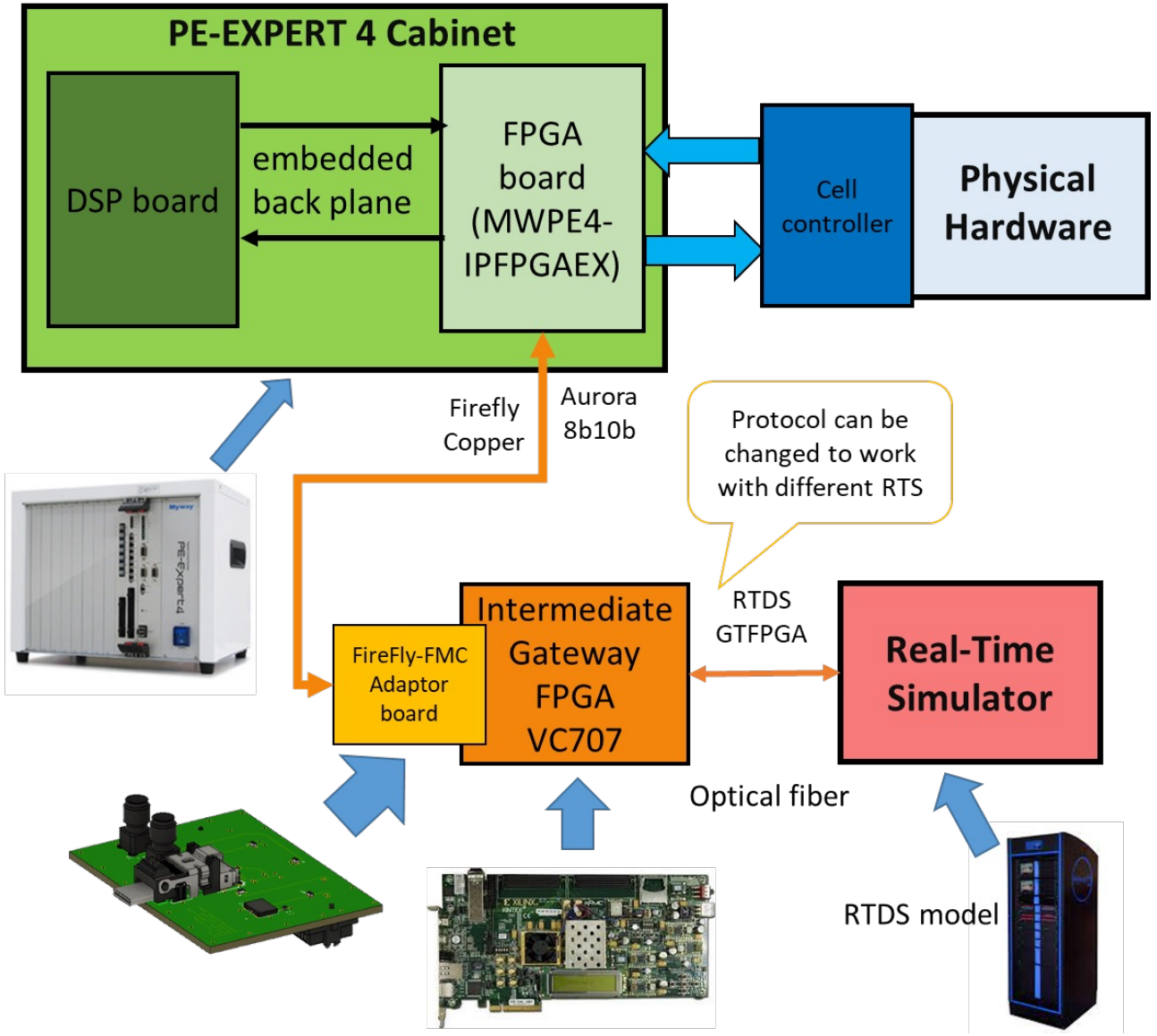
Traditional CHIL setup



Traditional CHIL setup diagram

First CHILplug Implementation

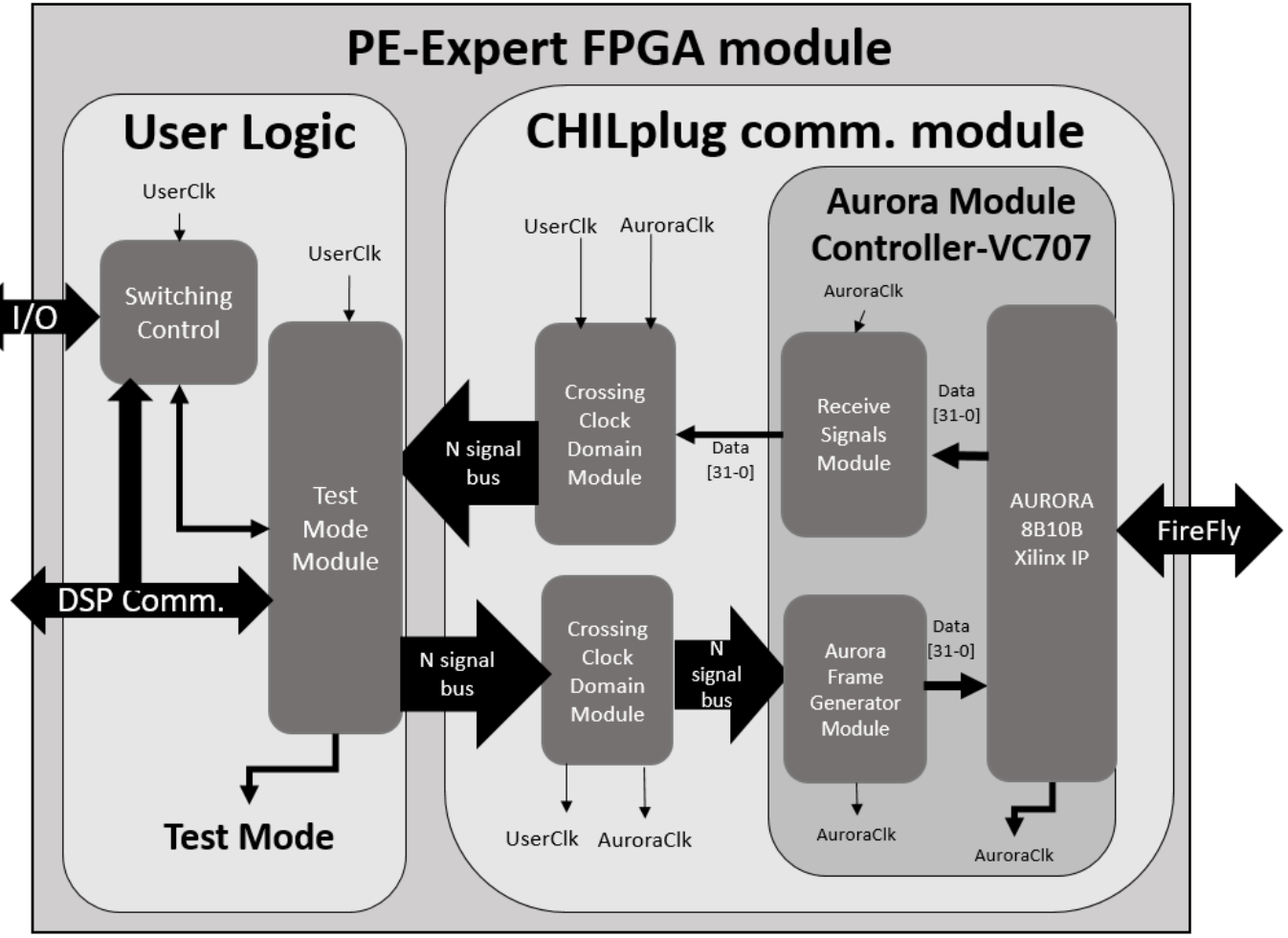
- Switched-Capacitor Modular Multilevel Converter (SC-MMC) Project
  - PE-Expert controller:
- CHILplug requirements
  - Minimum 1 Gbps throughput
  - CHILplug interface at FPGA to be able to connect to switching control layer



First CHILplug implementation [1]

CHILplug Interface - Controller

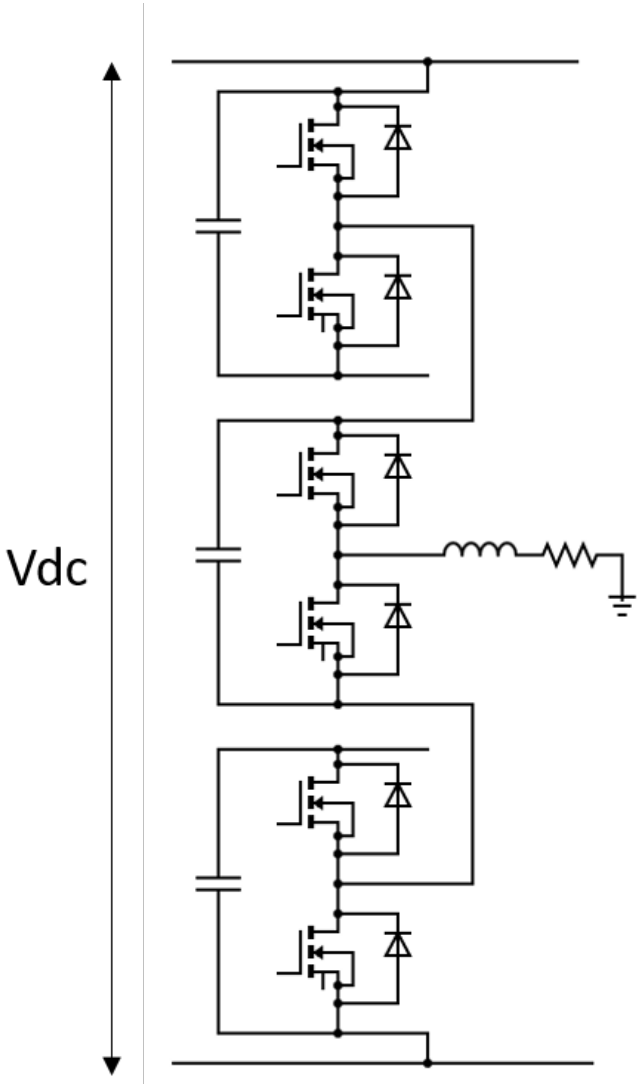
- CHILplug interface location
  - Communication at switching control layer hardware
- CHILplug communication module
  - Aurora 8b10b protocol at 2 Gbps
  - Compatible with RTDS
- Communication channel specifications
  - 32 signals of 32 bits
  - Channel loopback latency for 32 signals, 2x5us time steps



CHILplug main controller's FPGA modules

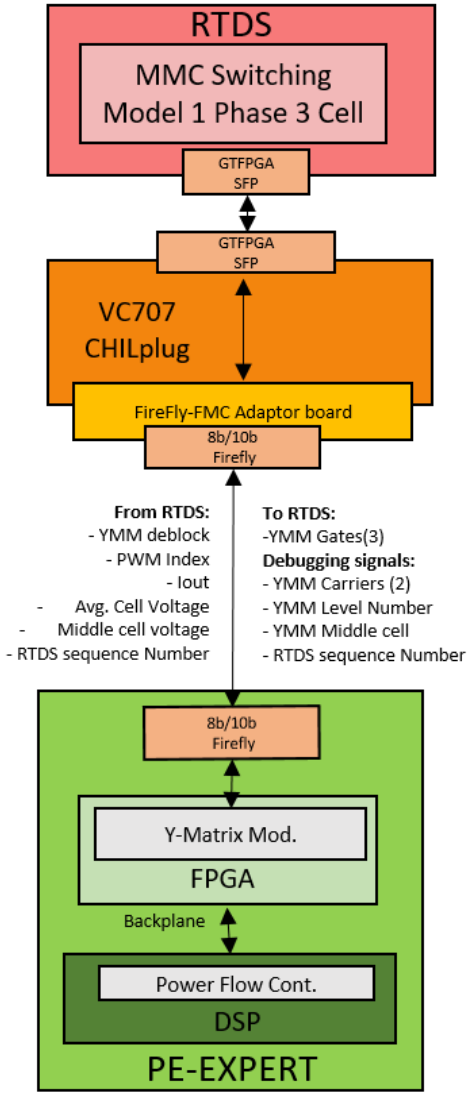
CHILplug Validation

- CHILplug test setup vs. CHIL test setup vs. Hardware Setup
- Controller design for a SC-MMC operates at 4.16 kVac and a dc-bus of 7-8 kV.
  - Initial tests performed for one phase open-loop to test modulation
  - Utilizing Y-Matrix Modulation [2] which requires mid-cell voltage and current in order
- Development and Testing process
  1. CHILplug testing
  2. CHIL testing
  3. Hardware Test



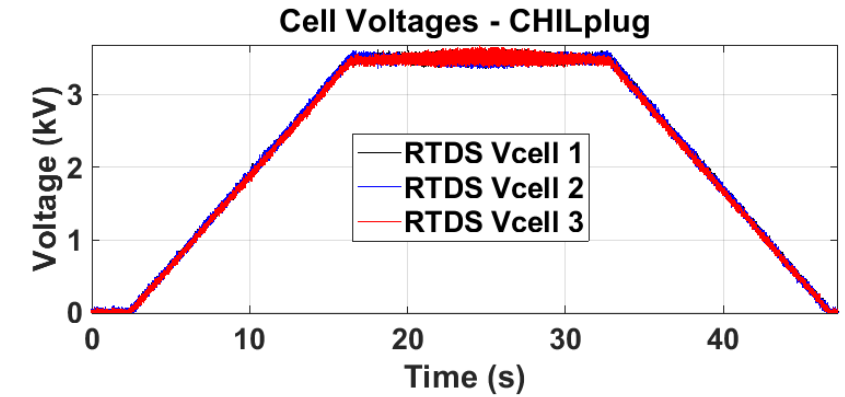
SC-MMC - single phase

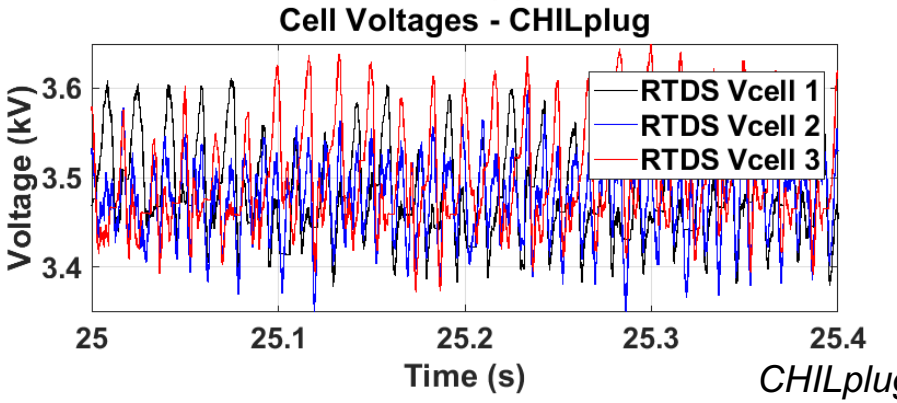
CHILplug Test

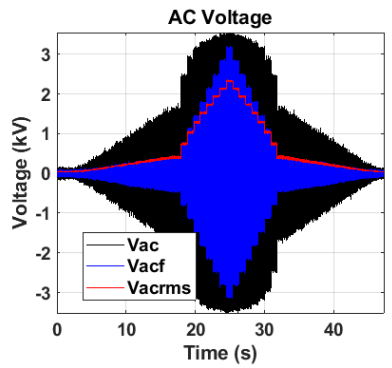


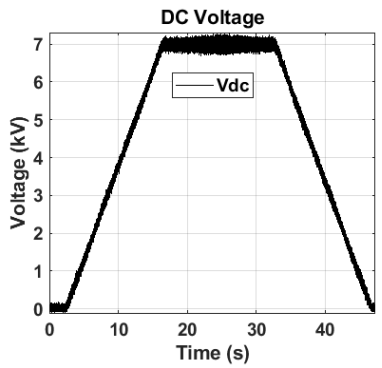
CHILplug test setup [3]

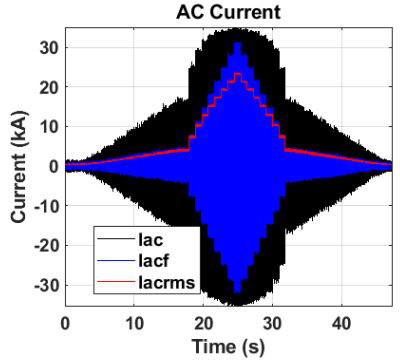
- Test purpose:
  - Verify cell balancing
- RTDS model
  - 1 phase of SC-MMC

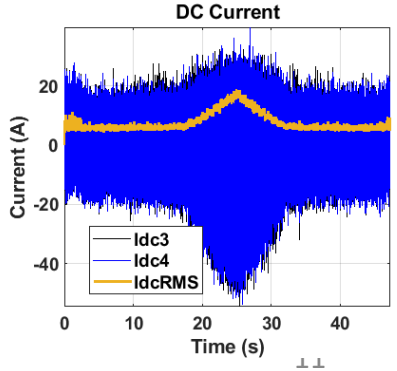








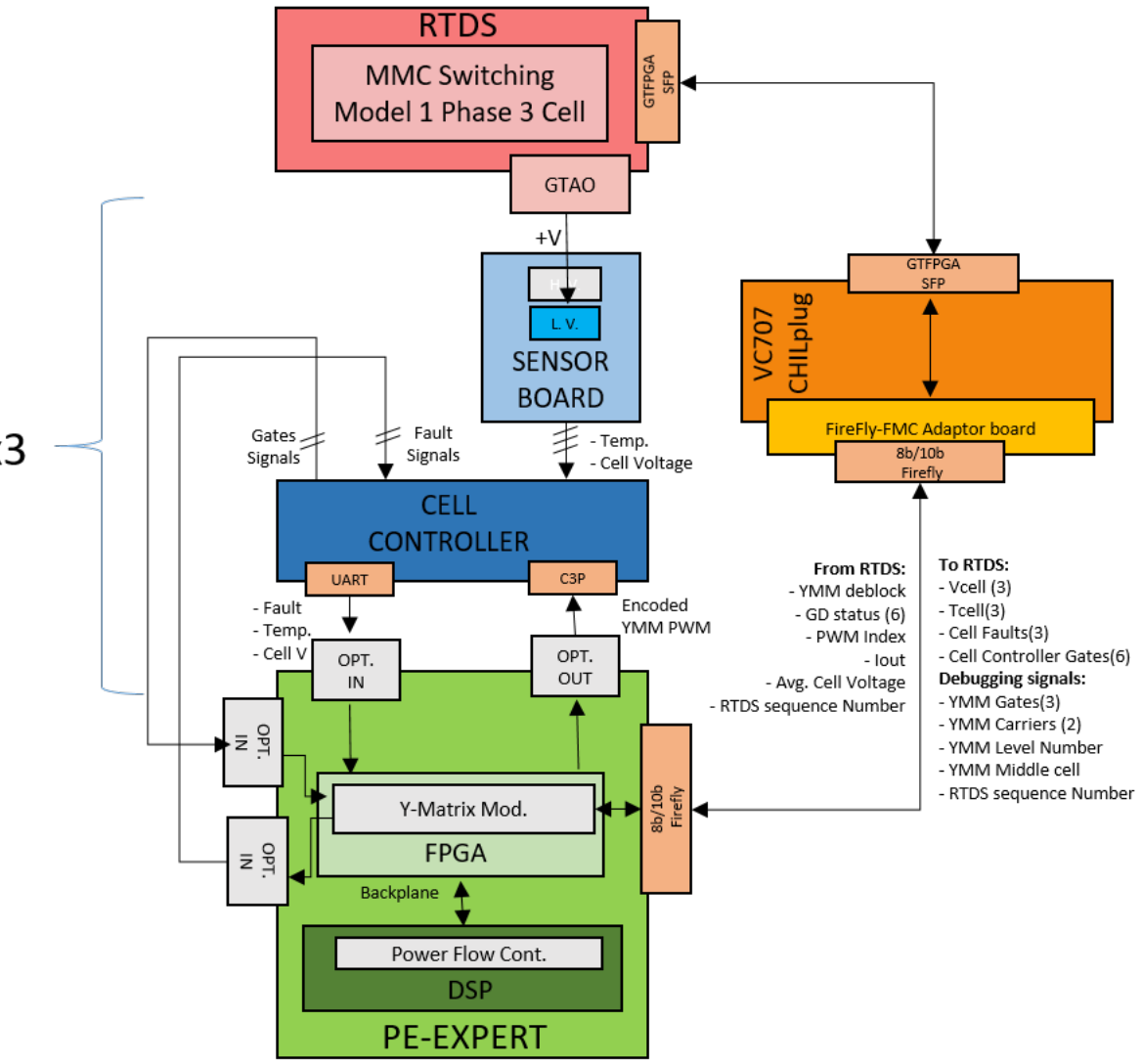




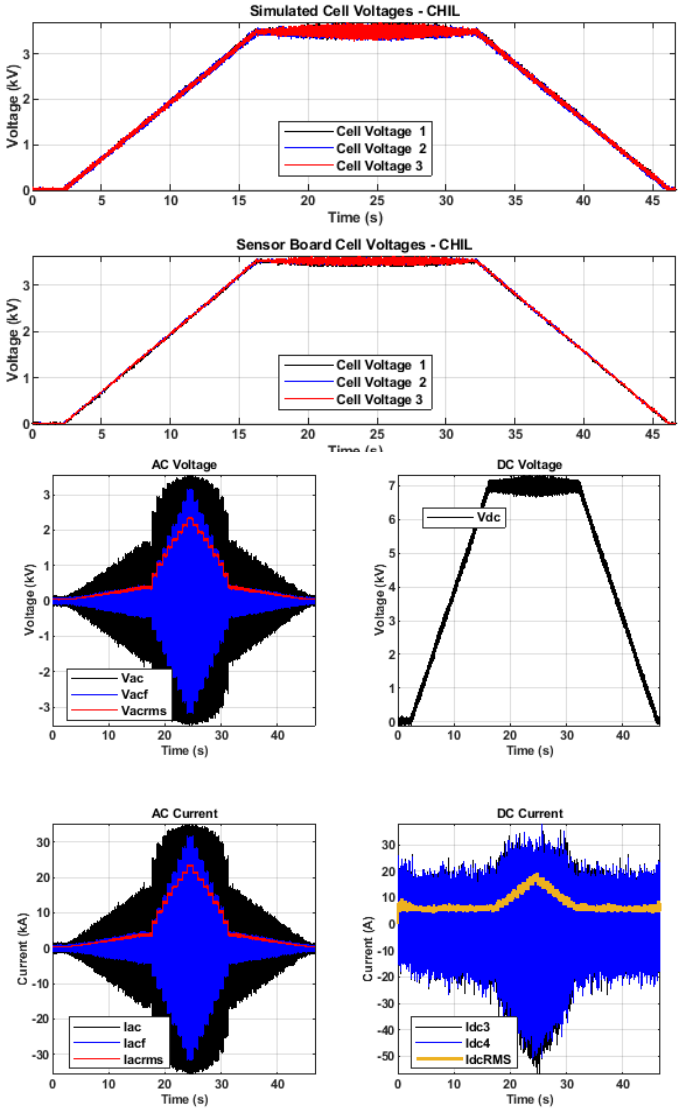
CHILplug test results [3]

CHIL Test

- Adding cell controllers to setup
- Using CHILplug as debugging tool

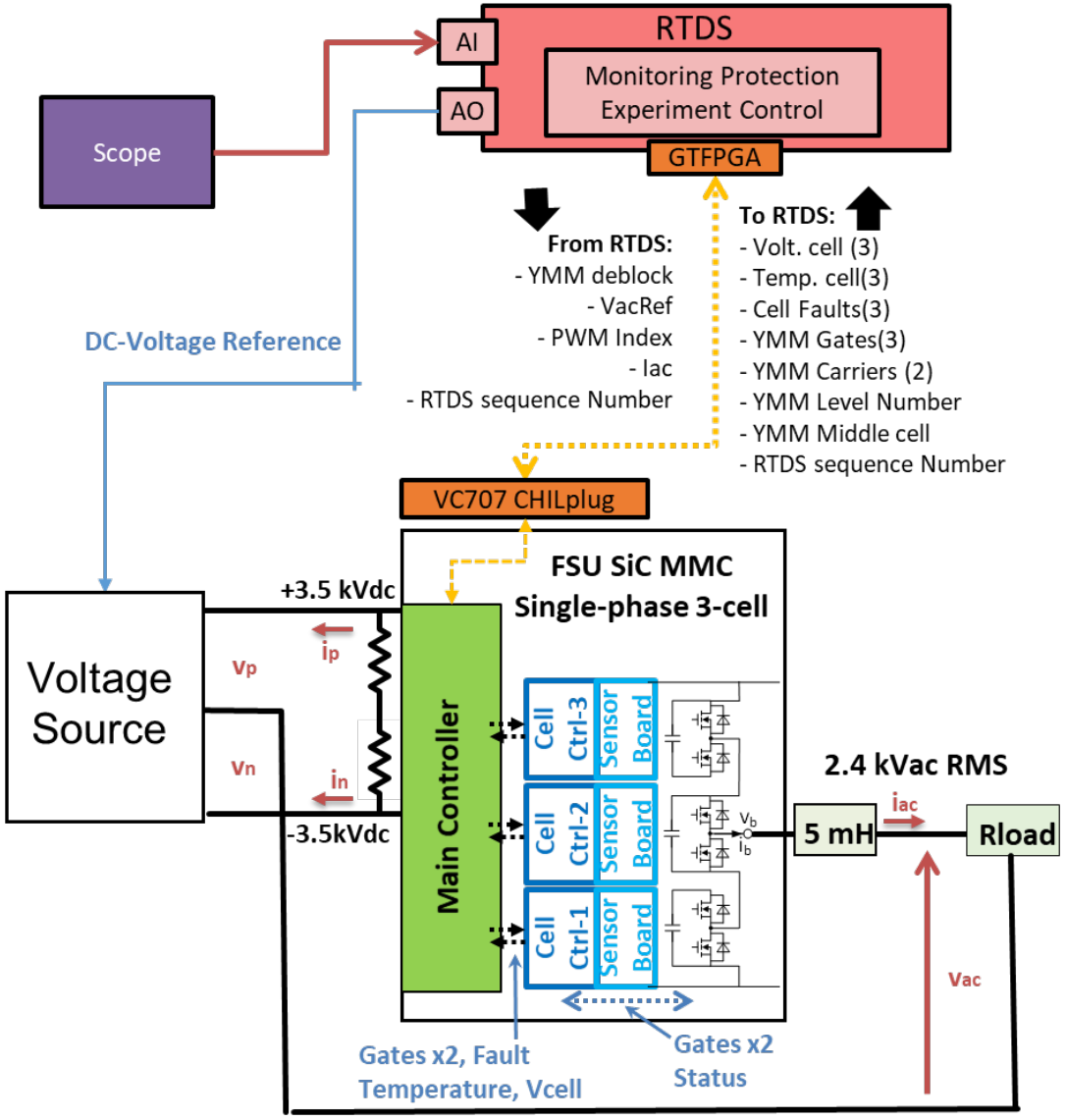


CHIL test setup [3]

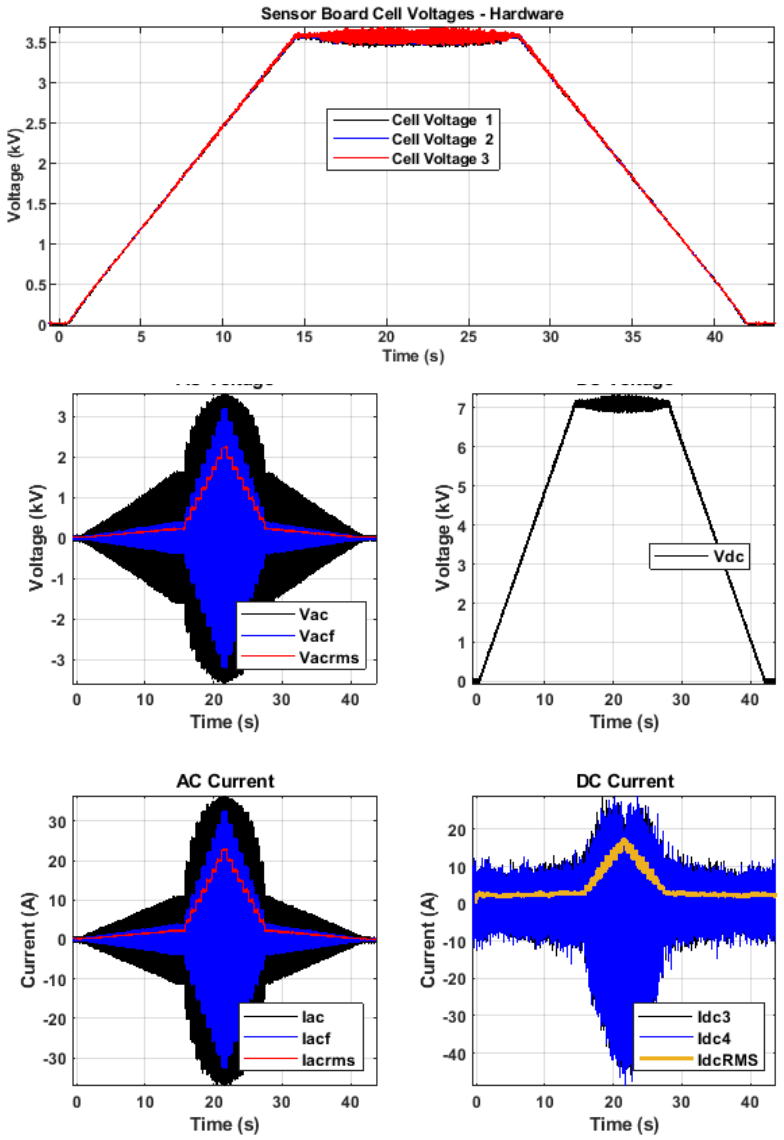


CHIL test results [3]

Hardware Test

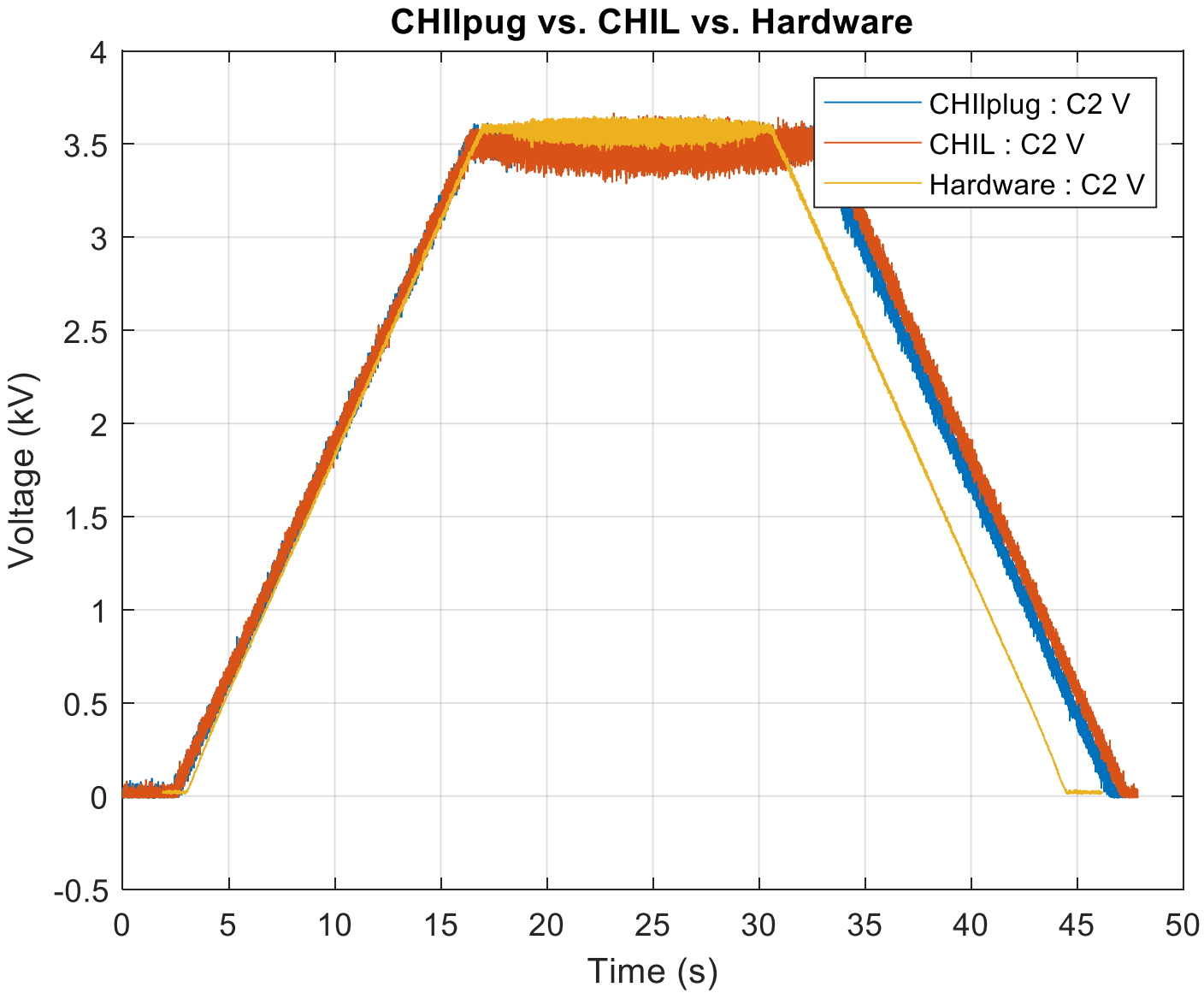


Hardware test setup [3]



Hardware test results [3]

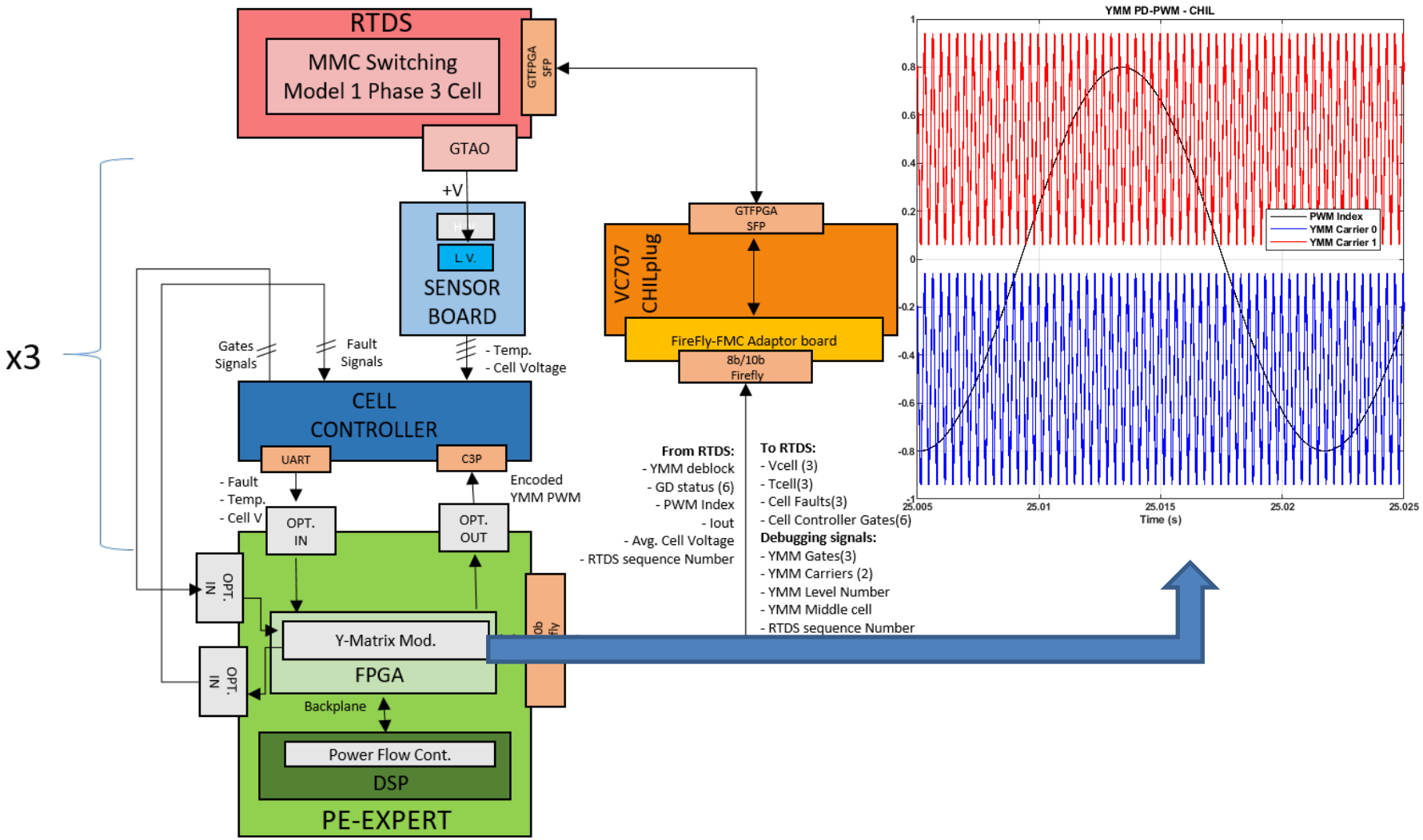
Result Comparison



Middle cell voltage comparison across the different tests

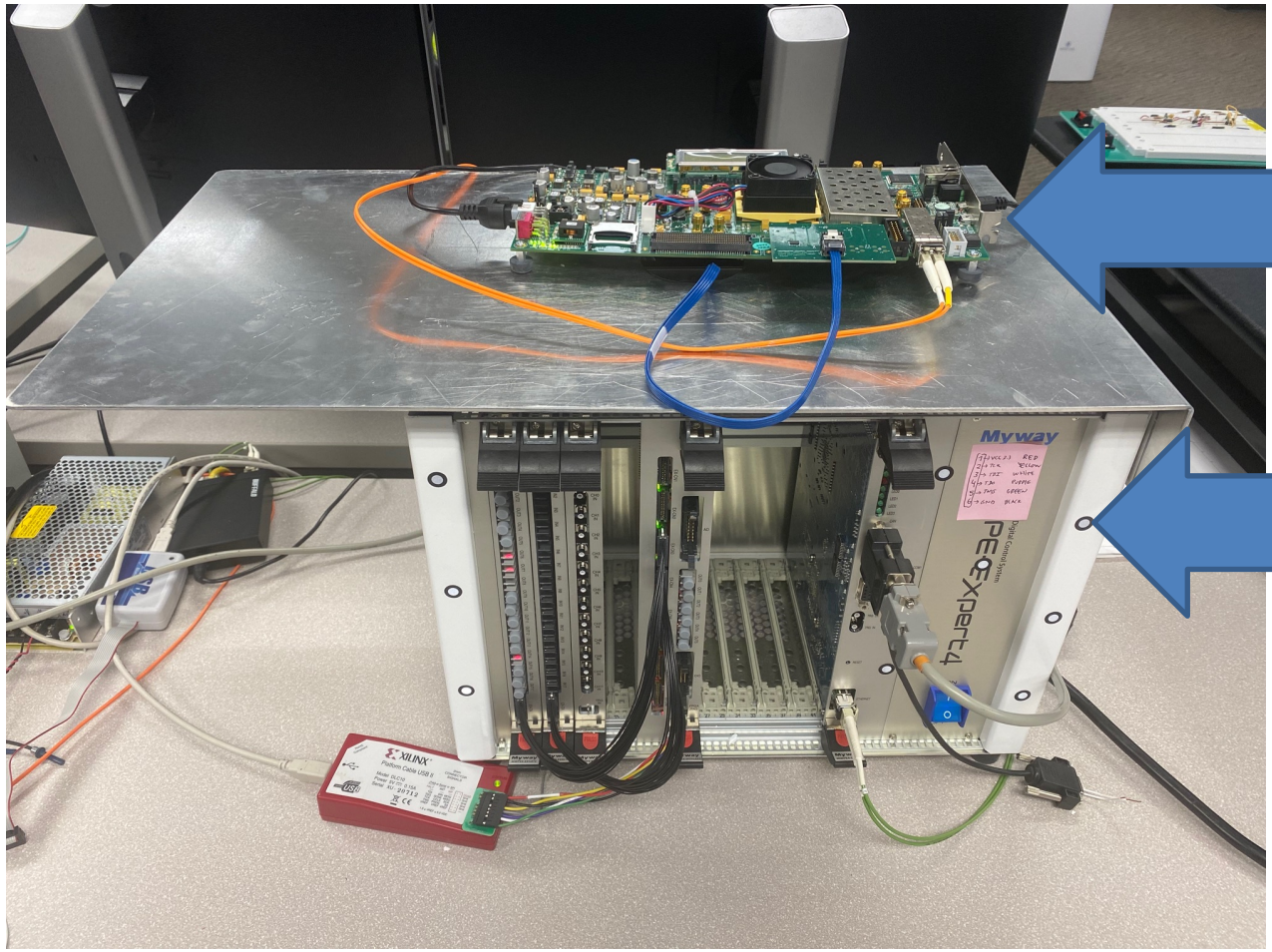
Using the CHILplug for debugging

- Cell controller faulty operation when added to CHIL
- Modulation previously verified using CHILplug
- Issue on communication interface



Lessons Learned

- Upfront cost
  - Controller with CHIL interface compatible with RTS
  - PE-Expert controller FireFly cable issues
- Communication line rates
- CHILplug supplements rather than replaces traditional CHIL



Conclusion

- The CHILplug concept
  - Convenient converter controller interface to RTS
  - Facilitates transition between offline and CHIL development stages
  - Reduces complexities in setting up a CHIL environment
- Additional benefits
  - Additional high-speed interface available through all development stages for:
    - Debugging
    - Data recording
- Usefulness
  - The CHILplug physical interface standardization to avoid costly one-off solutions
- Future work
  - Establish a more rigorous definition for the CHILplug process

Acknowledgment:
This work was in part sponsored by the Grid DoE-AMO Application Development, Testbed and Analysis for MC SiC (GADTAMS) project.

Refereces

- [1] I. Barnola, M. Stanovich, M. Steurer, K. Schoder, H. Pourgharibshahi, and R. F. Yehia, “CHILplug: Development and demonstration of a communication-based CHIL interface,” ASNE AMTS, 2022.
- [2] Q. Yang, H. Pourgharibshahi, R. B. Gonzatti, S. Martin, H. Li, and F. Peng, “Modular multilevel converter with minimum arm inductance and automatic sub-module voltage balance - y-matrix modulation and its theoretical proof of the automatic voltage balance,” in 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2417–2422, 2020.
- [3] I. Barnola, M. Stanovich, K. Schoder,S. Song,and M. Steurer, “SC-MMC Controller Validation Using a CHILplug Interface,” IEEE ESTS, 2023.
- Patent: Steurer, M., Schoder K., Stanovich M., LåΩangston J., *Interface for power systems,* U.S. Patent 11,016,452 B2 , May 25, 2021. https://patents.google.com/patent/US11016452B2/en?oq=11016452

Thank you for your attention