N00014-16-1-2956

CHIL setup for a Reconfigurable MW Class PHIL Amplifier

M. Bosworth, D. Soto, M. Steurer, J. Hauer, K. Schoder, J. Bell, D. Spencer, B. Shonka, M. Stanovich
Center for Advanced Power System
Florida State University
Tallahassee, FL, USA

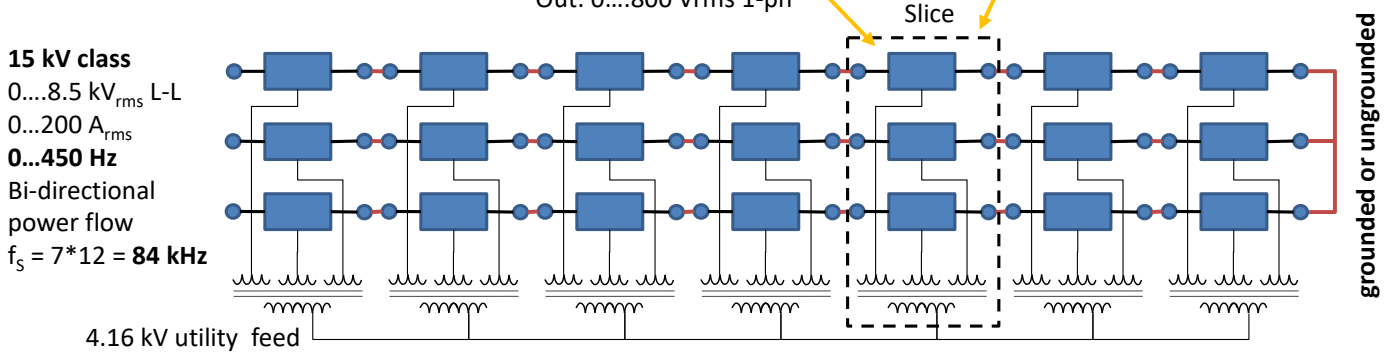
M. Ordonez, D. Chambless, S. Patnala
TECO-Westinghouse
Austin, TX

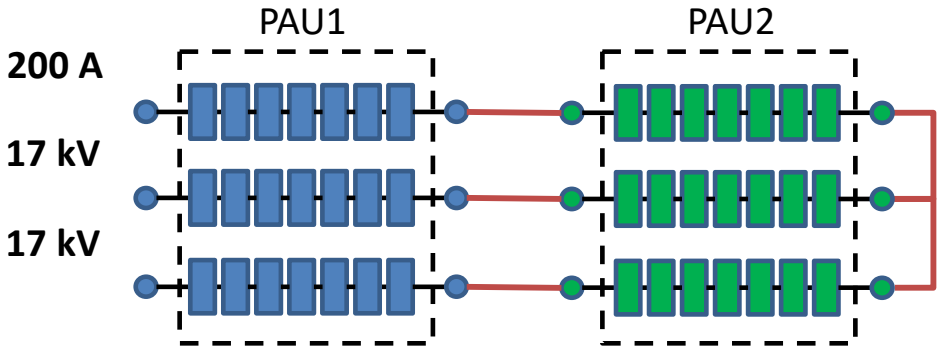
NEW – Reconfigurable MW Class PHIL Amplifier

TECO Westinghouse

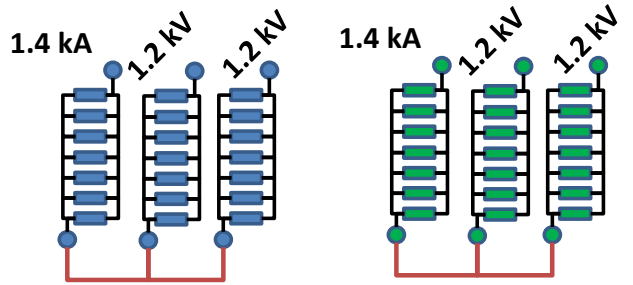
2 x Power Amplifier Units (PAUs) in CAPS MVDC Lab

Cube
In: 600V AC, 3-ph, 60 Hz
Out: 0….800 Vrms 1-ph

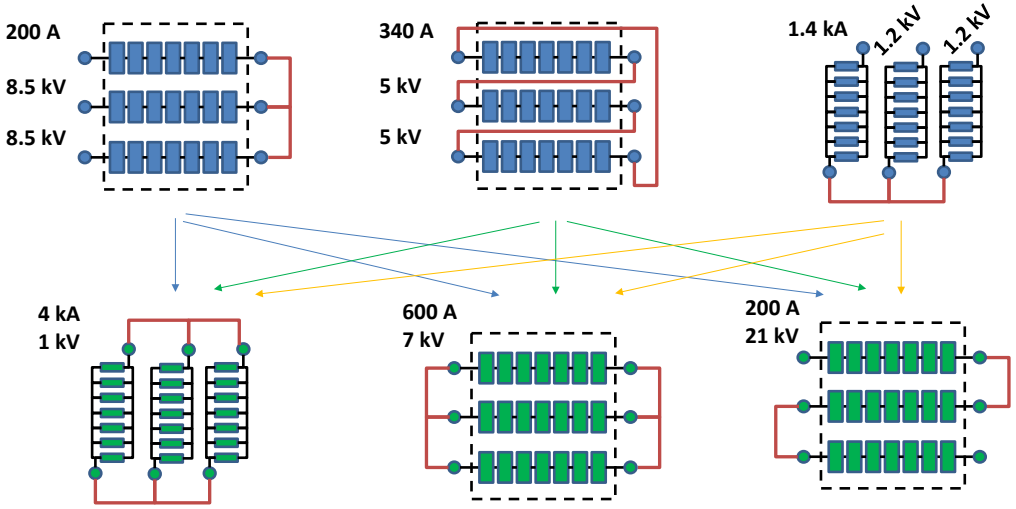




15kVac class PHIL interface



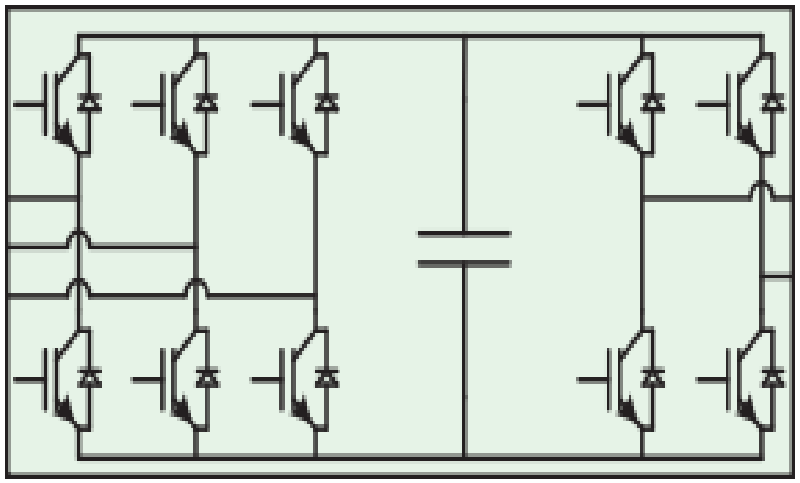
6-phase PHIL interface



Dual-PHIL interfaces at various voltage classes

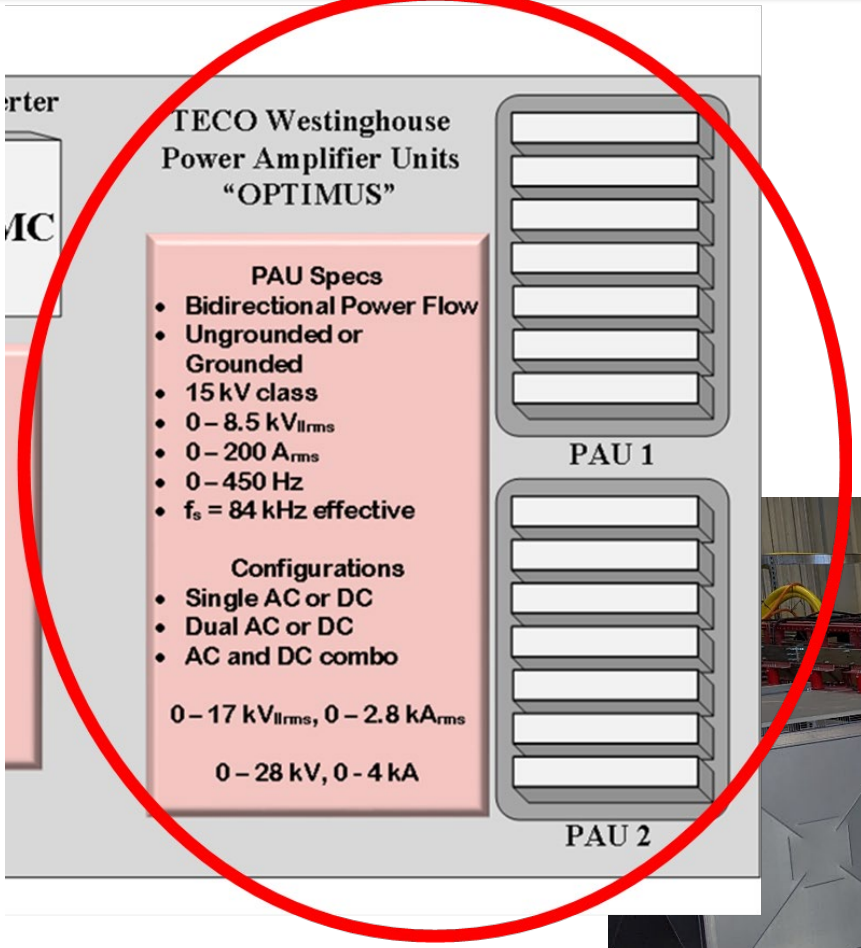
Cube Topology

Cube
In: 600V AC, 3-ph, 60 Hz
Out: 0….800 Vrms 1-ph



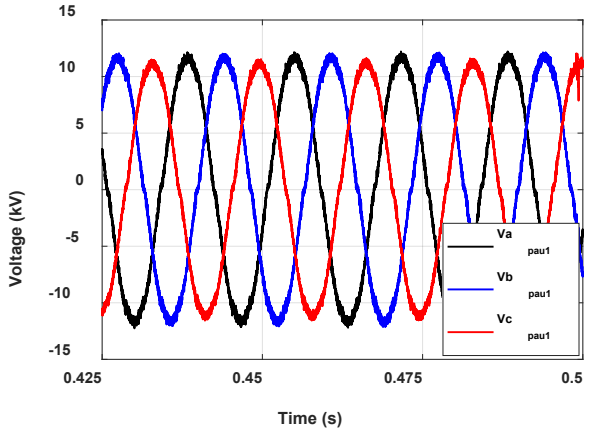
- Active Front End AFE, 4 kHz PWM carrier
- Nominal 1000 V controllable DC link
- DC link capacitance ca. 10 mF
- H-bridge switching frequency of 6 kHz per half bridge, interleaved for 12kHz effective
- PWM updated at 25kHz (from fastest control loop)
- 3-phase isolation transformer powering AFE not shown

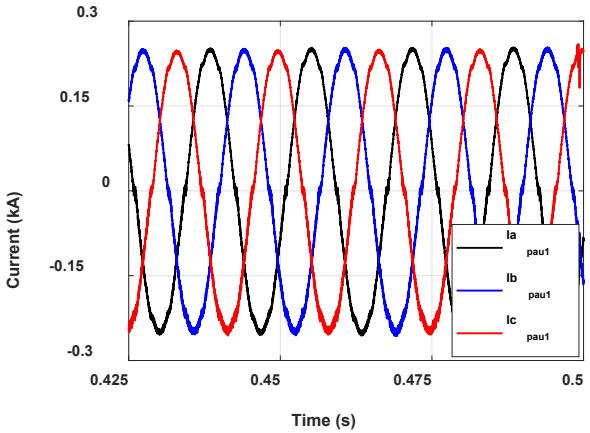
MVDC Lab – OPTIMUS Hardware

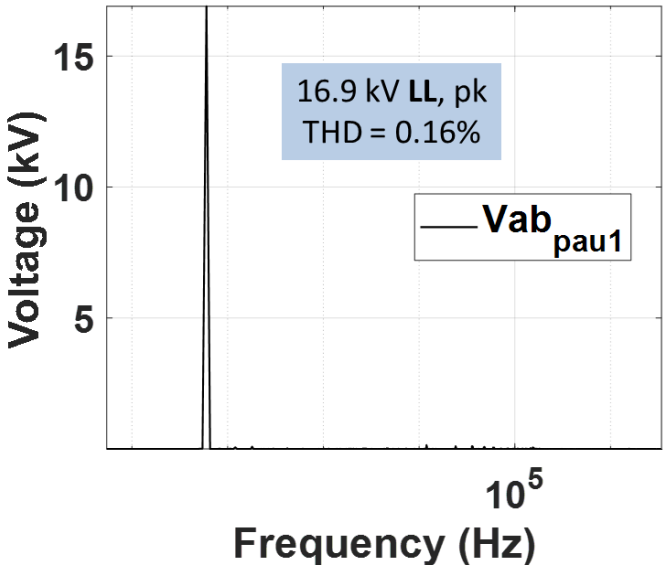


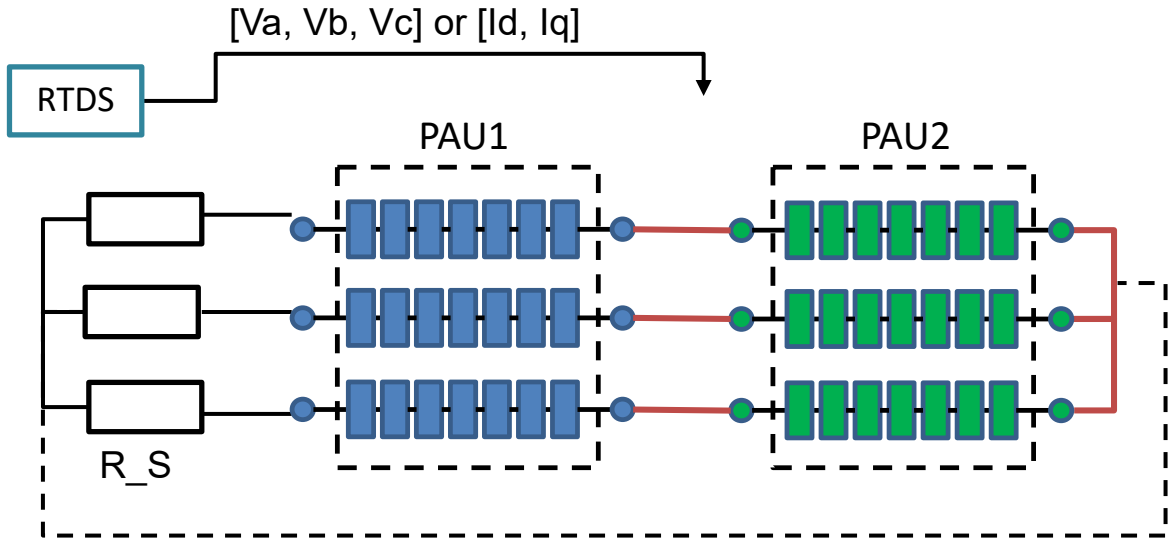
Unified PAU (14 Slices): AC1

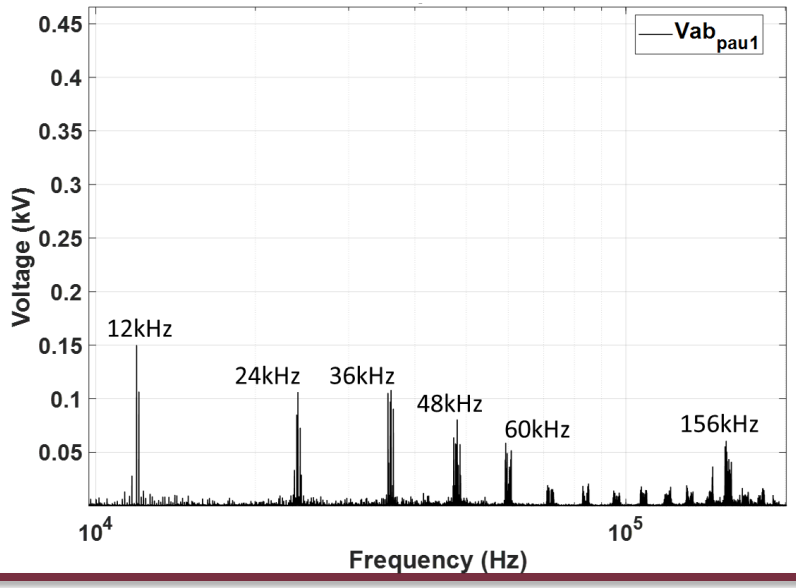
- 14 kV LN pk, 60 Hz
- 48 Ohm Load Resistor per Phase



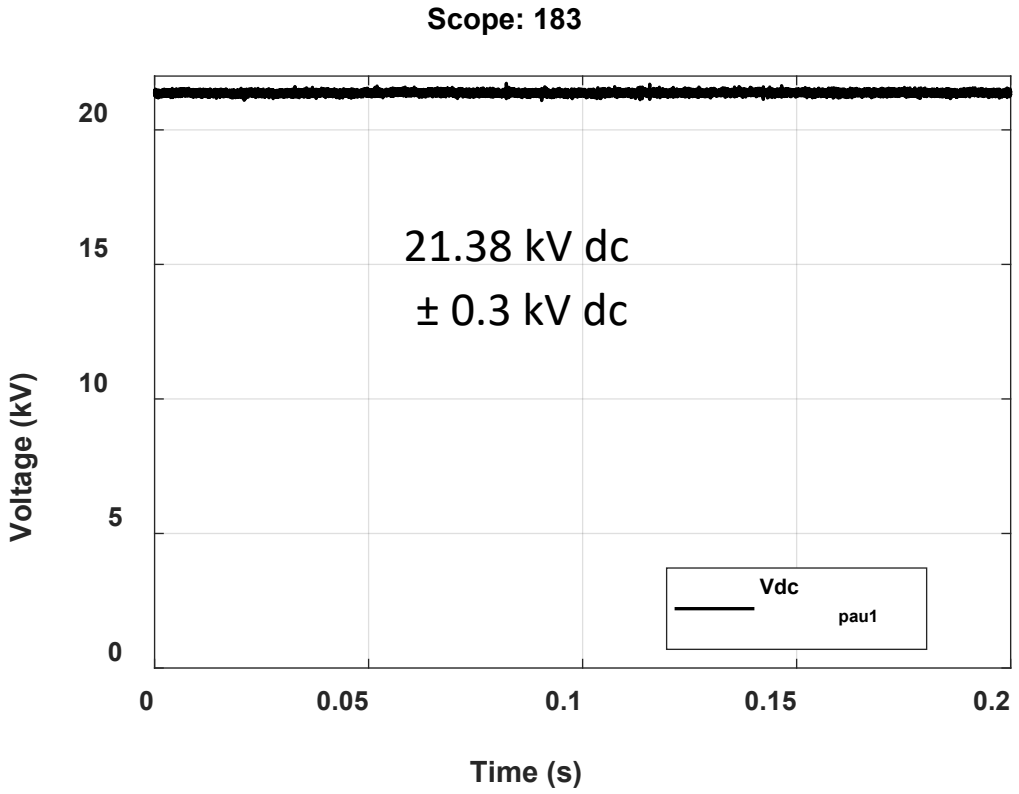




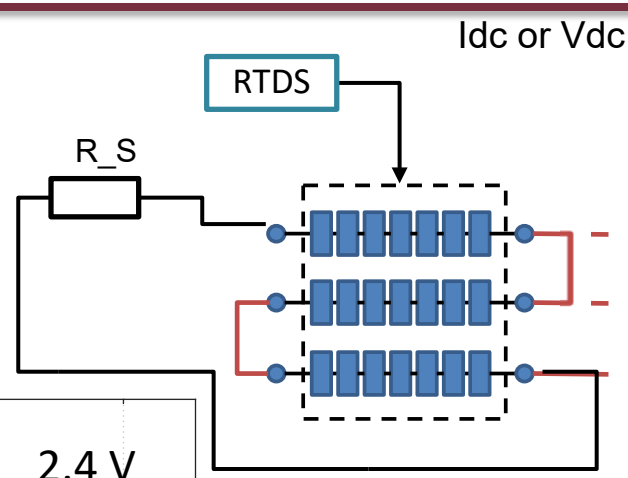


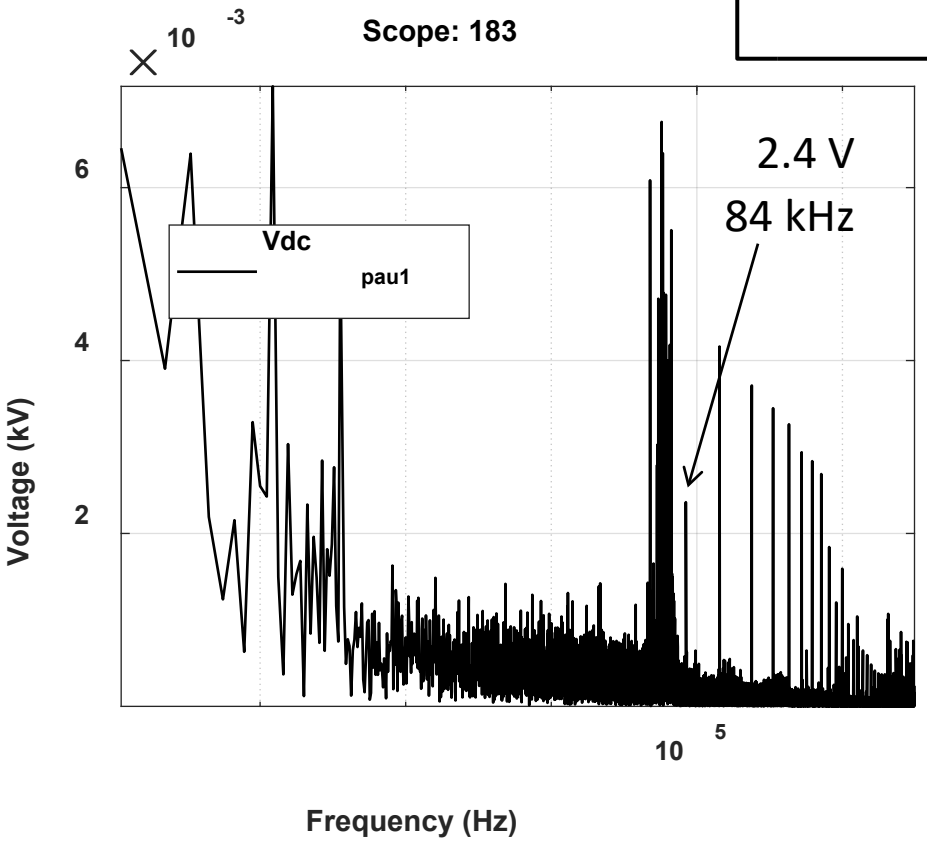


Single PAU: DC1 (21 kV request)

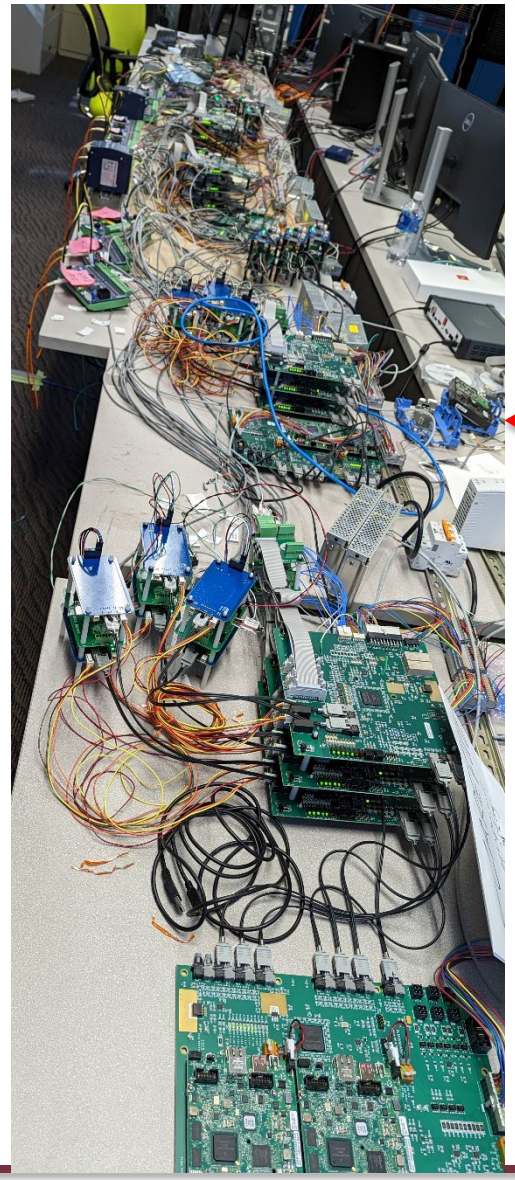


- 1 second dc pulse
- Resistor set up at 98 Ohms



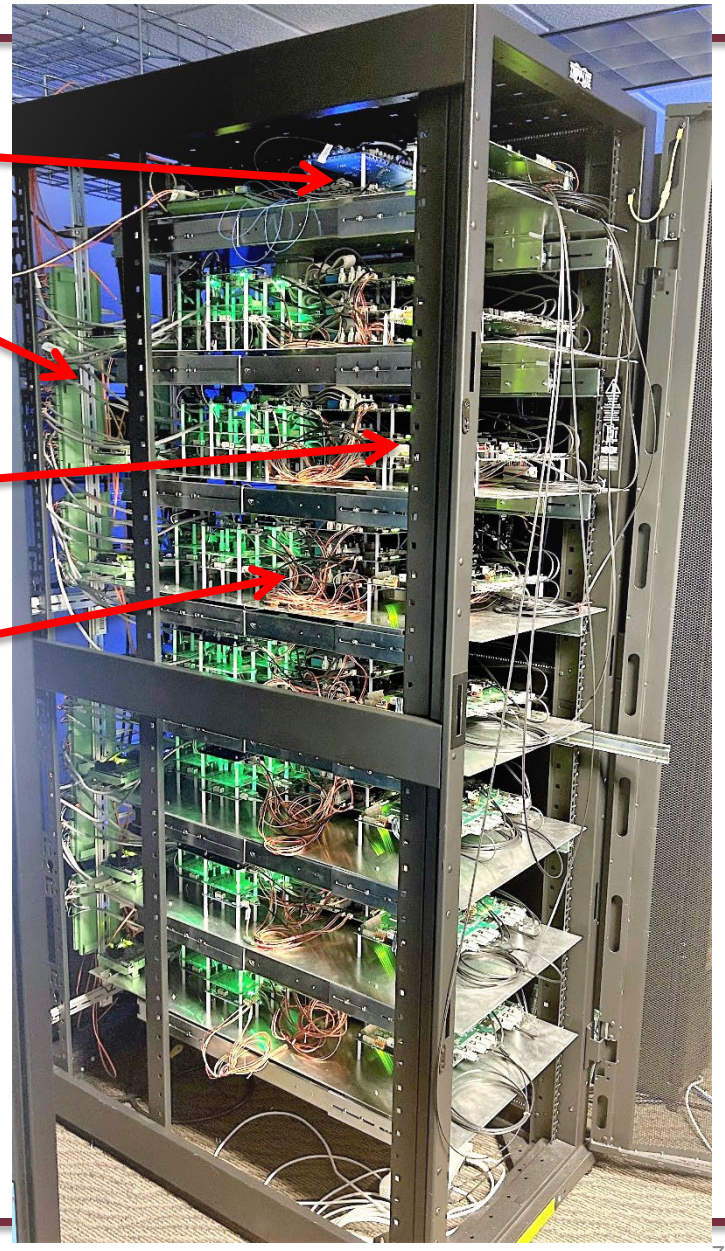


OPTIMUS CHIL Installation



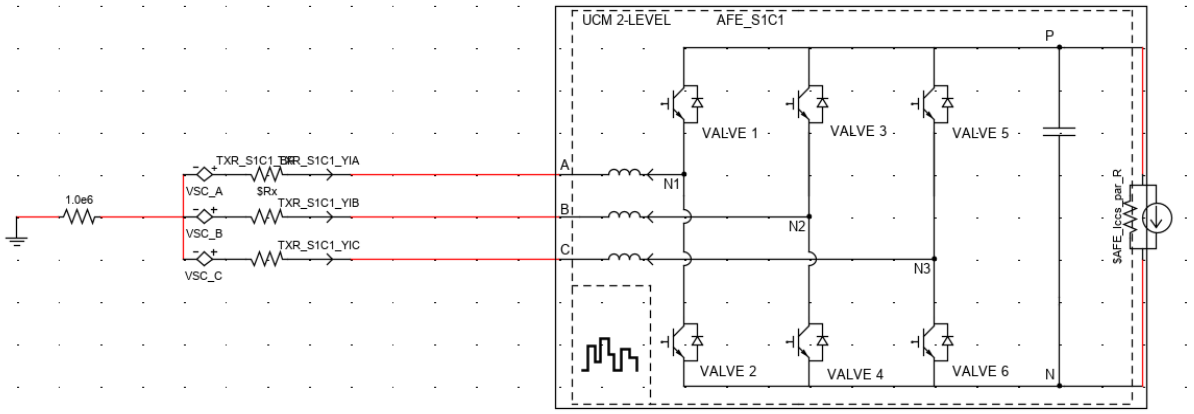
- RTDS Novacor 10 cores
- Time Step
  - Main: 60 µs
  - Substep: 7.5 µs
- 4 slice benchtop
- 7 slice tower

- Goal: 2x7 CHIL
  - Tower 1: AFE + INU modeled
  - Tower 2: INU modeled only



CHIL simulation of the PHIL amplifier is an essential tool to de-risking PHIL experiments

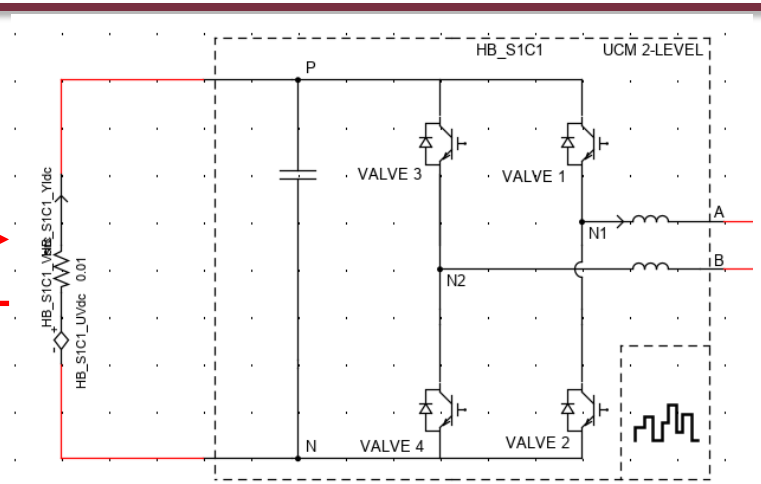
OPTIMUS CHIL RSCAD IMPLEMENTATION



AFE single cube UCM

Vdc

Idc



HB single cube UCM

CURRENT 7 SLICE CHIL MODEL:

- Currently model in RSCAD 5.014.1 (soon to be implemented/ported to RSCAD FX)
- Maximum of 2 AFEs per substep block
  - 1 GTDI for 2 AFE slices (Cubes firing pulses from controllers)
  - 1 GTAO for each AFE slice (Cubes voltage/current measurements)
- Maximum of 4 HBs per substep block
  - 1 GTDI for up to 4 HBs (Cubes firing pulses)
  - 1 GTAO for up to 4 HBs (Cubes output currents)
- 1 GTAO at the large time-step level
  - AFE input voltages and currents measurements
  - HB total output voltage and current measurements
  - HB neutral point voltages
- AFE and HB interconnected via controllable voltage/current sources

CURRENT 7 SLICE CHIL MODEL (ctd.)

- An UCM utilized per cube (3 per slice)
- The UCM provides easy interface to the TECO hardware via the UCM GTDI interface cards
- Substep containing HB slices 1 thru 4 electrically connected to substep HB with slices 5 thru 7 via substep transmission lines
- Main time-step runs at 60us and the substeps have a divisor of 9.
- All references to the hardware controllers sent digitally via optical fiber through a GTFPGA interface
- A backup of the substep I/O cards and the software PWM controls kept in a disabled hierarchy block for ease of access to switch to/from RSCAD based simulation controls and the TECO hardware controller interface.

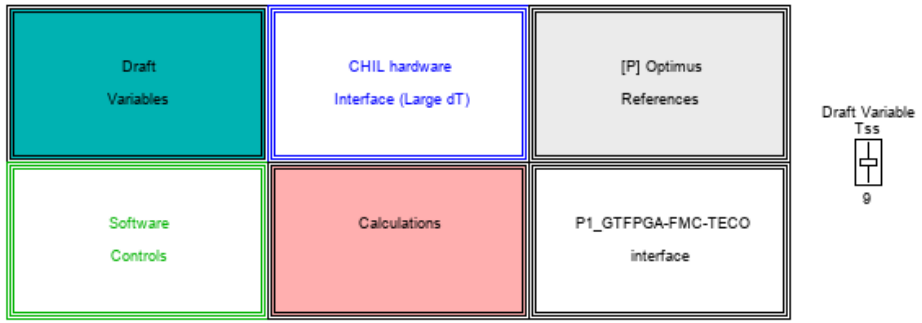
OPTIMUS CHIL RSCAD IMPLEMENTATION

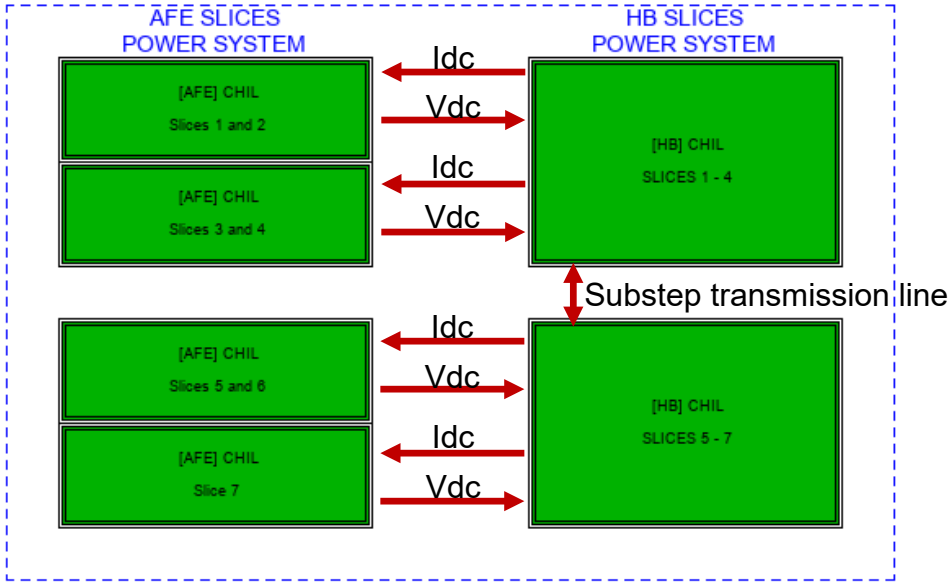
Current modeling limitations:

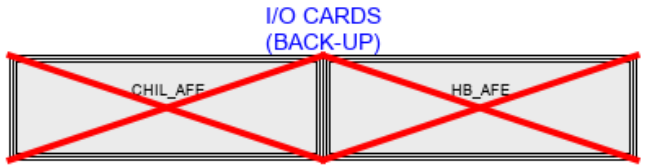
- Large time-step size at 60us due to reference signals dropping at 50us (To be corrected in future updates)
- Max of 2 slices per AFE can be modeled in a single substep block
- Max of 4 slices per HB can be modeled in a single substep block
- Time-step overflow if substep time-step below 6us (AFE)
- Max of 9 sub-step subsystems per novacor (1 core per substep block and 1 core for main step)
- Input transformer at AFE not modeled due to time-step limitations (Time-step overflow even at the allowed maximum of 10us for the substep)
- Cannot currently resolve the 84kHz effective switching frequency. At a time-step of (60us/9 = 6.667us substep) the highest possible resolvable frequency is 75kHz

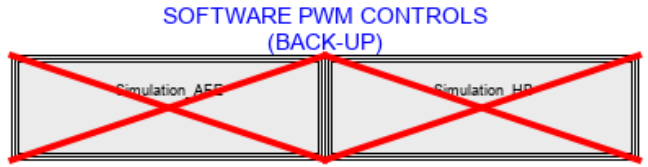
Second 7-slice model plans:

- Modeling just the HB side (No AFE needed)
- Current model has been tested without AFE with no issues.
- Expected improvements:
  - Allow for lower time-steps at the substep level by reducing the number of HB slices implemented per substep block
  - Resolve higher frequencies due to lower time-steps
  - Less hardware integration required
  - Simpler implementation than the current 7-slice CHIL

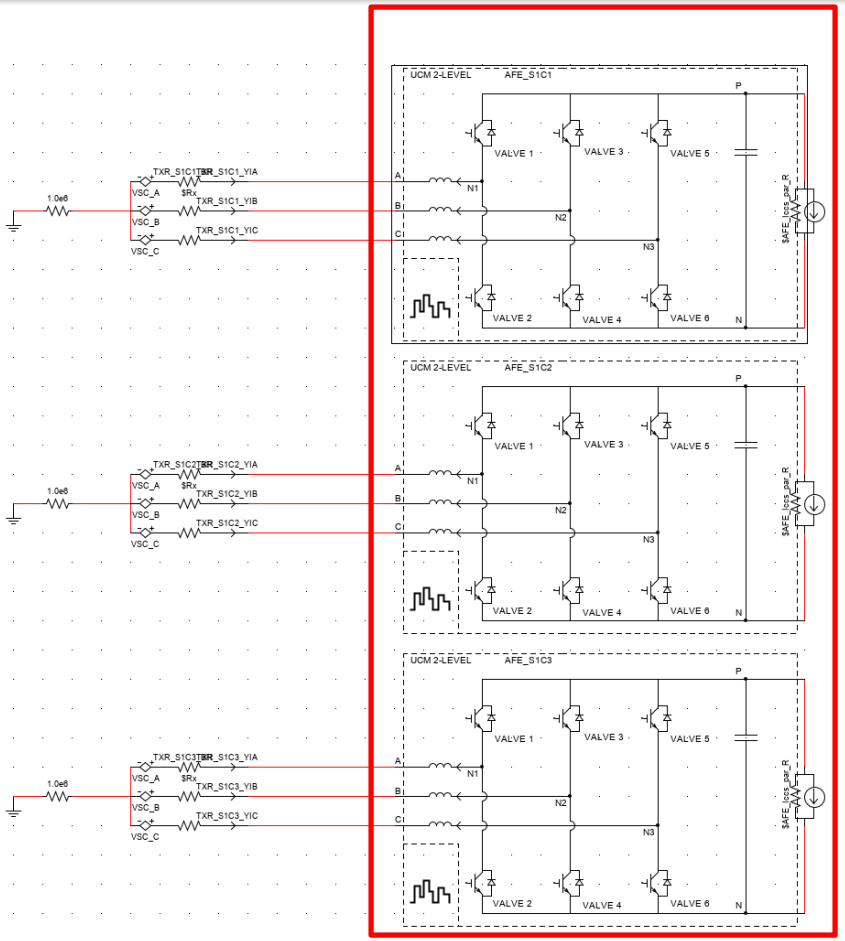






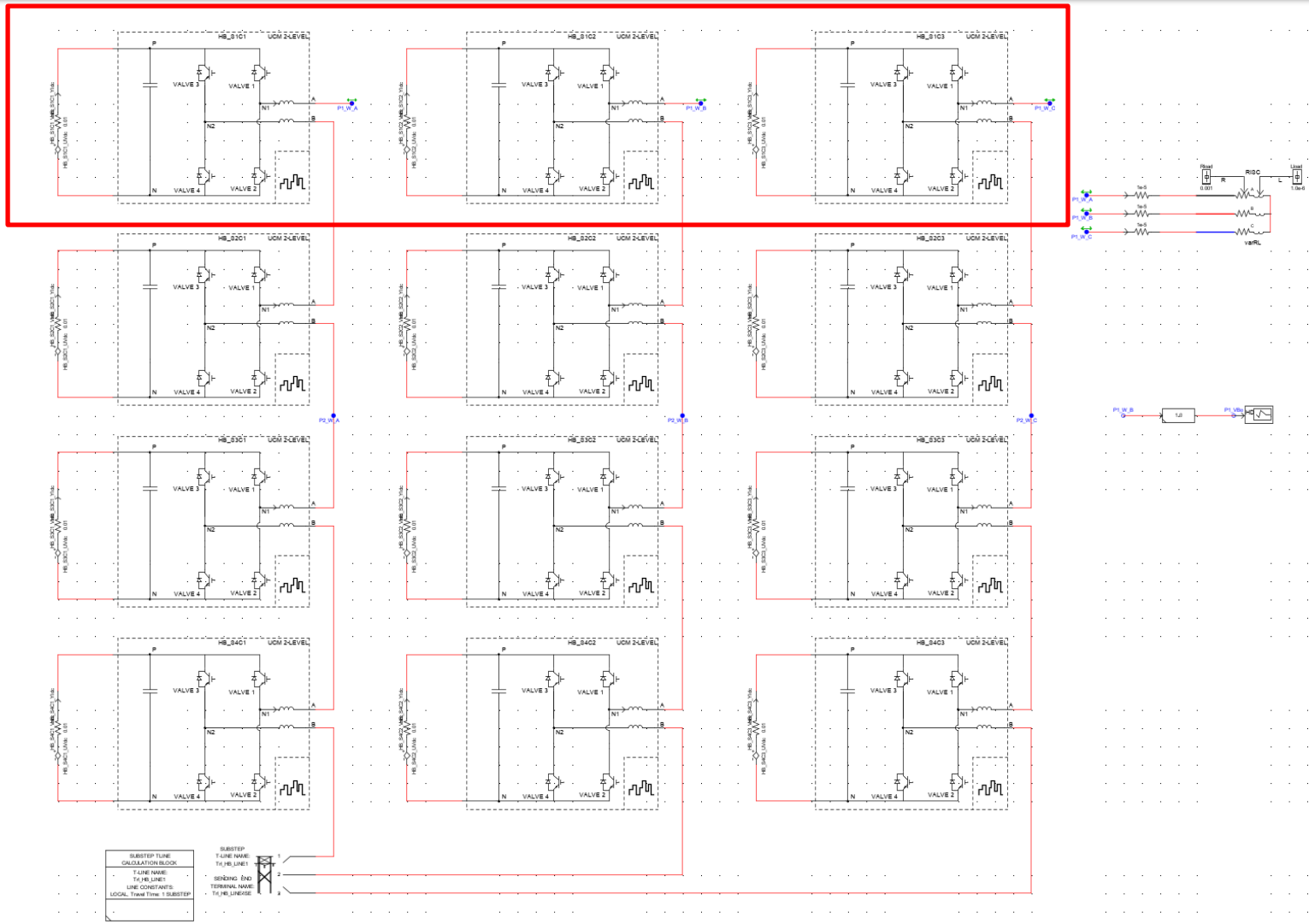


OPTIMUS CHIL RSCAD IMPLEMENTATION



AFE single slice three cubes using UCM

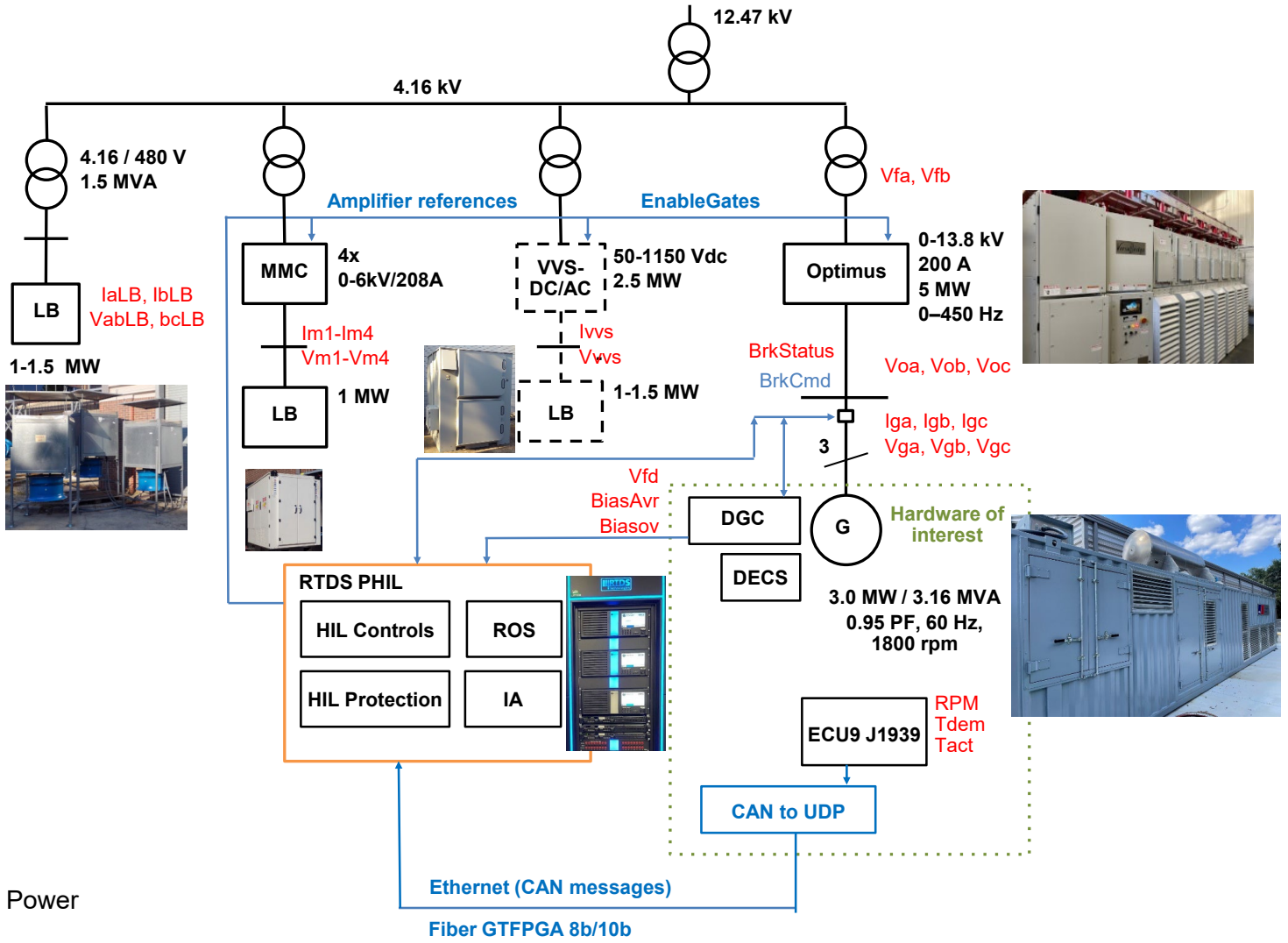
42 FPs for AFE + 28 FPs for inverter



HB Four slices three cubes each using UCM

First PHIL Application: 3 MW Diesel Gen Set Testing

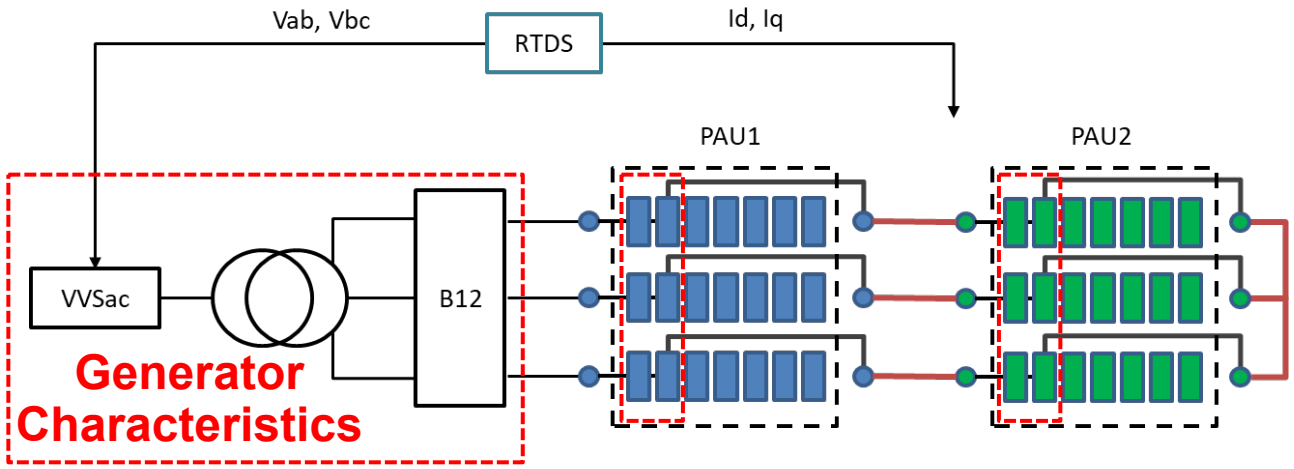
- Characterize generator behavior during <u>constant power step loads</u>
- Utilize new amplifier in current control mode
- De-risk this experiment in CHIL

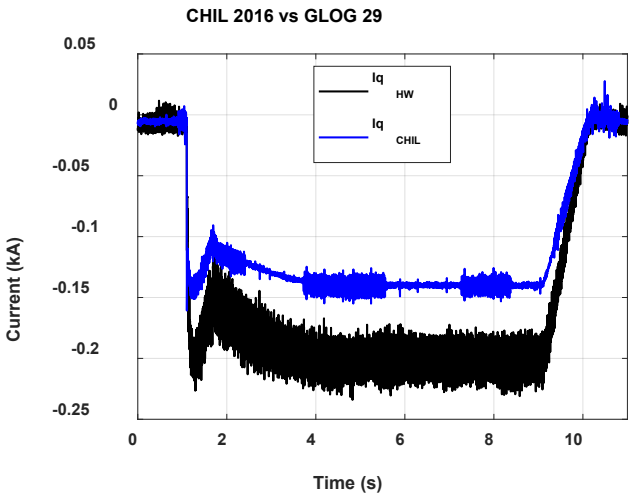


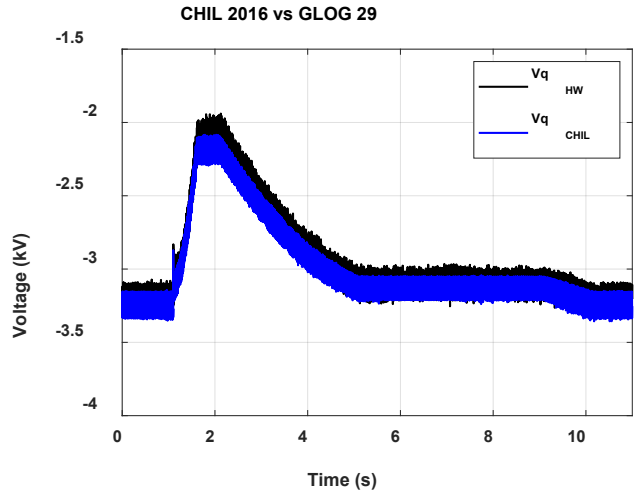
K. Schoder, et.al., “Dynamic Load Testing of a Diesel Generator Using Power Hardware-in-the-Loop Simulation”, submitted to the IEEE Electric Ship Technology Symposium, Alexandria, VA, 1-4 Aug, 2023

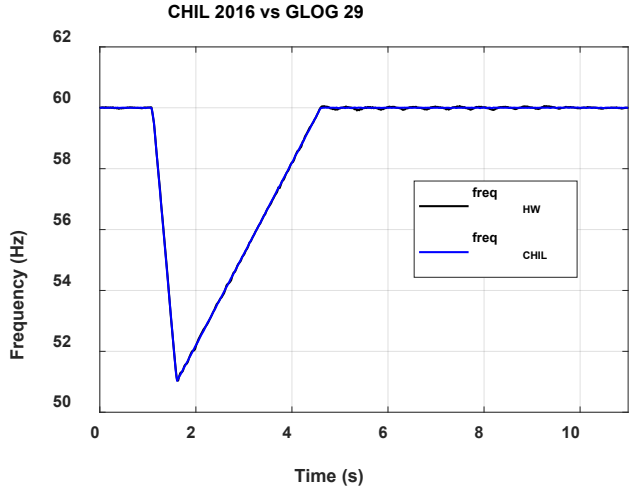
Example: Current control for generator tests

- Load acceptance
- Iq step from -5A to -138A
- VVS starts at 4 kV_LL (Vq = 3.3kVpk)
- VVS approximates expected generator response



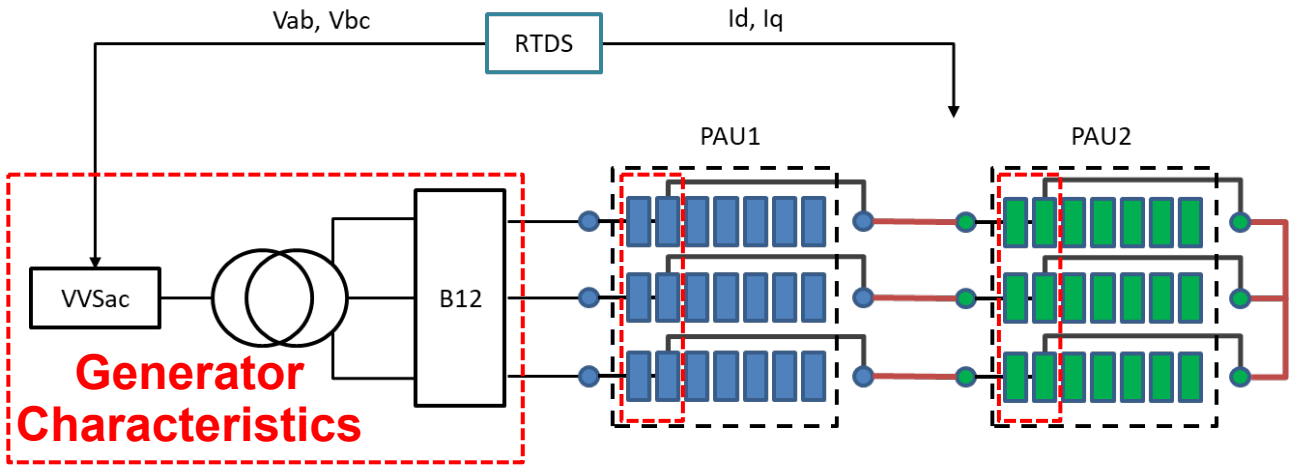


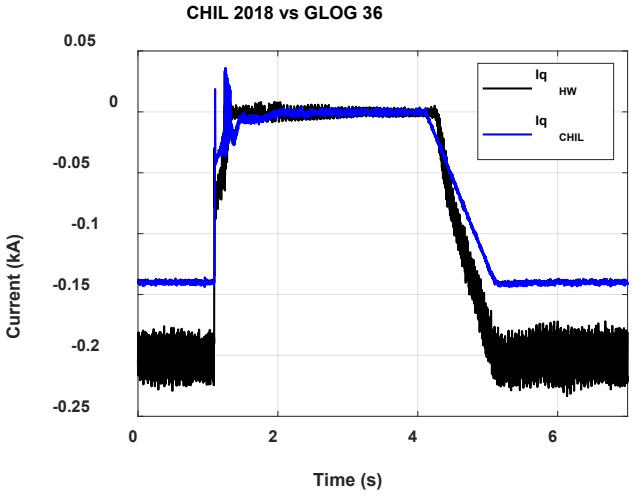


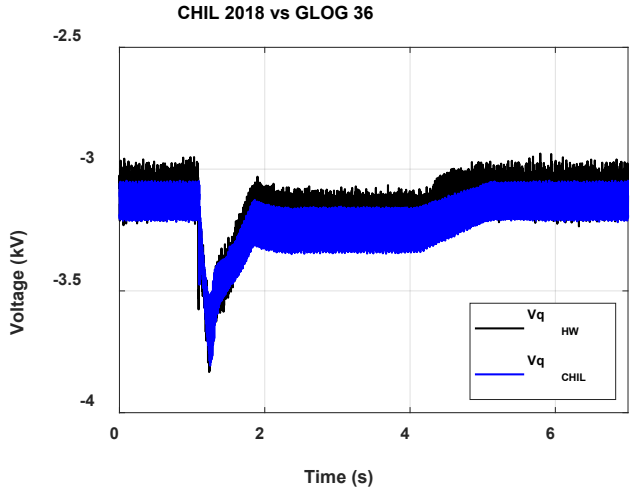


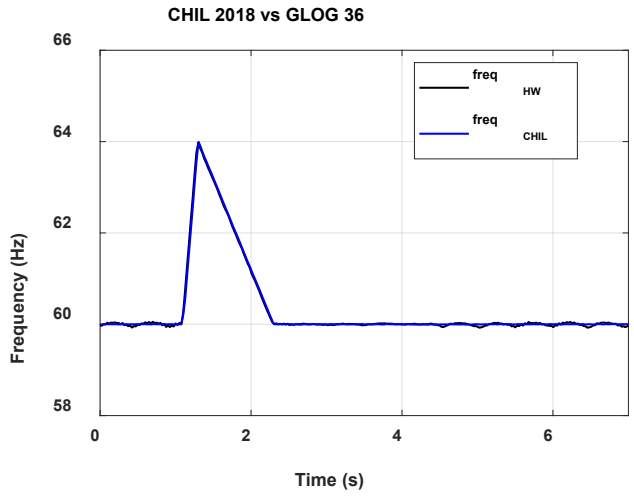
Example: Current control for generator tests

- Load rejection
- Iq step from -138A to 0 A
- VVS starts at 4 kV_LL (Vq = 3.3kVpk)
- VVS approximates expected generator response





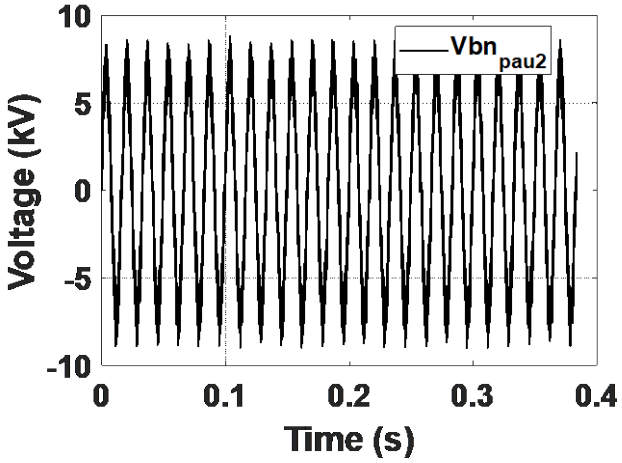




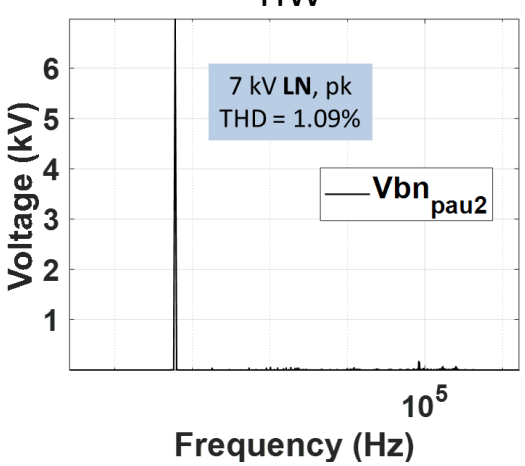
Single PAU (7 Slices): AC2

- 7 kV LN pk, 60 Hz
- 48 Ohm Load Resistor per Phase

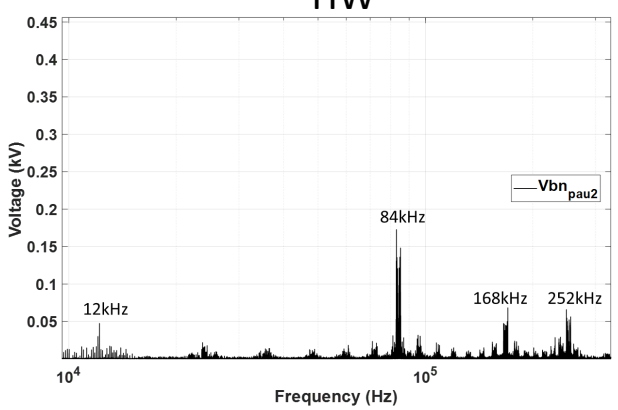
HW

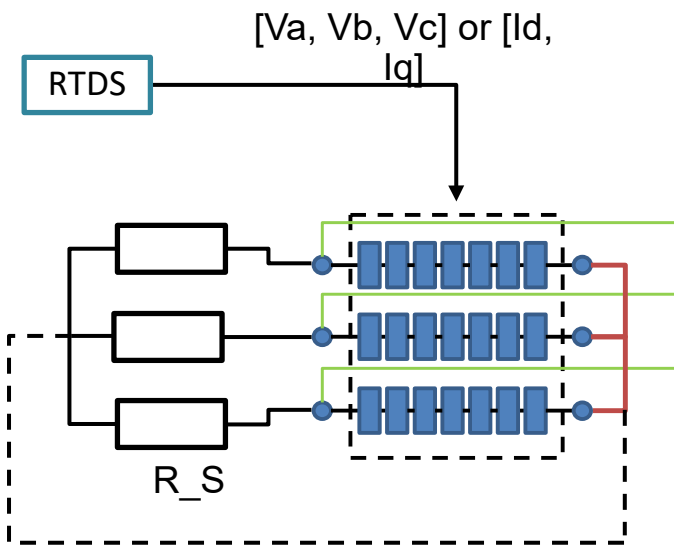


HW

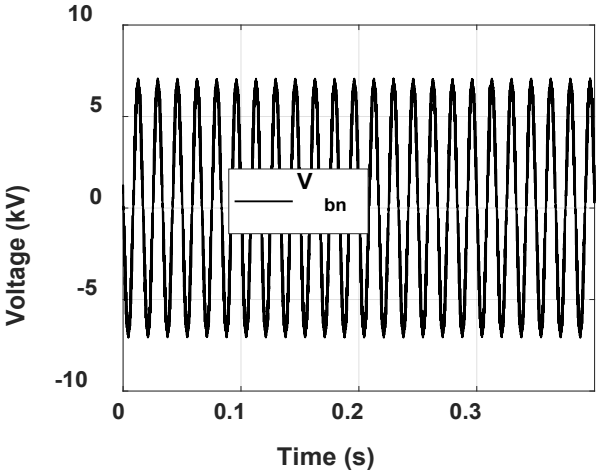


HW

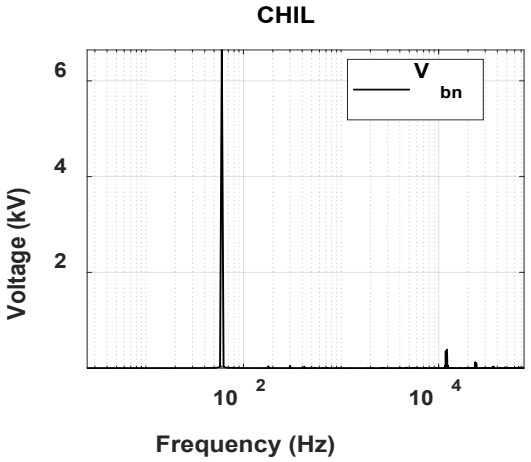




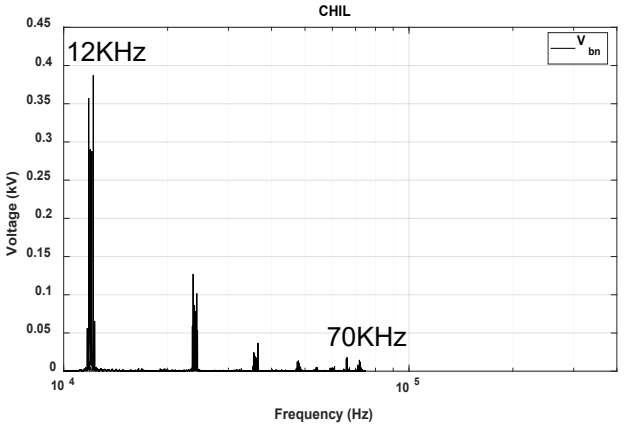
CHIL



CHIL



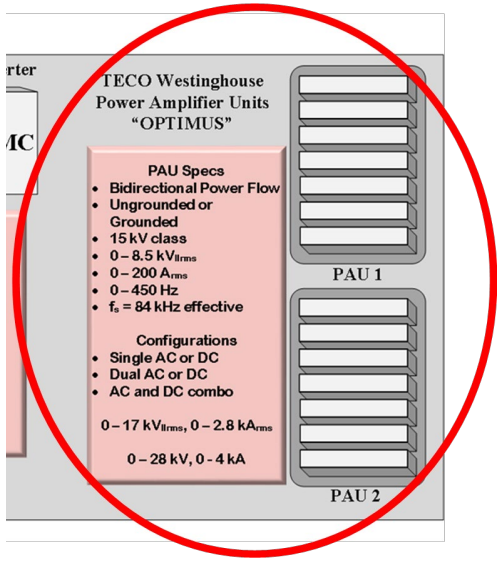
CHIL

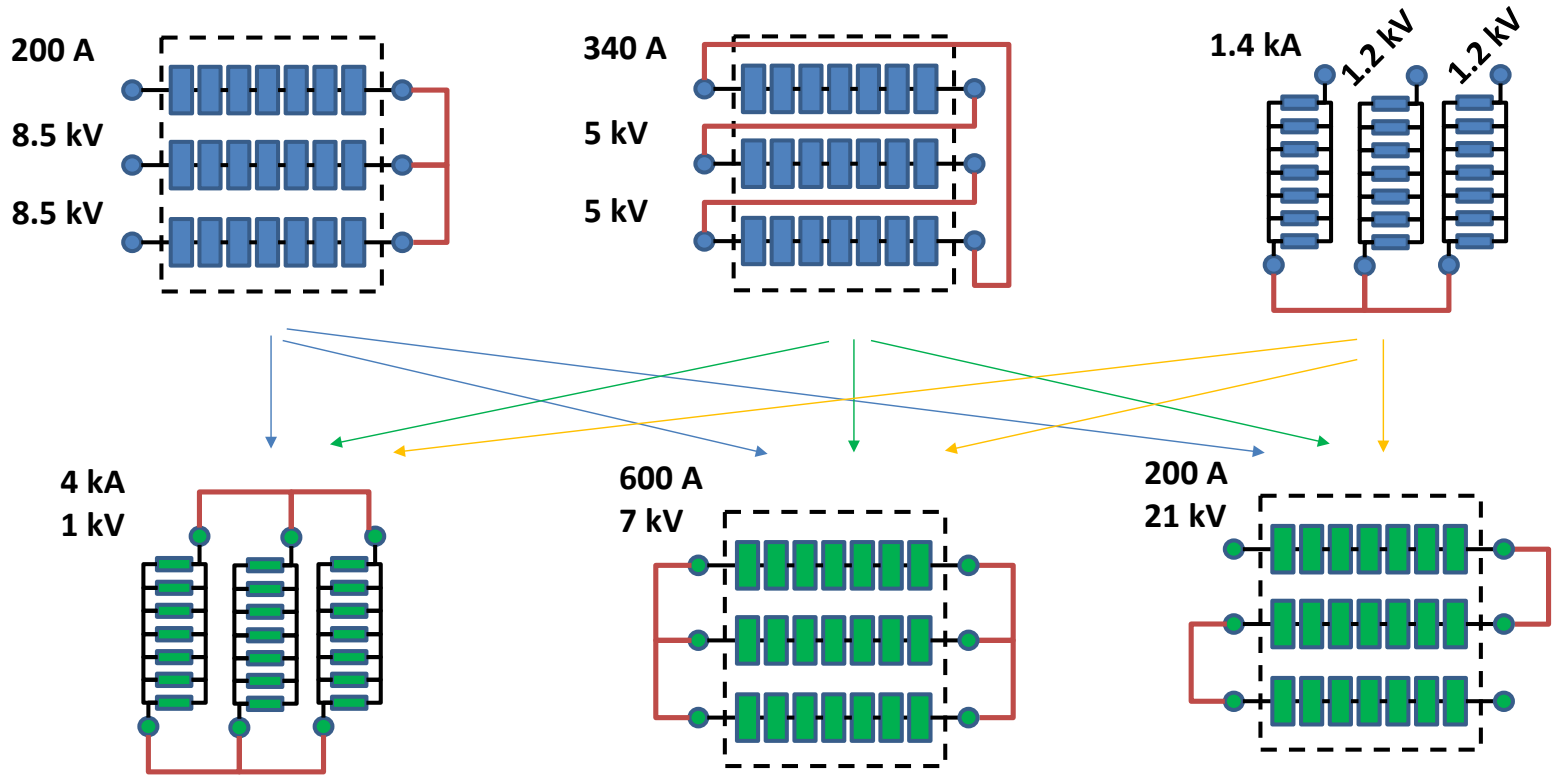


- CHIL data test conducted with newer firmware
- CHIL data resolution at 6.67us (150 kHz)

Ongoing and Future Efforts

- 7 and 14-slice CHIL build/validation
- DC current control implementation
- Validation of all control modes
- SW and HW changes to further increase bandwidth





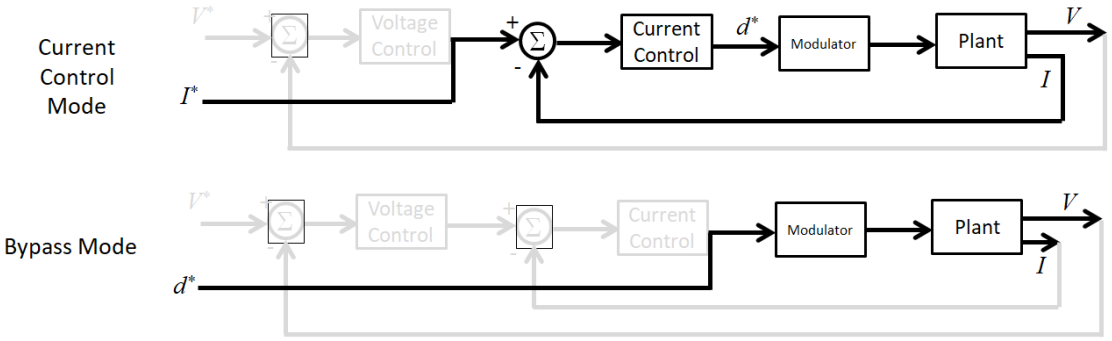
Concluding Remarks

- UCM works reasonably well for this application
- Relatively high switching frequencies of SiC converters pose an ongoing challenge to RTS
- Innovative methods to eliminate analog I/O between controllers and RTS will be advantageous
  - See CHIP plug

Backup

Control Modes of Operation

- Voltage controlled open loop 3-phase balanced
  - Uses Volts/Hz control.



- **Voltage controlled bypass mode**
  - Available and called “bypass mode”.
  - No current control loop or active balancing.

- **Current control**
  - CC11: PAU controller receives Idq_ref and θcmd from RTDS
  - CC12: PAU receives Idq_ref only from RTDS. PAU measured output voltages used for control