Hardware-in-the-loop testing of innovative under-frequency load shedding with TOR 300 device



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Project background

- Under-Frequency Load Shedding (UFLS) innovation in 2018
- NDA agreement signed between University of Ljubljana (UL) and Relematika Ltd. in 2019
- Implementation to intelligent electronic device (IED) TOR 300 EA 525
- Hardware-in-the-loop (HIL) testing with Real-Time Digital Simulator (RTDS)





UFLS basics







Frequency-stability margin







Definition of f-M zones



Frequency-stability margin M(t)





Implementation logic



Innovative UFLS





Hardware-in-the-loop setup



RTDS Simulator

IED TOR 300 EA 525





Software replica UFLS







Power system 1 – IEEE 9 bus system





IEEE

Power system 2 – Microgrid





Ε









• Conventional UFLS scheme

- Innovative UFLS scheme
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- Time delay introduced for the duration of $M_{\rm thr}$ violation affects the operation of the UFLS function
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Project outcomes and conclusions

- Frequency-stability margin M(t) was successfully merged with frequency measurement f(t), improving the existing situational awareness of an IED.
- The existing IED single-criterion tripping functionality was successfully expanded into a double-criteria tripping functionality.
- In an IEEE 9-bus test system model, the innovative UFLS functionality keeps more load supplied compared with the conventional UFLS.
- In high RoCoF(t) conditions, innovative UFLS acts identically to conventional UFLS, posing no risk to power-system security under extreme conditions.





Future plans

- Modelling and testing on other EPSs
- Upgrading the innovative UFLS technology frequency thresholds f_{thr} dependent on M(t)
- Implementation of frequency-stability margin *M(t)* in WAMS



