FULLY DIGITAL REAL–TIME ELECTROMAGNETIC TRANSIENTS SIMULATOR

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ABSTRACT

The paper details the design, architectural features and application of a fully digital electromagnetic transients simulator capable of real–time operation. The custom hardware and software developed to implement the Real–Time Digital Simulator (RTDS) is described with special emphasis given to the high level graphical user interface written especially for use with the RTDS.

INTRODUCTION

Simulation is one of the most powerful tools available to the power systems engineer when confronted with the need to study complex power system phenomena. With the general accessibility of main frame computers and the emergence of the EMTP in the 1970's, power system engineers could gain access to the simulation software with relative ease.

One of the limitations with digital computer based simulation programs, such as EMTP, is that a single run can take many minutes or even hours to compute the modelled system's response over a period of one second. Such non real–time operation precludes interfacing the simulator to physical control or protection devices. Generally, testing of physical control and protection devices is done using an analogue simulator or a special device which plays back, in real–time, the stored results of an off–line computer simulation to the device under test.

One drawback of the analogue simulator is its high capital and operating costs. Furthermore, general accessibility is low since a single study may occupy the analogue simulator for many weeks. With the play back device, major drawbacks include the long time required to obtain the simulated results and the fact that only open loop testing is possible.

The primary advantages of a fully digital simulator capable of real–time operation are that it incorporates the best features of both the computer based digital simulation tool and the analogue simulator.

THE RTDS: AN OVERVIEW

The impetus for the development of the RTDS came from the fact that as a research oriented institution the Manitoba HVDC Research Centre needed a simulation tool which could be used to study power systems which included HVDC valve groups and their controls and which could quickly be set up to simulate different power system models. The development of the RTDS has been ongoing for some four years. A prototype simulator has been in operation for almost two years and a commercial version, incorporating many improvements over the prototype, is currently under construction for delivery to two Canadian utilities.

There are a number of important features which characterize the RTDS. Firstly, it is comprised of custom made hardware as opposed to commercially available off–the–shelf processor boards. Secondly, special parallel processing techniques have been used to allow the RTDS to be expandable to simulate even very large power system models using time–steps on the order of 50μs. Finally, the software used to model the power system components is based on the standard techniques used in modern digital electromagnetic transients programs such as EMTP and EMTDC [1,2].

In order to provide an environment where the user could focus on the simulation study at hand and not on the intricacies of running the simulator, substantial effort was put into the development of a graphical user interface. The user interface, known as PS–CAD, includes software modules which allow the user to efficiently layout the power system model, perform the simulation and analyze the results.

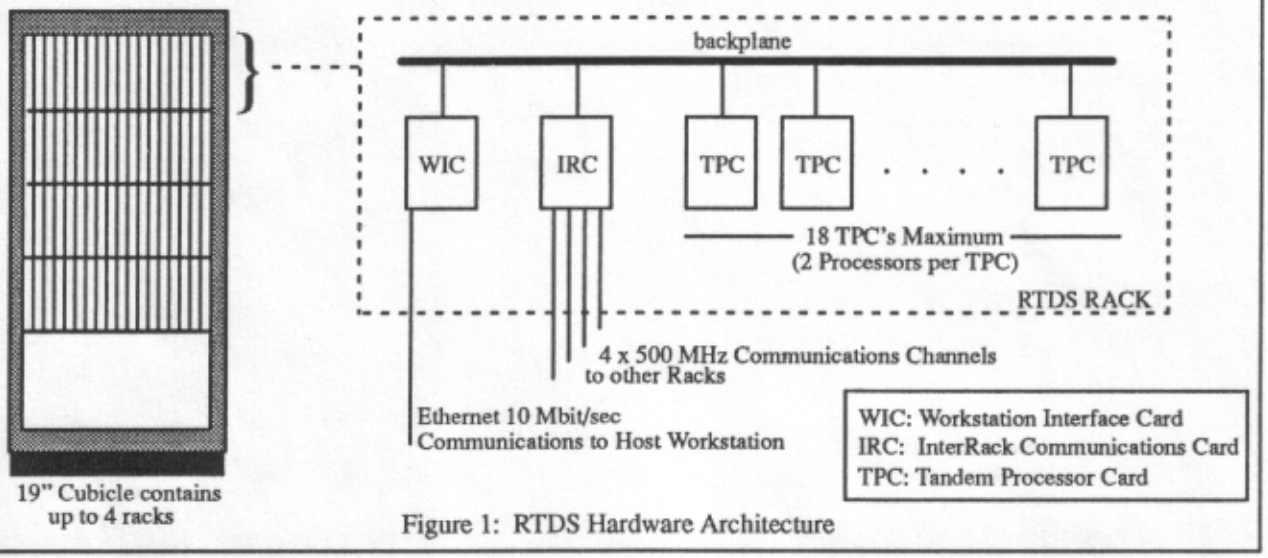


Figure 1: RTDS Hardware Architecture

THE RTDS: HARDWARE ARCHITECTURE

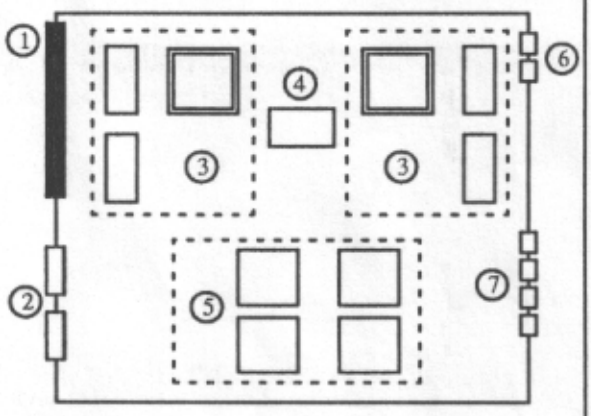
After careful study of the Dommel algorithm [1] for the solution of power system components and the diakoptic splitting of the power system network into subsystems [2] it was determined that a suitable hardware architecture for the RTDS should be one that mimicked the power system itself.

The RTDS hardware is organized into racks of tightly coupled processors which are in turn loosely coupled to other such racks. The term tightly coupled refers here to the fact that the processors within a single rack are connected to a common backplane. Individual racks may only be directly connected to four other racks. Figure 1 illustrates the rack components and interconnections.

Each rack is identical and consists of only three distinct types of printed circuit boards.

TPC: Tandem Processor Card

Each TPC contains two digital signal processors which have a combined computing speed of some 44 MFLOPs (Millions of Floating Point Operations per second). It is important to note that each TPC is identical and it is software which determines the card's function during a simulation run. The main functional blocks found on the TPC are shown in Figure 2.



1) Backplane Interface
2) Digital I/O & Analogue Input
3) Digital Signal Processor c/w Program & Data Memory
4) Dual Ported Memory
5) Custom VLSI to handle decoding and timing
6) Status LEDs
7) Analogue Output Channels

Figure 2: TPC Major Component Blocks

Depending upon the type of function allocated to the TPC, its two processors may operate independently or in unison so as to provide the processing power necessary to model complex power system components. Dual ported memory is provided to allow fast communications between the TPC's two processors without having to access the backplane.

Each TPC is provided with digital and analogue I/O channels. These can be used to interface the power system components modelled on the RTDS to external devices. For example, the firing pulses which trigger thyristors within a HVDC valve group can be provided by a physical control set and sent into the valve group model via a digital input port. Feedback quantities such as the commutating bus voltages can be provided back to the controls through the analogue output channels. An individual processor on a TPC has direct access to the following I/O ports.

- Four scalable analogue output channels
- One analogue input channel (12 bit res.)
- One 16 bit digital input channel
- One 16 bit digital output channel

The actual function allocated to an I/O channel will vary with the type of model which is assigned to the processor.

Data may be communicated to and from a processor's external memory during a simulation case. It is thus possible to interact with the simulator from a host computer workstation while it is performing a simulation.

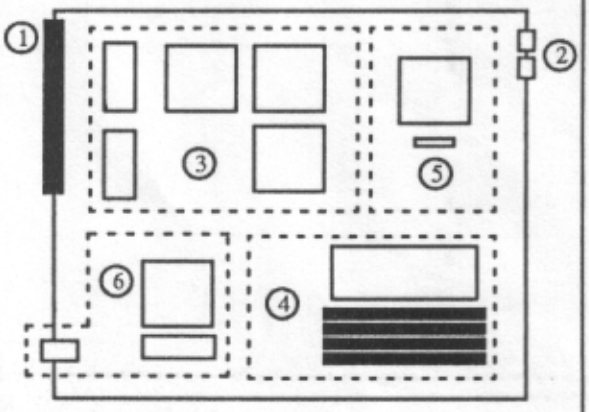
WIC: Workstation Interface Card

A single WIC resides on each rack of RTDS hardware. Its main function is to regulate communications between the RTDS and the host workstation, as well as to handle communication requests from the processors connected to the rack backplane. Figure 3 shows the WIC major function blocks.

Communication between the WIC and the host computer workstation is done via a standard ethernet based local area network (LAN). Each rack is assigned its own unique ethernet address and resides on the LAN as would any computer. The WIC's ethernet controller is able to decipher data packets meant for it and respond back to the originating workstation. One of the M68020 processor's tasks is to redirect data communication from the host to the appropriate processor residing on a TPC. The M68020 is also responsible to handle diagnostic testing for the entire rack. The M68020 does not actively participate in a simulation run except to pass data between the host workstation and the processors within its rack.

All data communications between processors over the rack's backplane are handled from specialized hardware residing on the WIC. Each digital signal processor is able to signal the WIC when it is ready to pass and receive data. All of the timing associated with passing of data during a simulation is predetermined by software before the case is actually run.

The time–step with which a simulation is performed is defined by the user. Off–line software determines whether or not the RTDS will be able to simulate the user defined power system model with the chosen time–step. The software also can be made to choose the minimum time–step with which real–time can be maintained for that case.

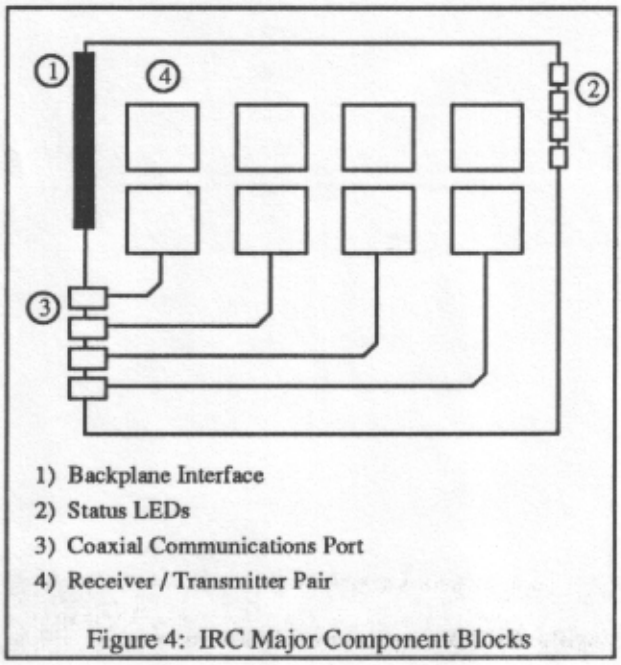


1) Backplane Interface
2) Status LEDs
3) Custom VLSI to handle backplane communications
4) M68020 Based Minimal Computer
5) Simulation time–step clock
6) Ethernet LAN port and controller

Figure 3: WIC Major Component Blocks

IRC: Inter–Rack Communications Card

Communications between racks is handled exclusively by the IRC. Each IRC provides communication paths to four other racks. Figure 4 illustrates the major component blocks found on the IRC.



1) Backplane Interface
2) Status LEDs
3) Coaxial Communications Port
4) Receiver / Transmitter Pair

Figure 4: IRC Major Component Blocks

Data communicated between racks is done over single coaxial conductors so as to reduce the wiring congestion. Full 32 bit data is converted to serial form and transmitted at 500 MHz. Error detection bits are automatically added and stripped from the bit stream by the receiver and transmitter pair hardware. Since it is only possible to directly interconnect one rack to four others, simulators comprised of more than five racks will not have every rack connected to every other rack. A map of the physical connection paths between racks is stored in a file on the host workstation. Software accesses this file to determine how the available RTDS hardware will be allocated to the user defined power system model.

An inter–rack communications link between two racks can handle many parallel transmission line connections between the subsystems modelled on those racks.

THE RTDS: SOFTWARE ASPECTS

A hierarchy of software was written specifically for use with the RTDS. Each level of software is accessible only from the one immediately above, with the highest level of software being the one with which the user directly interacts.

Component Models

The lowest level of software comprise the modules which are used to model the power system components. Since these software modules directly influence the time–step with which a particular system model may run, they are written using low level machine language code. All of the code used in conjunction with the component models is hand assembled and optimized. The following component models are currently available for use on the RTDS.

- Passive R–L–C branches, filters and sources
- Single and twin circuit transmission lines
- 2 & 3 winding transformers c/w saturation
- Breakers & fault switches
- Synchronous machine c/w
  Exciter, governor, turbine and multi–mass
- Series capacitor c/w MOV and bypass switch
- HVDC valve group (6P or 12P Graetz bridge)
- CT, CVT & PT models.

The user is able to interconnect these components to form the power system model required to perform a specific study.

Algorithms used to model the individual components, as well as the overall network solution are based upon the same mathematical foundations as those used in the EMTP and EMTDC. In particular, the network solution is based on the well known Dommel algorithm.

The RTDS Compiler

A compiler has been written which takes as input the power system layout as entered by the user, including the data associated with the power system components and the RTDS hardware configuration map. As output, the compiler produces all of the parallel processing code required by the digital signal processors, as well as the memory allocation and data communication schedules. In order to generate the executable code, the compiler accesses a library which contains the code for the component models.

A number of files are produced by the compiler which are used by higher level software in order

to determine when and where to access specific data while the simulation is in progress. A user readable file is also produced which specifies how the various digital and analogue I/O channels are allocated. For example, this file might contain information which indicates that analogue output channel #2 on card 5, rack 3 displays a particular node voltage.

One of the compiler's ancillary tasks is to determine whether the time–step requested by the user is sufficiently long to permit continuous real–time operation. At the end of the compiling procedure the minimum allowable time–step for the particular system model is displayed. It is possible for the user to run a case with a time–step smaller than that which limits real–time operation. The only drawback being that it is no longer possible to interface external devices to the RTDS.

Allocation of the available RTDS hardware to the user defined power system is done by using a number of rules. The most important aspect of the allocation is to recognize that travelling wave based transmission line models split the nodal admittance matrix into block diagonal form. The portions of a power system isolated from each other by transmission lines and represented by a unique block in the system matrix are referred to as *subsystems*. Each subsystem is usually allocated one single rack of hardware. Figure 5 shows how a simple network could be allocated to three racks of RTDS hardware. In order to make most efficient use of the available RTDS hardware it is possible that a single rack is allocated to model more than one subsystem. The circuit of Figure 5, for instance, could easily be modelled using only a single rack of hardware.

Not only is it possible to use transmission line models to split the power system network into subsystems, but valve group models also perform the same function. Thus, if the user's model includes HVDC valve groups, the AC and DC systems could be defined as separate subsystems.

The WIC Multi–Tasking Operating System

A real–time, multi–tasking operating system was developed for the M68020 processor which resides on the WIC. Its major functions are to handle data I/O requests which are usually initiated by the user or software running on the host workstation. A detected error in transmission of data across racks will be flagged and noted by the operating system and will force the simulation in progress to stop.

The operating system software essentially provides low level services for higher level software such as the graphical user interface. It is possible for the system administrator to request that a set of diagnostic tests be run from the WIC card. All detected errors are returned and the operator is advised as to which card within the rack is the likely cause. Since a medium to large size simulator may contain some 360 individual processors, diagnostics become a very important tool in the efficient day to day operation of the simulator.

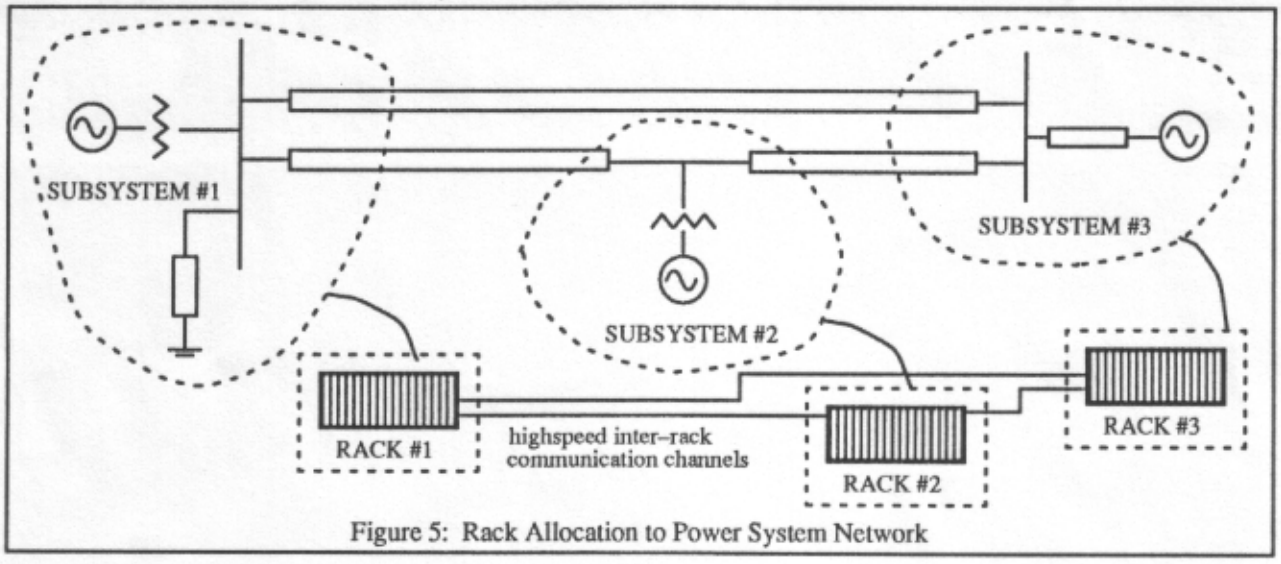


Figure 5: Rack Allocation to Power System Network

The Graphical User Interface Software (PS–CAD)

PS–CAD is a family of graphics based software modules which allows the user to perform all of the tasks necessary to simulate a power system using the RTDS. Figure 6 shows the various PS–CAD software modules and their relationship to each other. The software modules were written specifically to run on computer workstations which include a Unix O/S with a X11 based window manager and an ethernet LAN port. Most of the commonly available computer workstations adhere to these standards.

It should be noted that the PS–CAD software functions as the graphical user interface for both the RTDS, as well as the EMTDC transients simulation software. The user may select which simulation tool is to be used to perform the actual simulation of the power system model.

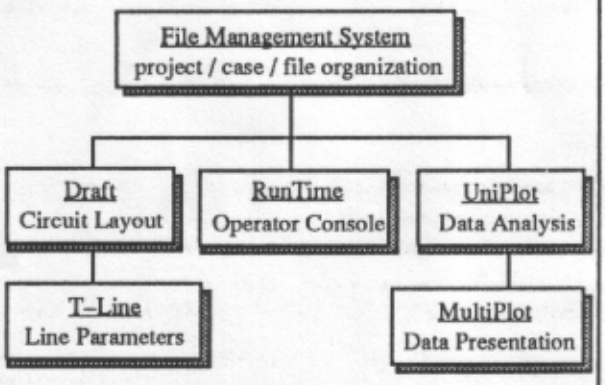


Figure 6: PS–CAD Software Modules

The fundamental steps that the user must perform in order to simulate a new power system model are as follows.

- Define a new Project and/or Case within the FILEMANAGER module.
- Layout the power system model using the DRAFT module.
- Perform the simulation by compiling, loading and running the case from the RUNTIME module.
- Analyze the results using the UNIPLOT module.

PS–CAD: FILEMANAGER

The FILEMANAGER PS–CAD module allows the user to maintain a database of simulation cases. It is also possible for various users of the RTDS to share their simulation databases. It is very easy for a user to accumulate a great number of cases occupying significant storage space on the host workstation's disk drive. To this end convenient backup and restore features have been included as part of the FILEMANAGER. The user is able to quickly backup or restore selected project database entries or just individual cases.

Once the user has created a new database entry or entered an existing entry any of the other PS–CAD modules can be started by selecting their corresponding icon.

PS–CAD: DRAFT

From within the DRAFT module the user is able to sketch a layout of the desired power system and to enter the parameters associated with the system components. Figure 7a shows a screen dump of the DRAFT software. The right hand side of the screen, referred to as the palette, contains icons of the available power system components. The user selects the desired component and copies it to the left hand side of the screen, known as the canvas. Buswork icons are available to interconnect the individual components so as to form the desired power system model. When the EDIT option associated with a particular component icon is selected, a window appears into which the user enters the various parameters required by the component. Figure 7b shows one of the EDIT windows associated with the synchronous machine model.

It is possible to load numerous specialty libraries into the palette area. For example, the machines library includes a wide range of machine sizes and types. The machines include matching exciters and governors with typical data already entered.

Once the user has completed the circuit layout and parameter entry, the COMPILE option will generate a data file which contains the data necessary for the RTDS compiler (or EMTDC).

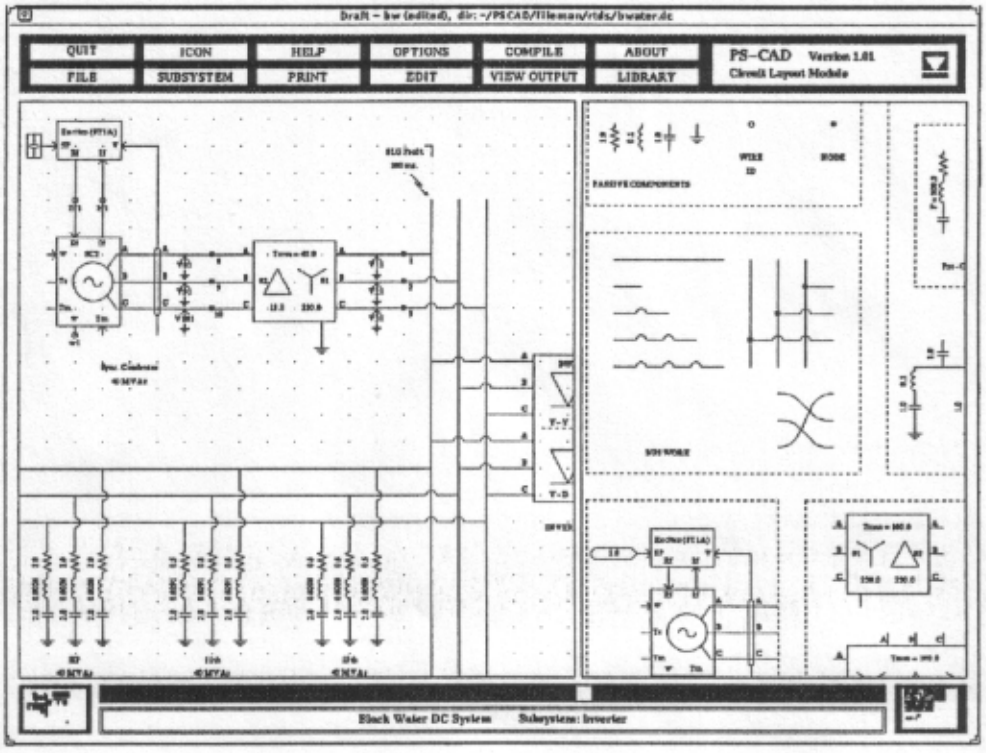


Figure 7a: Screen Dump of DRAFT Window

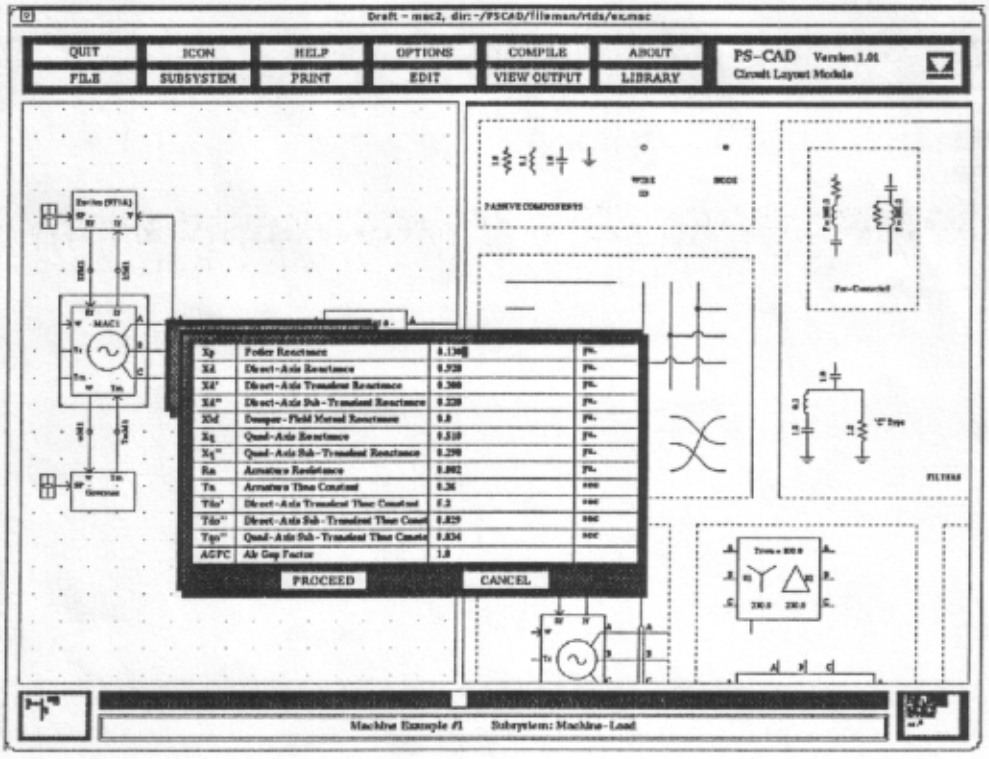


Figure 7b: Synchronous Machine Model Parameter Window

PS–CAD: T-LINE

A special software module exists to allow users to enter transmission line data. By defining the geometry and type of the conductors and ground wires, the software is able to perform eigenvalue analysis in order to compute the line's modal transformation matrices. The line's modal surge impedances and travel times are also computed. This data is required by the RTDS compiler.

As an added feature, the T-LINE package will also compute and plot the magnetic field, ground gradient, radio interference and audible noise associated with the user defined transmission line.

PS–CAD: RUNTIME

The PS–CAD RUNTIME module provides an operator's console with which the user is able to interface to the RTDS. Once the user has selected the desired case to run, the RTDS compiler will be invoked if necessary, the case downloaded from the host workstation onto the RTDS and the simulation started. During the simulation the user can monitor specific quantities using graphical icons of meters and plots. It is also possible to interact with the simulation in progress by selecting an assortment of available input icons. For example, a fault may be initiated by selecting a push button. The type, duration and length of the fault would have been defined during the DRAFT session. Figure 8 shows a screen dump of a RUNTIME window. Components which can be seen in the screen dump include sliders which control the set point of an exciter, meters which show machine quantities such as speed and torque, as well as plots which contain the three phase bus voltages during a single line to ground fault.

Due to the bandwidth of the ethernet LAN (10Mbits/sec), components such as meters are updated only every second or so. Meters are thus limited to displaying r.m.s. or other relatively slowly changing quantities. Plots, on the hand, must be refreshed manually by the user. By selecting the UPDATE option at the plot, a signal will be sent to the appropriate RTDS WIC to collect a certain number of samples of a user specified quantity. Once the data has been captured, it is sent back over the ethernet to the host workstation and displayed on the plot's grid.

Updating of plots can be automatically initiated shortly before a disturbance is applied. The result is that the user will be able to observe the response of the system to the disturbance with the plot containing a short span of data from before the disturbance. This feature can be likened to the pre–trigger feature found on most oscilloscopes.

PS–CAD: UNIPLOT & MULTIPLOT

Data captured during a RUNTIME session can be stored for plotting and analysis using the UNIPLOT module and for formatting into report ready pages using MULTIPLOT. Data collected from various simulation runs may be plotted simultaneously to allow close comparison of the results. It is also possible to perform fourier analysis on the waveforms directly from within UNIPLOT.

THE RTDS: APPLICATIONS

The first real application of the RTDS hardware was to test a Joint Var Controller (JVC) which was to be installed at Manitoba Hydro's Dorsey Converter Station [3]. It was required that the RTDS model a portion of the Nelson River HVDC System with emphasis placed on the inverter station's AC system. The JVC would monitor the reactive power supplied by component models representing synchronous condensers whose ratings were significantly different. Since all of the machines were connected to a common bus through transformers, the JVC's function was to ensure that the reactive power load was shared equally amongst the different machines. Figure 9 illustrates the setup used to perform the JVC tests. Input quantities produced by the RTDS and monitored by the JVC included the commutating bus r.m.s. voltage and machine reactive power outputs. The JVC in turn would provide set–point raise or lower pulses which were used by the exciter models simulated on the RTDS.

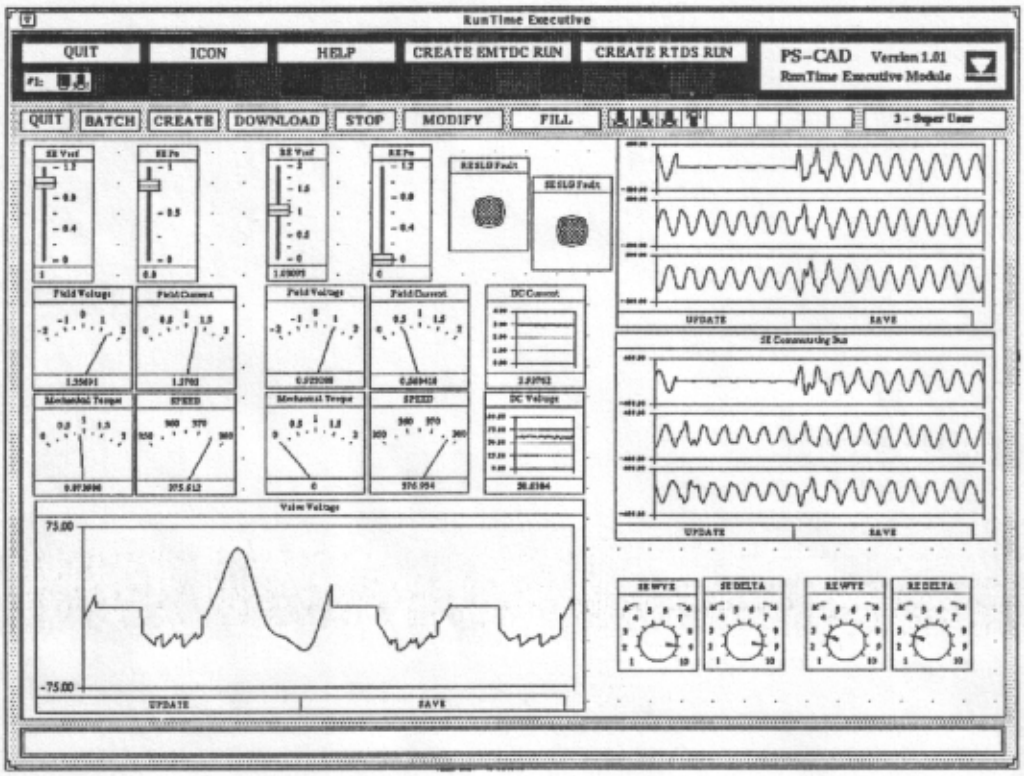


Figure 8: Screen Dump of RunTime Window

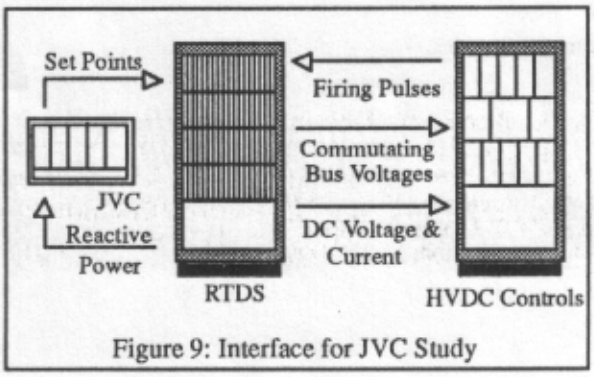


Figure 9: Interface for JVC Study

More recently the RTDS hardware was used to test relay performance when the protected line included series capacitors which were protected by MOVs. Protection of a series compensated line presents significant challenges to the relay designer since the series capacitors combined with their protection devices may show wide variations in impedance during fault conditions. By using the RTDS to model the line, its compensation components and associated sending and receiving end systems, relays can be tested to ensure proper operation under various fault conditions [4].

Figure 10 shows how the RTDS would be interfaced to the protective relay under test via voltage and current amplifiers. Due to the fact that the RTDS operates continuously in real–time, the relay's trip signal can be fed back to the RTDS and used to operate a breaker model. On–site testing of protection relays with the RTDS has demonstrated decided advantage in time and expediency over off–line playback test methods.

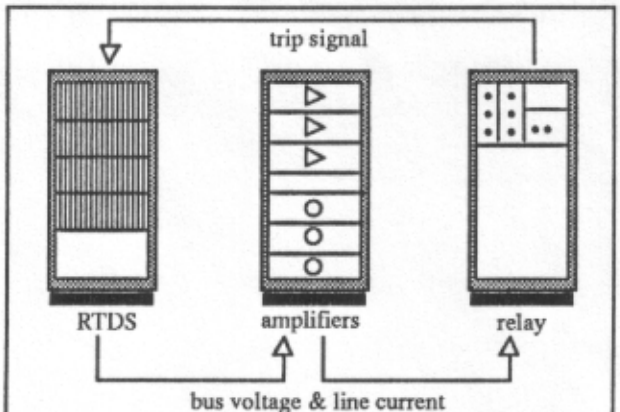


Figure 10: RTDS – Protective Relay Interface

RTDS hardware has also been successfully interfaced to an analogue HVDC simulator. A single cubicle of RTDS hardware can model a significant number of power system components, including long, mutually coupled transmission lines. An economical option to expand the capabilities of an existing analogue simulator facility is to interface a digital simulator, comprised of a few racks of hardware, onto the analogue simulator. Some care would have to be taken as to exactly which point in the system model the interface could be made, however. A typical application would be to make the interface at the AC commutating bus of a HVDC converter station. While the analogue simulator could provide models of the valve groups, converter transformers and dc system, the digital simulator could model the AC system extending out from the commutation bus.

The general scope of studies which could be performed using the RTDS includes –

- Conventional TNA type studies
- Breaker reclose sequences
- Relay test studies
- Power swings due to disturbance
- AC/DC System interactions
- DC System controls studies
- SVS applications and controls
- Geomagnetic induced current effects
- Operator training

THE RTDS: LIMITATIONS

Although real–time digital simulators provide definite technical and economic advantages over their analogue counterpart, there are nevertheless a number of limitations associated with the RTDS. Firstly, since the power system component models are written in low level machine language code highly integrated with the hardware, it is not possible for the user to develop their own unique component models. Secondly, there are limitations to the time–step with which a particular case may be run and still maintain real–time. Although time–steps on the order of 50 μs are adequate for many studies, certain simulation cases will demand a much smaller time–step. As time goes on faster processors will replace those being used today and the minimum simulation time–step will decrease accordingly.

The splitting of a network into subsystems, which are in turn allocated to single racks leads to limitations in the number of components which may be contained in one subsystem. This limitation may not be that severe since a significant subsystem size can be handled by a rack containing 36 processors (18 TPCs). Furthermore, by placing a very short, artificial line section the user can divide a single subsystem into two separate subsystems.

Placement of surge arrestors is limited to those which are located directly across series capacitors in the current version of the RTDS. Surge arrestor models can lead to the requirement that iterative techniques be used within a single time–step. On the RTDS these iterative techniques would lead to unacceptably large time–steps. The user is thus restricted to series capacitor MOV protection only, since the iterative techniques are not required in this case.

FURTHER DEVELOPMENT

Although there is no question that digital real–time simulators will play an important role in power system studies in the near future, there will be many challenges to meet the requirements of the users. Power system engineers involved in electromagnetic transients simulation studies are extremely demanding. Larger and larger system models with more complex power system components will be required. As more power electronic devices are introduced into the system models, time–steps will have to be reduced in order to ensure accurate results.

Since many of the power system controllers, especially HVDC and SVS controls are becoming digital, there is some demand to allow users to design new controllers using the RTDS hardware. Work is currently under way to develop a library of low level control function blocks. The user would be able to interconnect these blocks in a manner similar to which the power system model is assembled. Signals from the power system model could be used as input to the control function blocks. In this manner the RTDS could be used not only to model the power system, but also to design and test new control concepts for the power system components themselves.

OPERATIONAL EXPERIENCE

It has been observed that the most important feature of the RTDS is its graphical user interface, PS–CAD. New users are able to use the RTDS to perform power system simulations almost immediately. By allowing the user to graphically enter the schematic of the system model, many of the errors commonly made by new users are eliminated. Furthermore, by allowing the results of a simulation to be displayed very soon after the system model has been assembled, new users can quickly gain confidence in their ability to perform simulations.

Rough estimates indicate that the cost of a RTDS is some five times less that that of an equivalent analogue simulator. Since the RTDS is essentially nothing more than a specialized computer, its operating cost is extremely low.

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BIOGRAPHY

Rudi Wierckx was born December 7, 1961 in Rotterdam, The Netherlands. He graduated from the University of Manitoba with a B.Sc (EE) in 1983 and M.Sc. in 1985 and is currently enrolled in the Ph.D program. Since 1985 he has been employed by the Manitoba HVDC Research Centre with the title Simulation Engineer.