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PRACTICAL EXPERIENCE AND TECHNIQUES FROM AN HVDC VENDOR

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2023 EUROPEAN RTDS TECHNOLOGIES INC. USER'S GROUP MEETING 2023

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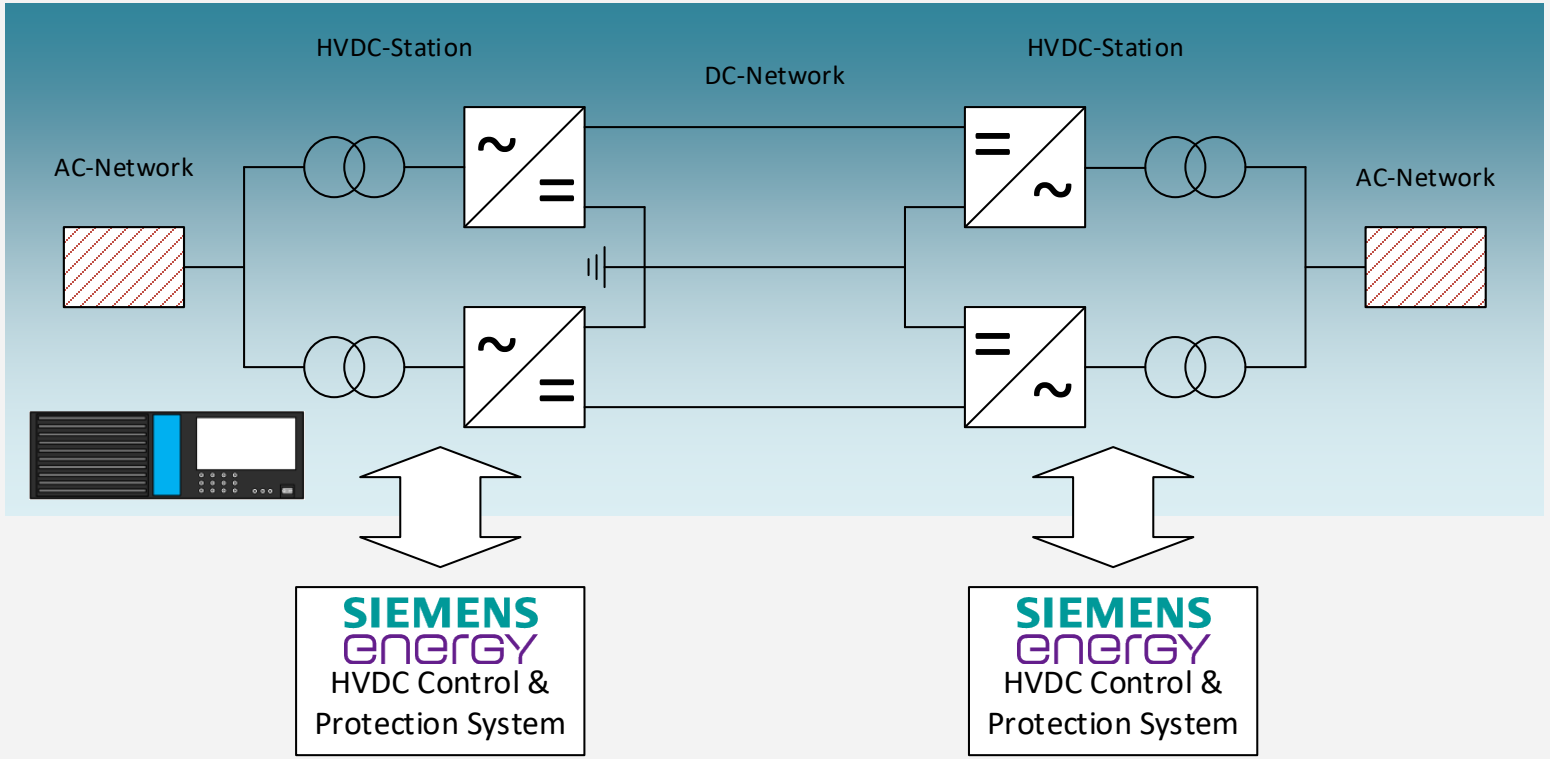
TOPICS

- Introduction
- Automated Hardware in Loop Test Setup with RTDS Simulator
- Modelling of Hybrid AC-DC-Systems
- Reduction of Computational Burden for HVDC Lines

PRACTICAL EXPERIENCE AND TECHNIQUES FROM AN HVDC VENDOR

- Hardware-in-the-loop testing of HVDC Control & Protection Systems
- Electrical model of HVDC System running in RTDS
- Controlled by real C&P Hardware



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AUTOMATED HARDWARE IN LOOP TEST SETUP WITH RTDS SIMULATOR

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AUTOMATED HARDWARE IN LOOP TEST SETUP WITH RTDS SIMULATOR

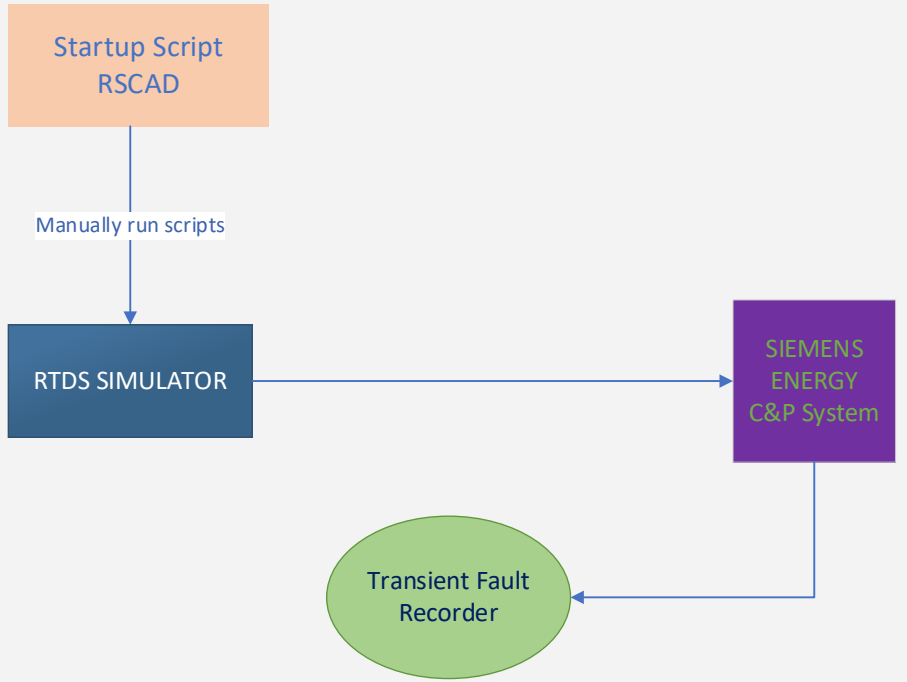
Motivation

- Test DC Protection Settings
- Automated Test Environment with a RTDS Simulator
- Implementation in Project during Integration and Testing Phase with Siemens Energy Control and Protection Cubicles
- Reduce Testing time and effort
    - Easy Analysis of the Test Records

AUTOMATED HARDWARE IN LOOP TEST SETUP WITH RTDS SIMULATOR

Initial Test Setup

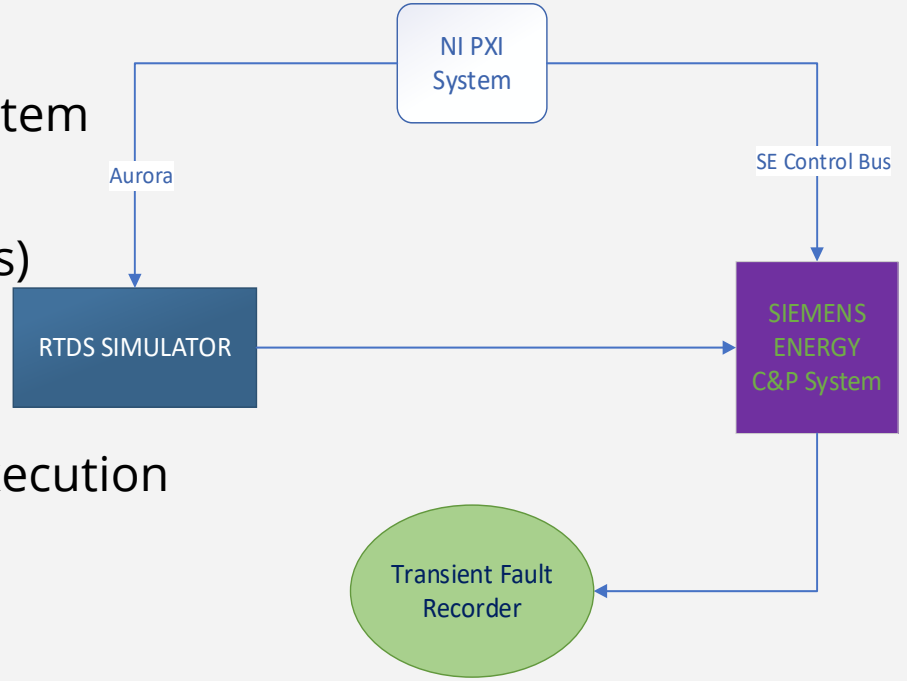
- Signal Check Model (Steady State Values)
- Startup Scripts for Slider Settings for each Protection Setting
  - Manually run a new script after for each protection
  - Developing Scripts and matching timing is also a tasking job
- Multiple weeks of testing for a complete check of the protection settings
  - Large number of tasks done manually



AUTOMATED HARDWARE IN LOOP TEST SETUP WITH RTDS SIMULATOR

Automated Test Setup

- NI PXI System to communicate with Control & Protection System via control bus and RTDS Simulator via Aurora
- Signal Check Model (RSCAD) with Aurora Variables (no sliders)
- Automatic execution of scripts to perform tests for all protection settings
- Aurora Communication for a seamless and uninterrupted execution in RTDS Simulator

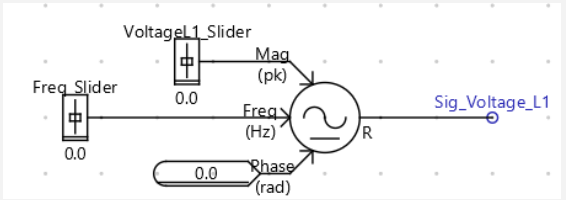


AUTOMATED HARDWARE IN LOOP TEST SETUP WITH RTDS SIMULATOR

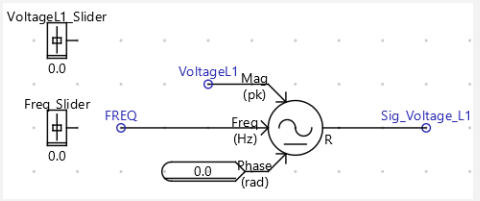
Automated Test Setup

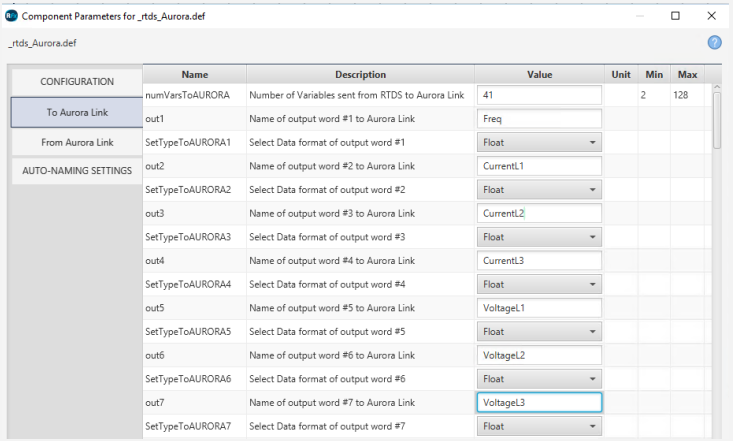
- The Sliders are replaced with Aurora Variables
- Scripts for all protection Settings can run simultaneously without stopping the tests

Implementation with Slider (Initial Setup)



Implementation with Aurora Variables (Automated setup)





AUTOMATED HARDWARE IN LOOP TEST SETUP WITH RTDS SIMULATOR

Advantages

- Aurora Communication is effective and advantageous in this Test Setup
- Weeks of testing effort during project phase reduced to some hours
- Manual effort to prepare start-up scripts and during testing significantly reduced

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MODELLING OF HYBRID AC-DC-SYSTEMS

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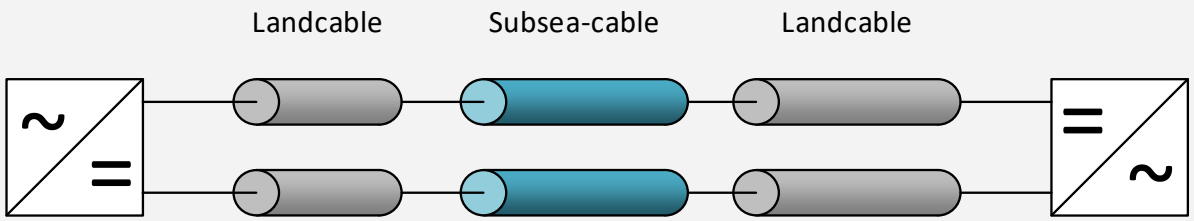
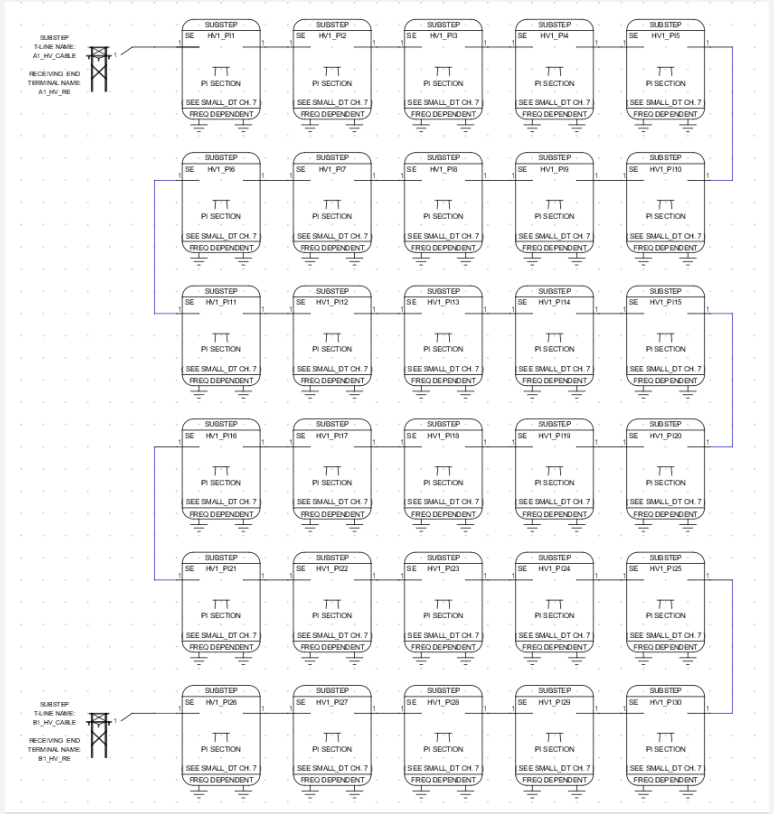
MODELLING OF HYBRID AC-DC-SYSTEMS

DC-System modelling

- In the past, modelling DC-systems was straight forward
  - Constant geometry over a longer distance
  - Low number of different geometries in one system

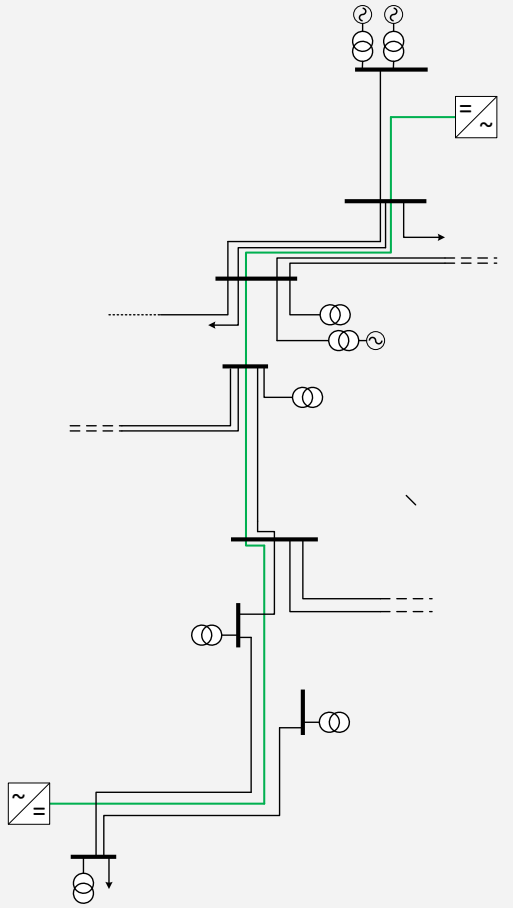




MODELLING OF HYBRID AC-DC-SYSTEMS

DC-systems using AC-towers

- No need to install new towers
- Challenges for simulation
  - Model must be valid for frequencies from DC- to several kHz AC
  - Input data features a high number of different line segments with different geometries and different parallel AC-systems
  - Coupling effects between AC-and DC-system have to be included



MODELLING OF HYBRID AC-DC-SYSTEMS

Two-Step-reduction

- Customer input as transmission system overview, tower geometries, systems on that tower… with 40+ segments
- The customer input was used to create a studies model which has improved performance and runs at 20µs – this was intended to be used in PSCAD
- The 20µs model featured 16 frequency dependent sections (Freq Phase), with up to 18 conductors on one tower (DC, 380kV, 220kV, 110kV)

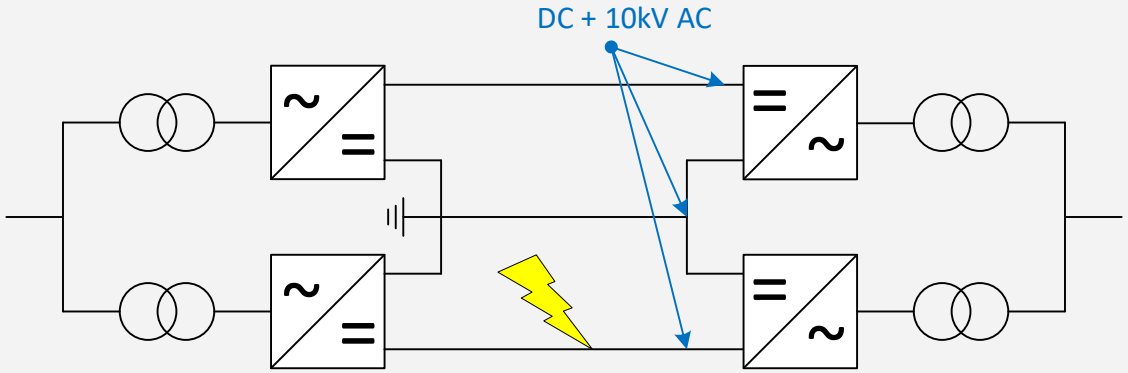
Requirements for RTDS

- Running at 50µs
- Maximum of 12 Conductors on one tower
- Bergeron Coupling lines in the beginning and the end to interface into substep (HVDC station)

MODELLING OF HYBRID AC-DC-SYSTEMS

Reduction – Acceptance criteria

- No change in DC-resistance of complete system
- 10kV induced AC-voltage on the DC-voltage of the non-earthed station
- No significant change in dynamic behavior for DC-faults compared to 20µs model



MODELLING OF HYBRID AC-DC-SYSTEMS

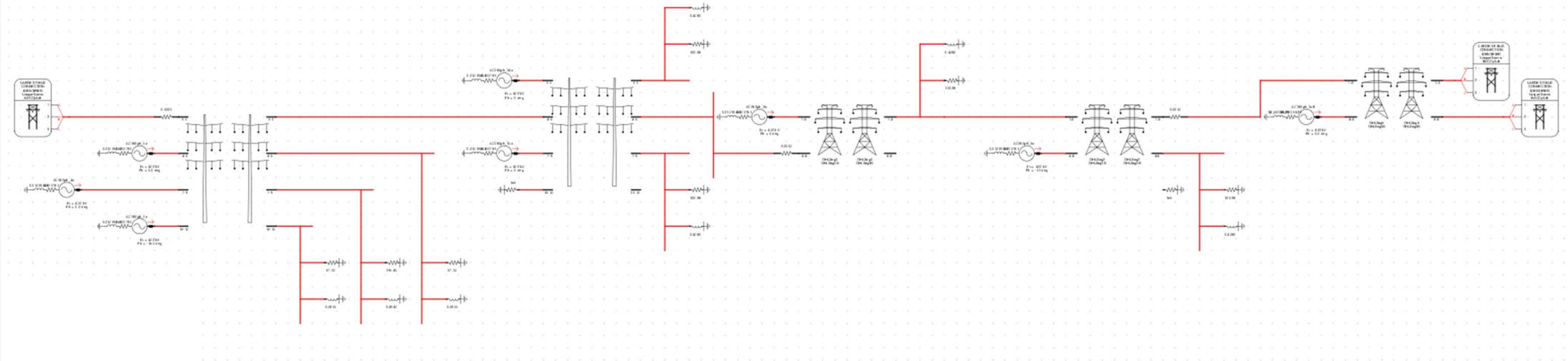
Reduction – Approach

- Removed parts of the system that had very little influence on the behavior (110kV and 220kV systems)
- Combined parts of the overhead-line that had similar geometry – also parts that were not directly next to each other
- Adapted the line length to keep the DC-resistance constant
- Adapted the loadflow in the parallel AC-systems to reach 10kV rms on the DC side
- Repeat Dynamic-performance study and benchmark vs detailed model
- Benchmark offline simulation vs realtime simulation

MODELLING OF HYBRID AC-DC-SYSTEMS

Reduction – Resulting model

- 7 overhead line segments running in large timestep
- Bergeron transmission lines in the beginning and end as an interface to the HVDC station
- 630 Load units + network solution

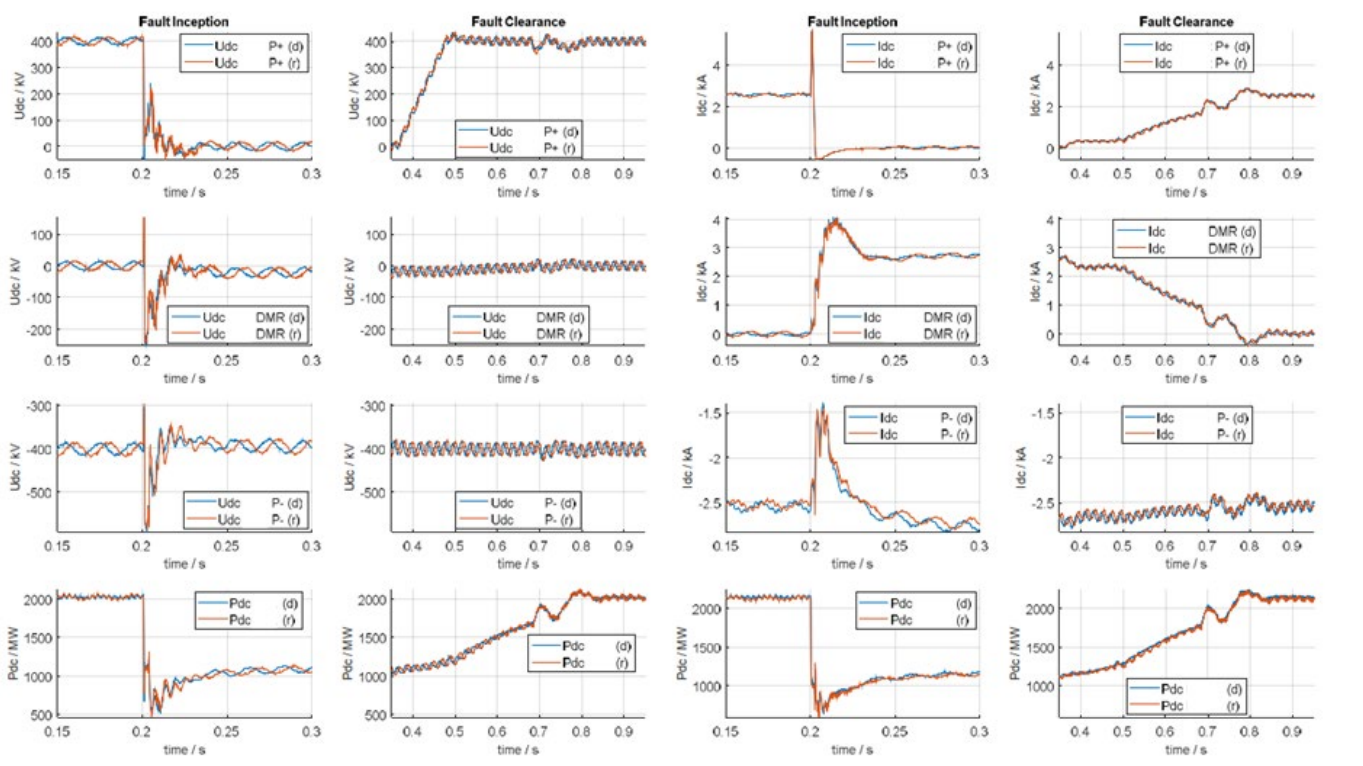


MODELLING OF HYBRID AC-DC-SYSTEMS

Reduction – Result

Benchmark tests vs the detailed model using the HVDC control show very good representation of

- AC-DC-coupling effects
- DC-line losses
- DC-fault performance



Dynamic benchmark test for DC-fault using the HVDC control

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REDUCTION OF COMPUTATIONAL BURDEN FOR HVDC LINES

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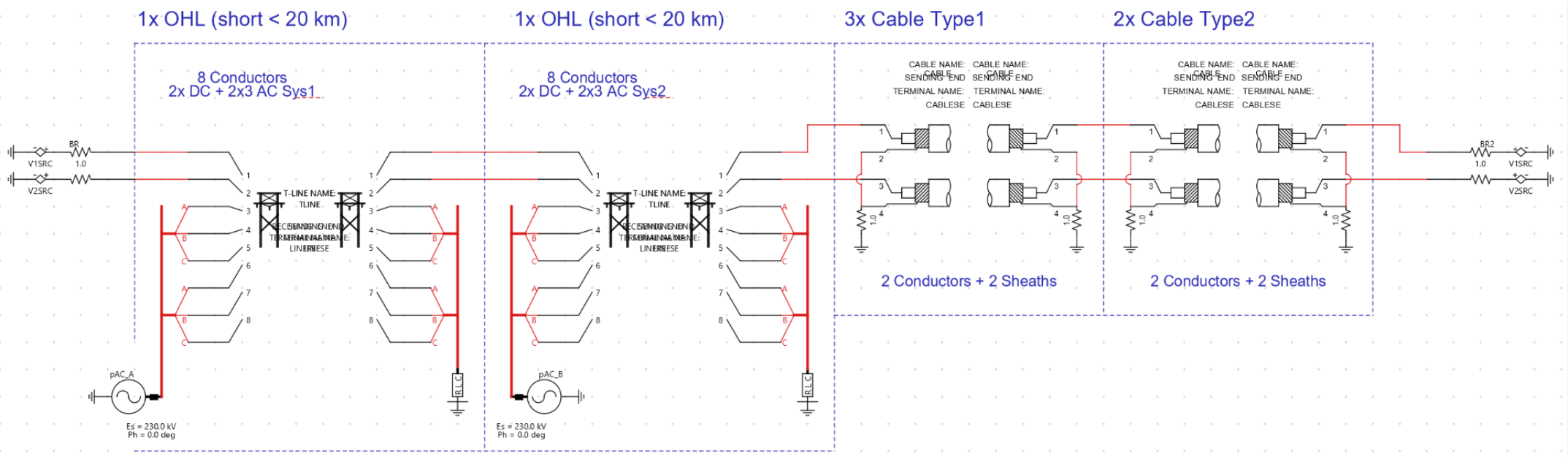
EXAMPLE CASE



Complex Transmission lines require lots of hardware power when modelled in full detail.

→ Trade-off between detail grade and performance

In this example the required 14 NovaCor cores can be reduced to 3 by optimisation with minimal reduction in precision.

PERFORMANCE OPTIMISATION

Model Simplifications

General Tip: always check the model requirements and design the model accordingly

- Use of mainstep instead of substep
  → big savings for esp. cables (might require interface lines)
- Use of a PI Section model
  → for short(er) cables or tlines / low frequencies (e.g. < 5 kHz)
- Merge of similar lines
  → check fault location requirements

Example requirements: up to 10 kHz, Fre-Phase preferred, multiple Fault locations, few cpl lines

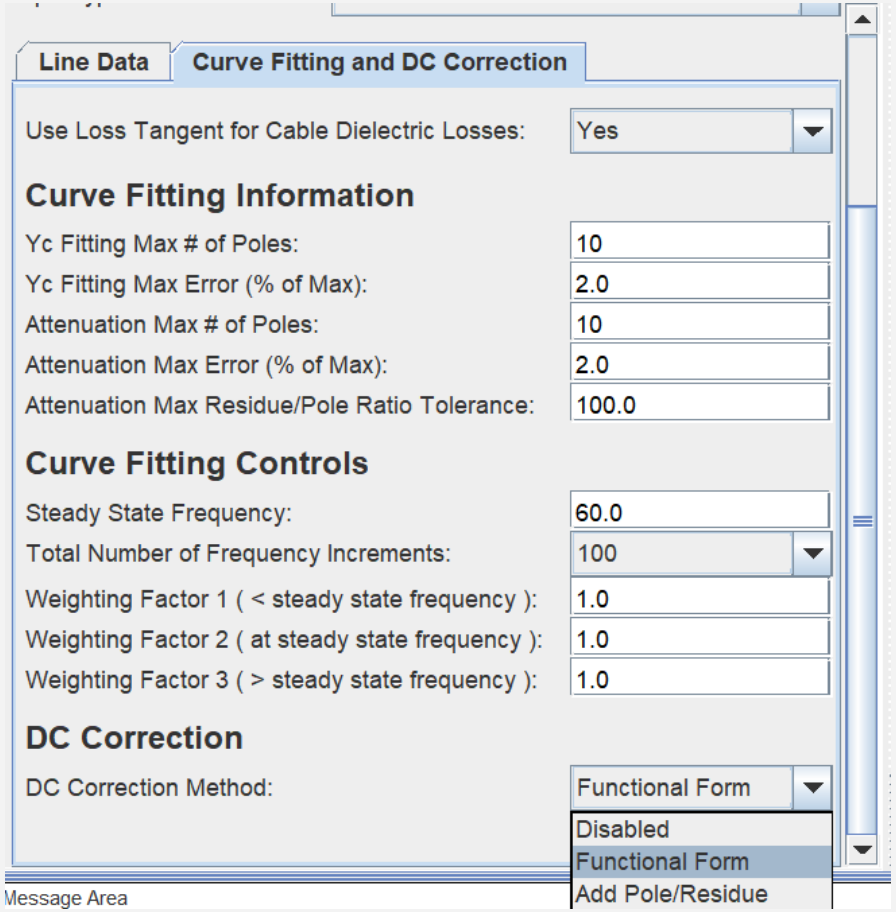
PERFORMANCE OPTIMISATION

Tline + Cable optimisation

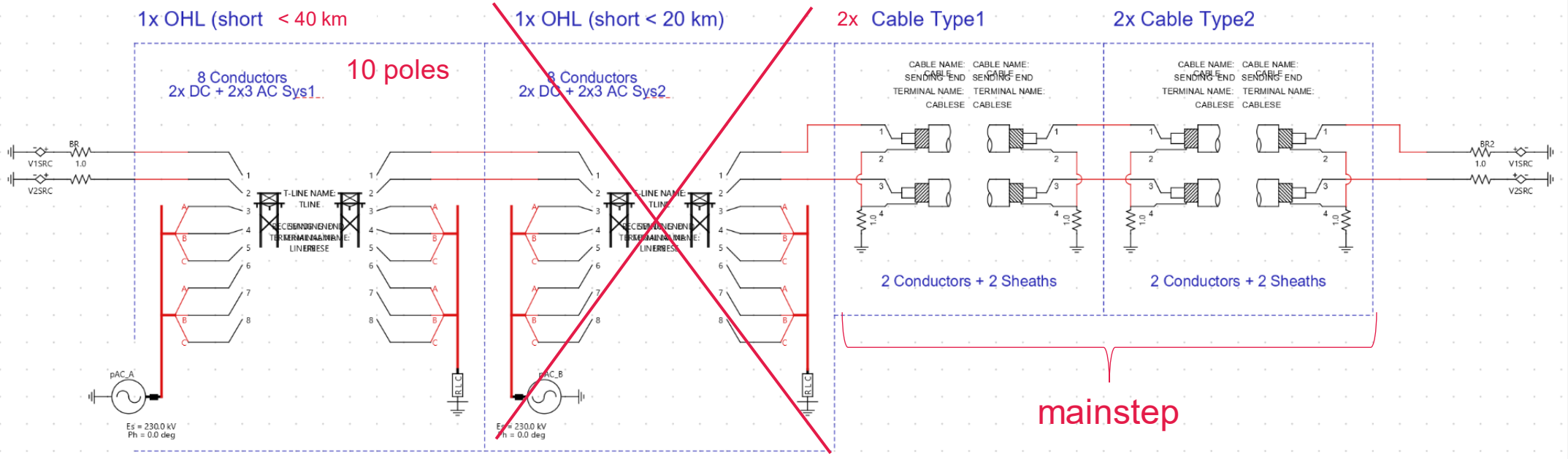
Component Performance is impacted by:

- Number of conductors (G-Matrix ~ n^2)
  - → Negligible mutual coupling; low impact parallel lines
- Number of Poles / Curve Fitting
  - → Higher Fitting error can be compensated by smaller frequency spectrum
  - → DC Correction set to functional form

When using less than 8 conductor 10 poles, GTFPGA model becomes an option



EXAMPLE CASE



→ Merge of OHL

→ Merge of Type1 cable to 2 segments (50% length fault criteria)

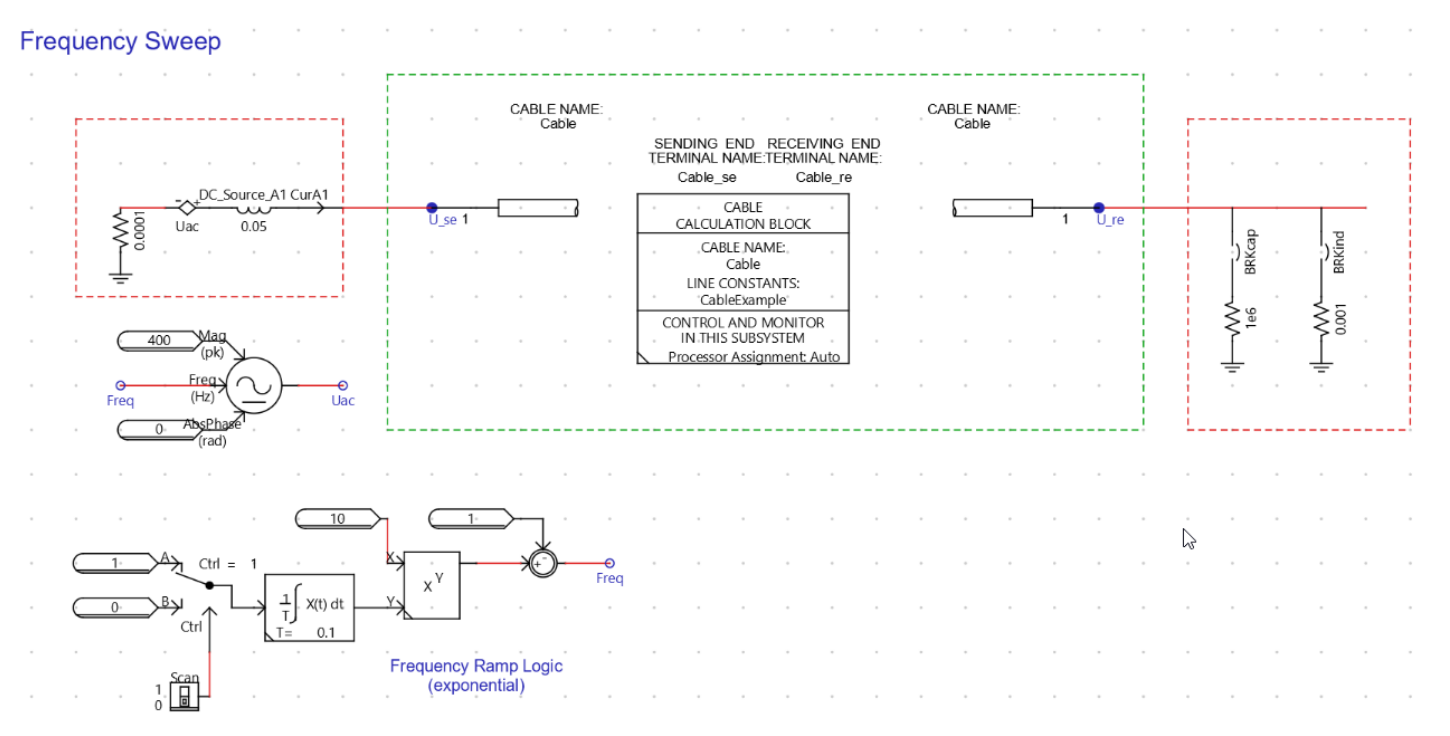
→ Move Cable to mainstep, include interface line

→ Reduction of OHL to 10 Poles (instead of 12; f_{max} = 15 kHz)

→ Option to use GTFPGA and/or removal of 1 AC-system (3 conductors)

BENCHMARKING

Frequency Sweep/Scan



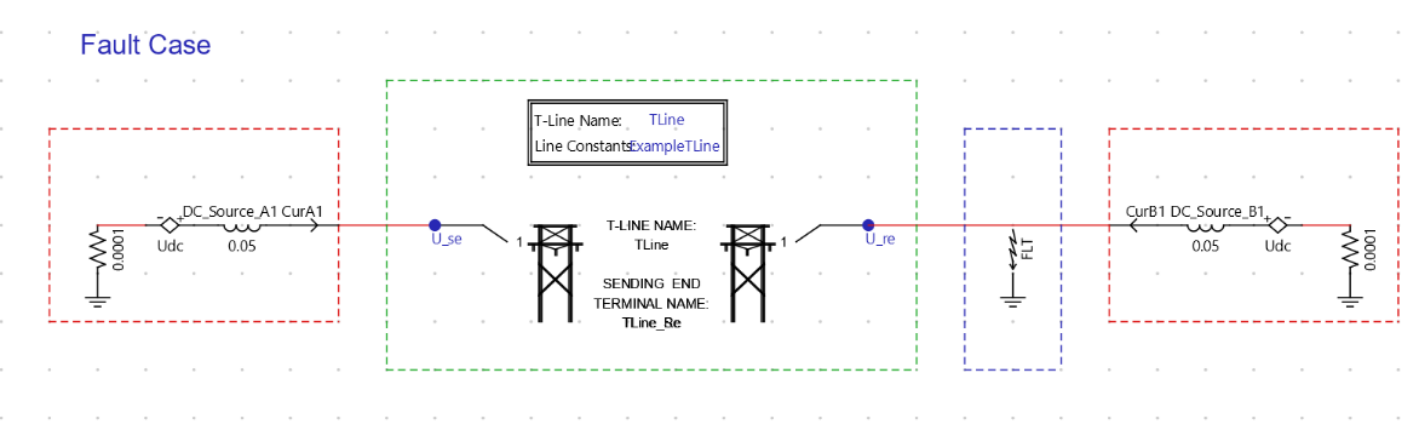
Simple Test circuit for capacitive and inductive frequency sweep

Frequency will be ramped up (from 0 to e.g. 10 kHz).

Poles and frequency behaviour should overlap as much as possible between reduced and original transmission line

BENCHMARKING

Fault Test(s)



Example Circuit for Fault Testing

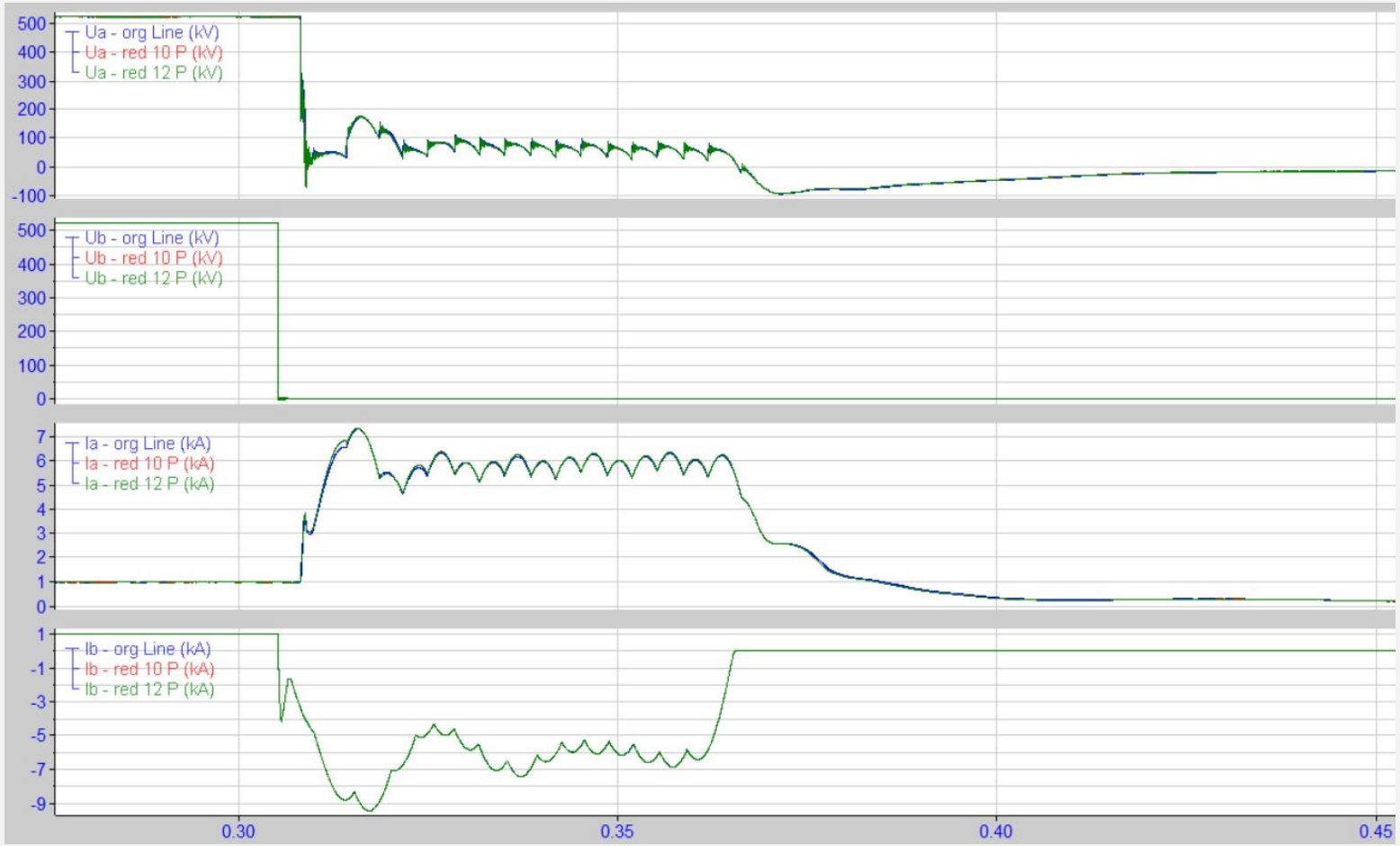
Steady state voltage is applied to the current sources. Then the fault FLT is applied.

Voltage and Current curves between reduced and original line should overlap
Curve fitting graphic 12vs10 poles

BENCHMARK EXAMPLE

Ground Fault at Station B

Comparison between
Original Line (blue)
Reduction 10 Poles (red)
Reduction 12 Poles (green)



THANK YOU FOR YOUR ATTENTION, QUESTIONS?