RTDS HARDWARE NEW DEVELOPMENTS

CYPRIAN PETERS

RTDS TECHNOLOGIES INC.

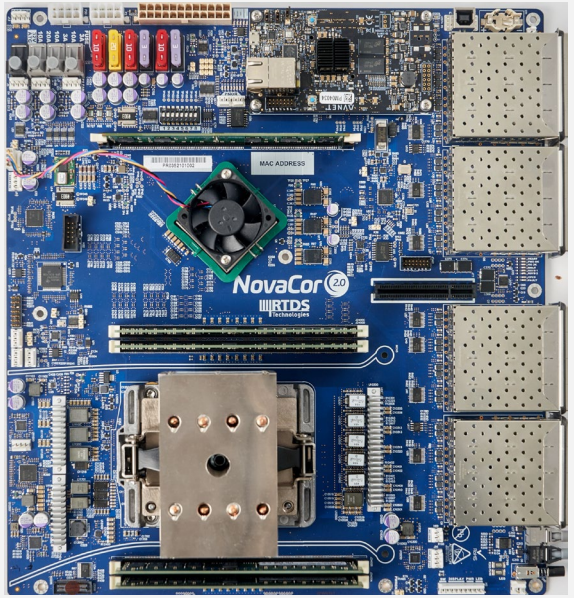
AGENDA

- NovaCor 2.0
- Introduction to GTSOC
- Using GTSOC for Black Box Controls
- GTSOC v2

INTRODUCING NOVACOR 2.0

- New generation of RTDS Simulator hardware
- Based on IBM's POWER9 (multi-core RISC processor, same family as POWER8)
- 3.8 GHz clock frequency
- 20-25% performance increase over NovaCor 1.0

NovaCor 2.0



INTRODUCING NOVACOR 2.0

- Same form factor and hardware architecture as NovaCor 1.0
  - Optional cubicle for housing up to three chassis
  - Core licensing allows for scalability
- Same user experience
- 100% code compatible

COMMERICAL INFORMATION

- 5% higher price compared to NovaCor 1.0 (with 20-25% increase in capability)
- Core licenses from NovaCor 2.0 and 1.0 are ***not interchangeable*** (i.e. cannot transfer cores between 2.0 and 1.0 chassis)
- Hardware exchange available to customers with active hardware warranty

HARDWARE EXCHANGE PROGRAM

- Similar to NovaCor 1.0, no exchange discount on base unit (must purchase chassis, which includes one core license)
- Exchange discount applicable for each additional core license by returning the following equipment

Exchange Item	Exchange Discount
5 x 3PC	50%
2 x GPC	50%
1 x PB5	50%
1 x GTWIF	50%
1 x NovaCor 1.0 core license	50%
1 x NovaCor 1.0 chassis	50%

CAPABILITY COMPARISON

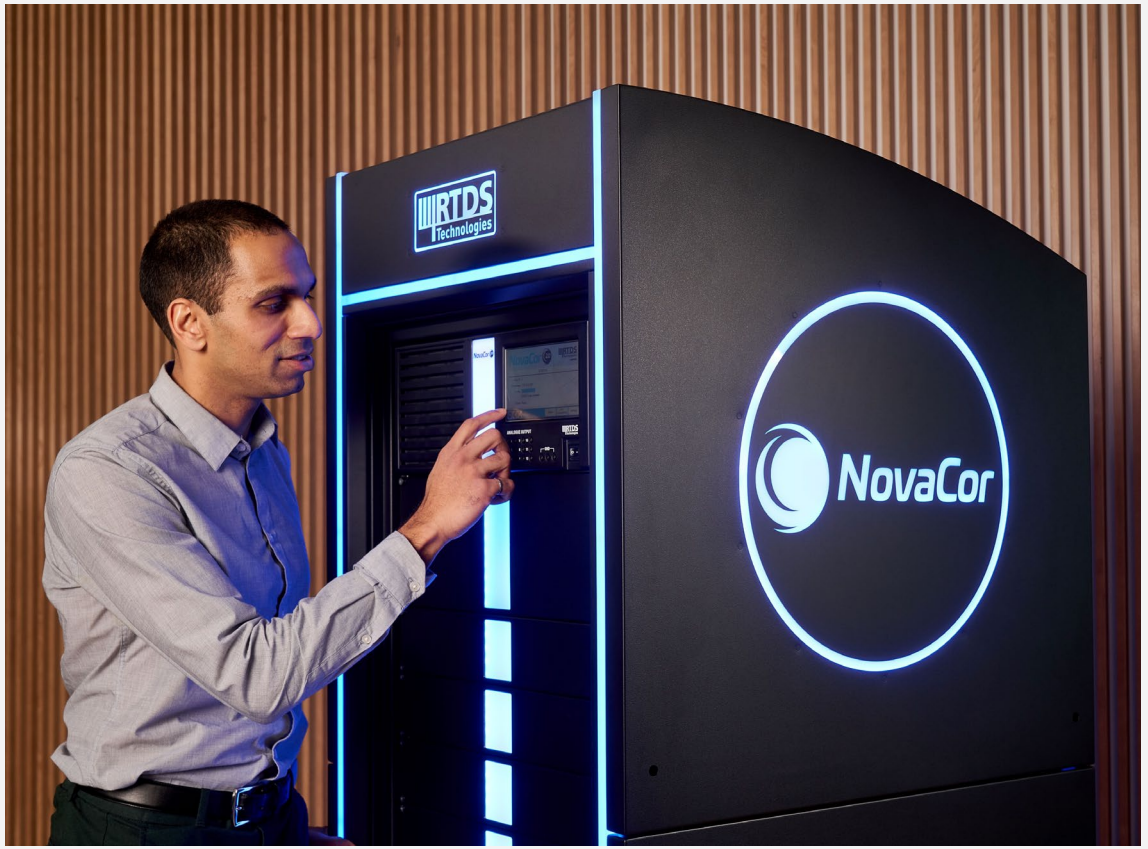
Category	NovaCor 1.0	NovaCor 2.0	Percent increase
Load Units	300	360	+20%
Mainstep Nodes	90	108	+20%
1 core	300	360	+20%
2 cores	600	720	+20%
Substep Nodes	60	75	+25%
Superstep Nodes	300	360	+20%
Distribution Mode	1200	1500	+25%
TSA	2000	2000	Unchanged

NEW FEATURE: STANDBY MODE

- Reduces chassis power draw to only a few watts
- Improved remote reboot capability

NOVACOR 2.0 COMPATIBILITY

- Connect NovaCor 2.0 units to NovaCor 1.0 units for multi-chassis simulation
- Not compatible with earlier hardware generations (PB5, GPC, etc.)
- Compatible with all existing I/O and peripherals
- Supports RSCAD FX (not compatible with RSCAD V5 and previous)



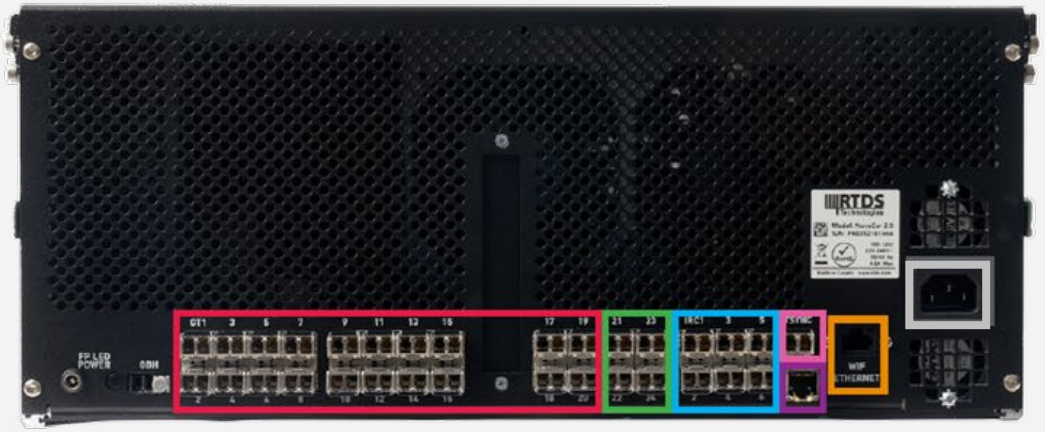
OTHER SPECIFICATIONS

Front of NovaCor 2.0 chassis

12 x analogue outputs

Chassis on/off

Back of NovaCor 2.0 chassis



20 x fibre ports for analogue/digital I/O and GTNETx2 cards

4 x fibre ports for Aurora protocol-based I/O (via licensing)

6 x fibre ports for inter-chassis connections

1 x GTSYNC fibre port

1 x Ethernet port for UDP-based I/O

1 x Ethernet port for workstation interface

Power

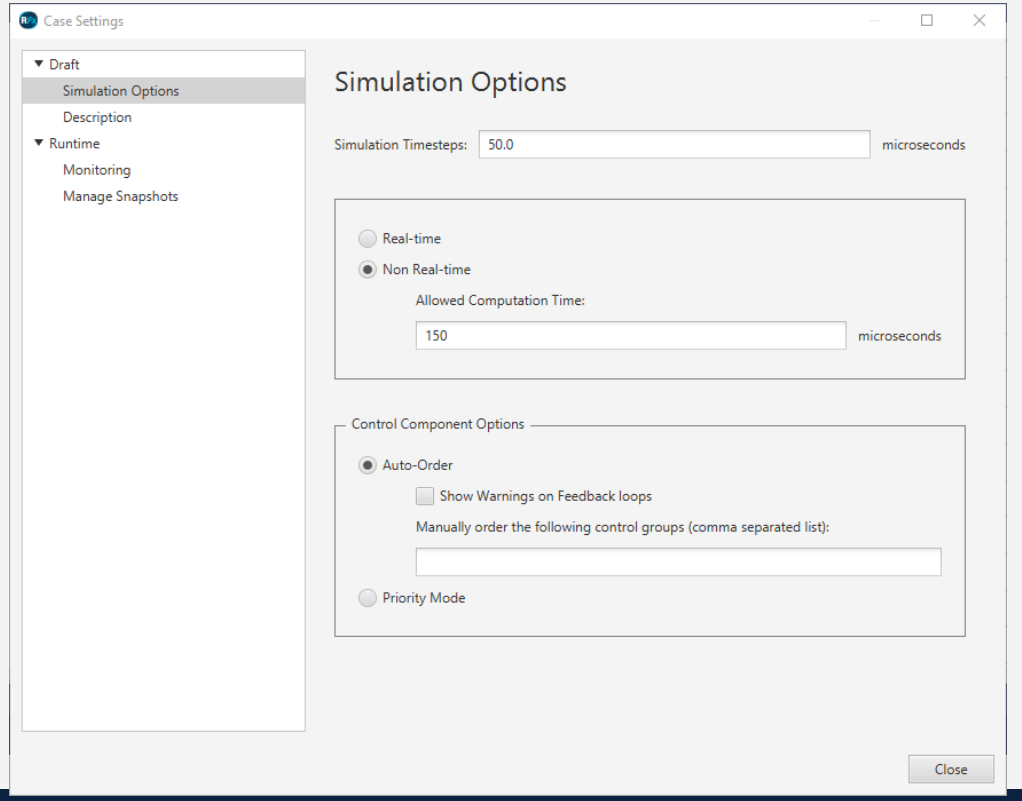
OTHER SPECIFICATIONS

PROCESSOR	IBM® POWER9® RISC processor 10 cores operating at 3.8 GHz
CONNECTIVITY	20 x I/O ports 6 x IRC ports 1 x GBH port 1 x GTSYNC port 1 x UDP port (for external devices) 4 x Aurora ports (for licensing) 1 x Ethernet port (for WIF)
SCALABILITY	Up to 10 licensed cores per chassis Up to 144 interconnected chassis
POWER	450 W max., 100-240 V, 50/60 Hz
DIMENSIONS	48.3 x 52.2 x 17.8 cm (W x D x H) ~15 kg (weight)

NON-REAL-TIME SIMULATION

The RTDS Simulator has always supported Non-Real-Time

- Supported on all generations
- Traditional non-real-time has same capacity as real time (i.e. no increase in network size when switching from real time to non-real time)
- Allows slower and faster than real time modeling
- Support for traditional non-real time mode will continue



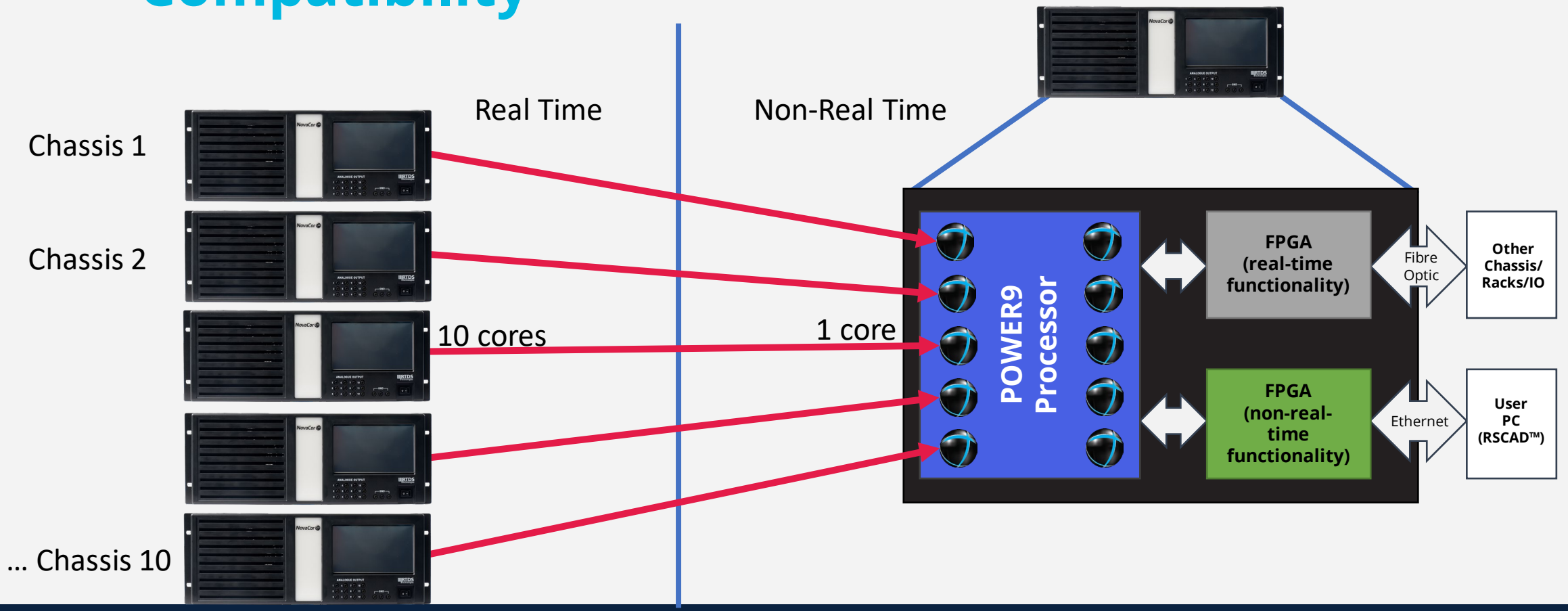
NEW FEATURE: ENHANCED NON-REAL TIME SIMULATION

New feature available on NovaCor 2.0

- **Enhanced simulation capacity** when using non-real time simulation
  - ~10 times real time capacity
  - Minimum execution time of 200 microseconds

LARGE NON-REAL TIME SIMULATION

Compatibility



LARGE NON-REAL TIME SIMULATION

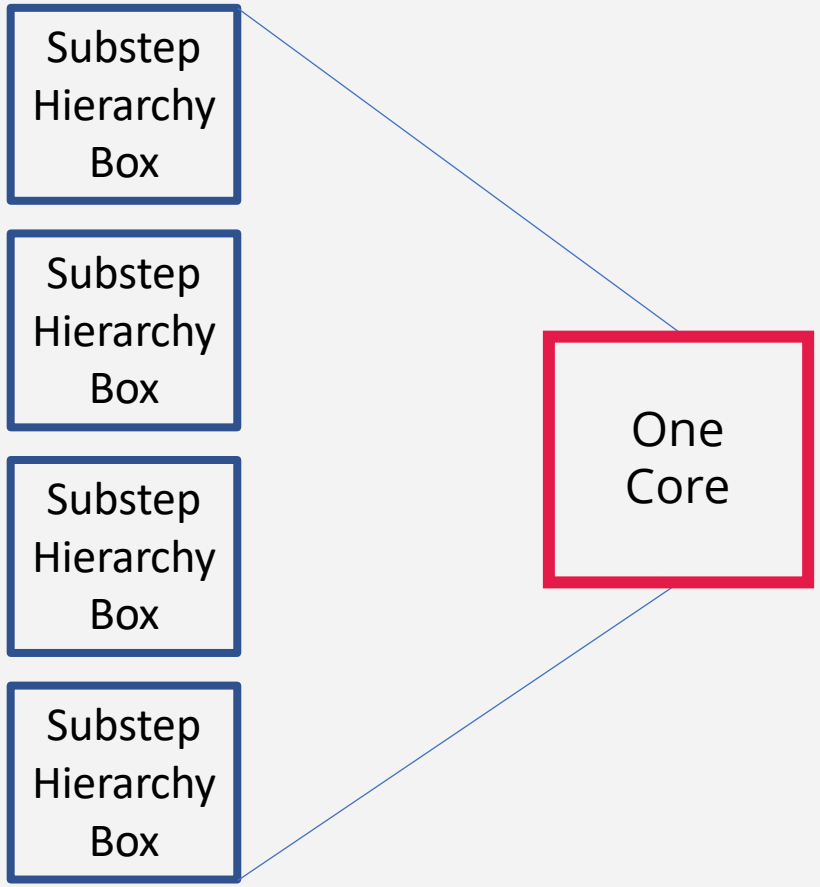
Quick transition

- Allows quick and easy transition between non-real time and real time simulations
- Identical handling in RSCAD FX for real time and non-real time simulations with the use of subsystems

LARGE NON-REAL TIME SIMULATION

Substep Support

- All on one core
  - ✓ Move Substep subnetworks from one chassis to one hierarchy box for non-real time simulation



LARGE NON-REAL TIME SIMULATION

Compatibility

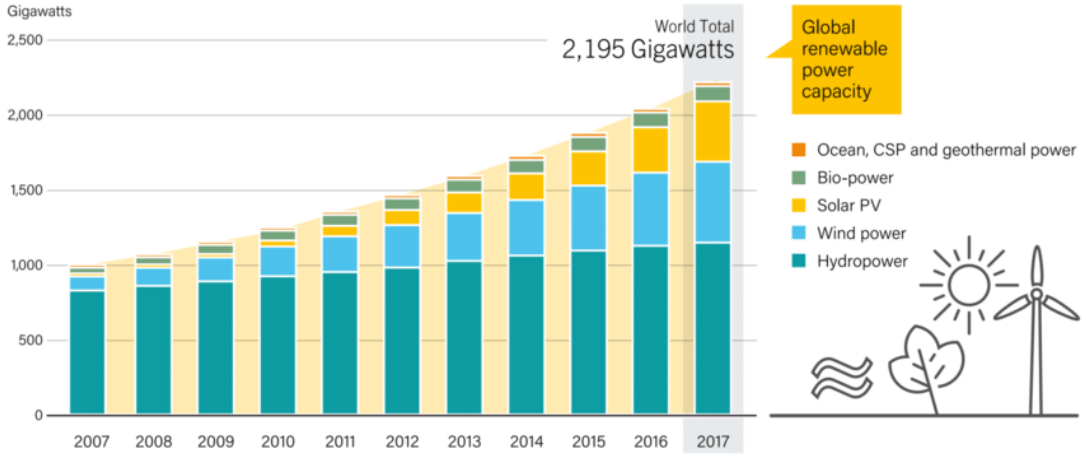
- Support for GTSOC black box models
- No other I/O allowed
- Support for co-simulation with PSCAD™
- Inter-connection with NovaCor 1.0 non-real-time simulation allowed
  - ✓ Standard real time limits will apply for NovaCor 1.0

THE CASE FOR GTSOC

- Renewable energy growing rapidly (From January to September 2022, **77 GW** of new renewable auction capacity was awarded globally)

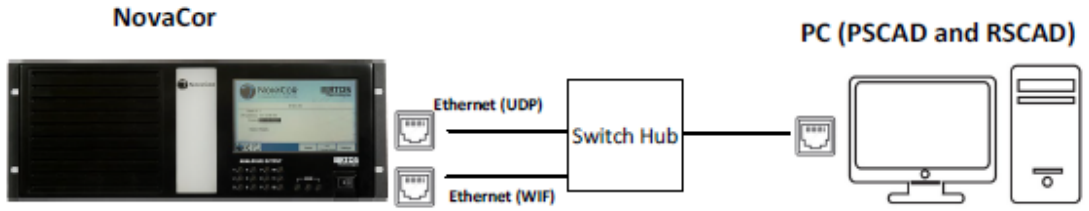
- Utilities require accurate model
- Manufacturer IP protection

- Controller **hardware**-in-the-loop simulation
- Controller **software**-in-the-loop simulation (black box controller)



ALTERNATIVE METHODS

- CBuilder
- Precompile method
- PSCAD-RSCAD Cosimulation (not real time)
- Interval Zero (Webinar with Vestas)
- GTSOC (best solution)



Introduction to GTSOC

Real-time required!

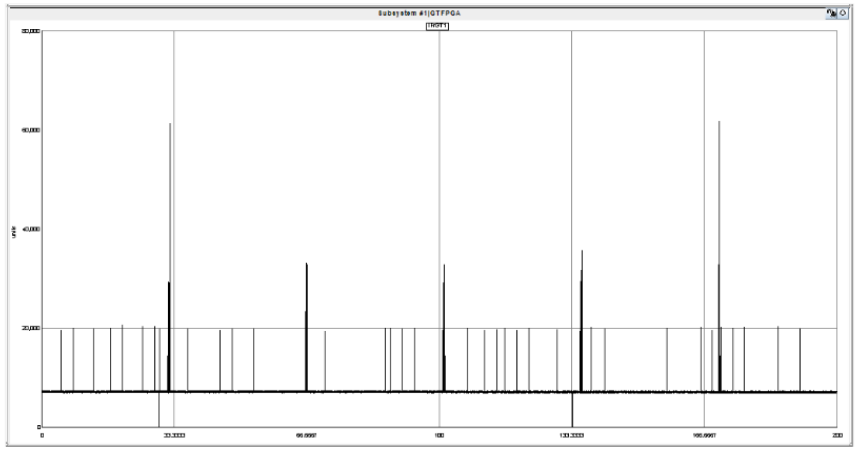
- Hardware
- Operating system
- Dynamic or static library

		Operating System		
		Windows	Linux	Bare Metal
Hardware	PC	Dynamic: .dll Static: .lib	Dynamic: .so Static: .a	X
	ARM	X	Dynamic: .so Static: .a	**Static: .a**

× **Linux OS running dynamic library (.so)**

The problem is the **indeterministic** execution time spike ~ 200 us, which is hard to eliminate without third-party real-time OS support.

80µs

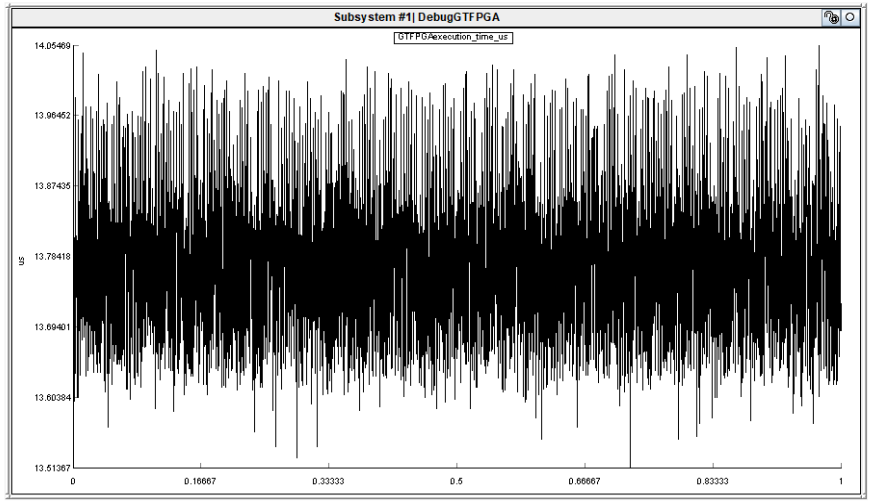


8µs

✓ **Bare-Metal running static library (.a)**

Bare metal guarantees **deterministic** timing:
<1us spike.

14.05µs



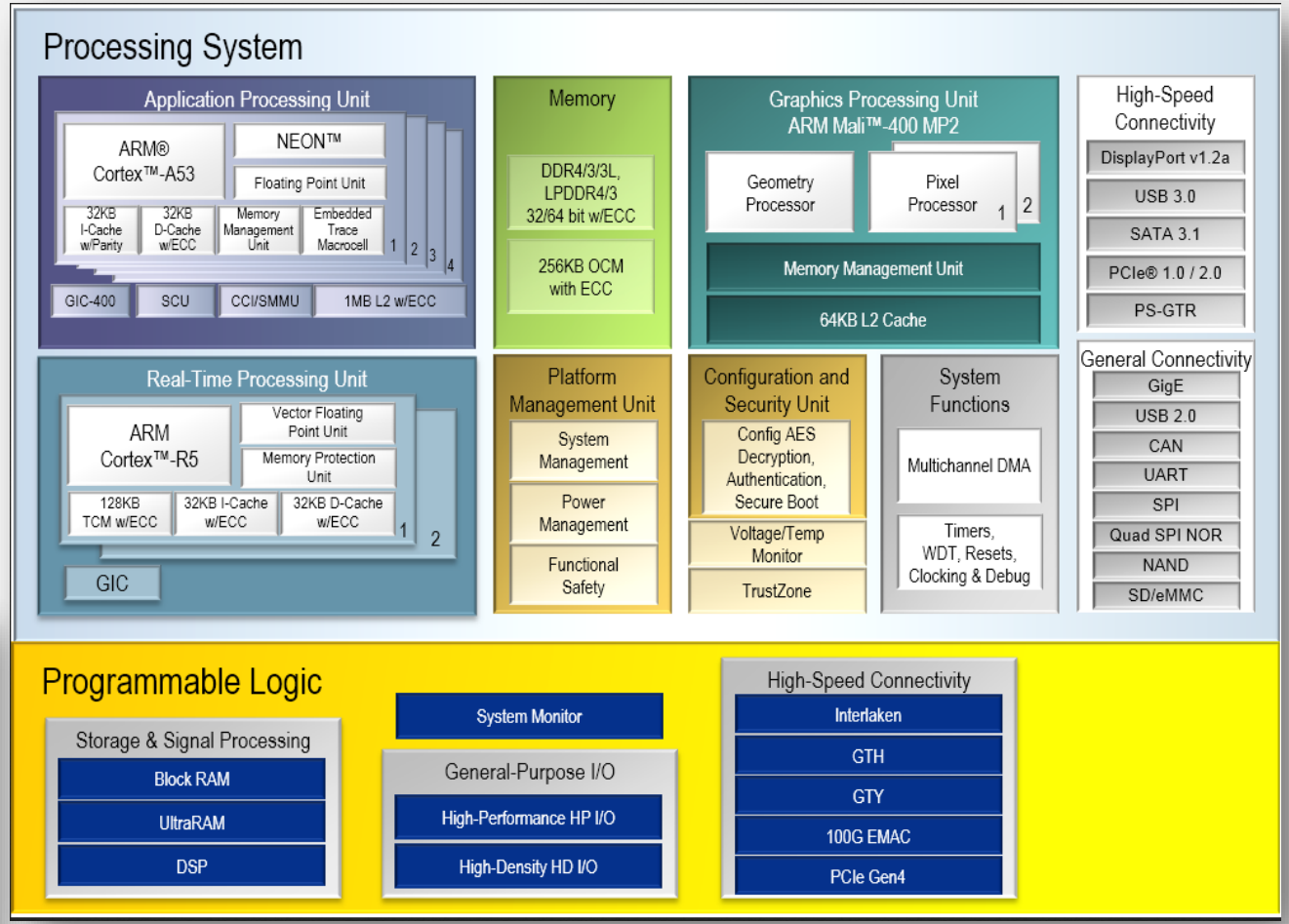
13.51µs

INTRODUCTION TO GTSOC

- New generation of FPGA platform
- GTSOC - integration of FPGA and Multi-Processor System-on-Chip (MPSoC)
- New applications using processors: e.g. Blackbox controller simulation

INTRODUCTION TO GTSOC

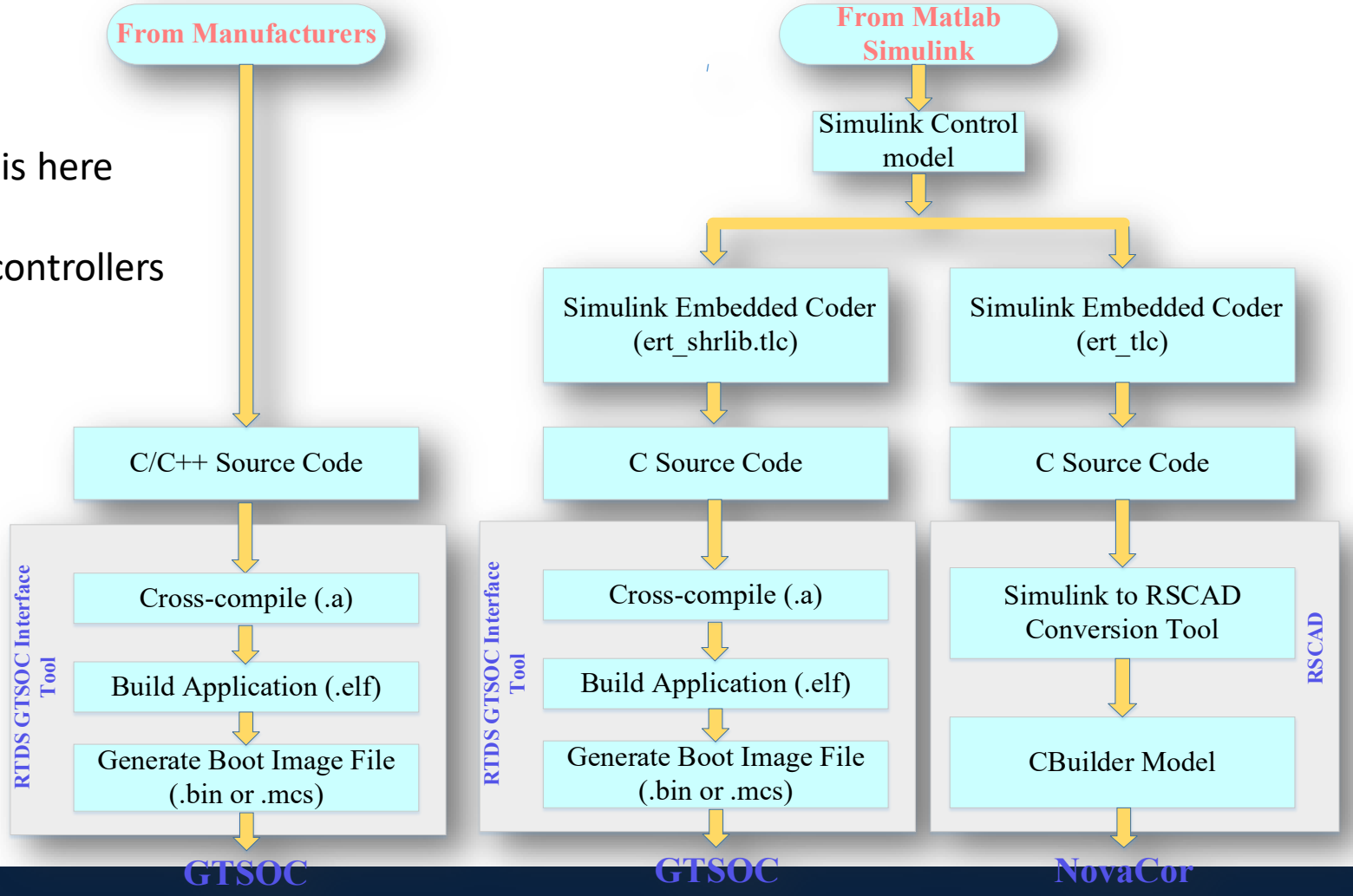
- **Xilinx Zynq UltraScale+ XCZU15EG**
- **Processing System (PS)**
  - 4 Application cores: ARM Cortex-A53
- **Programmable Logic (PL)**
  - Larger than VC707-based GTFPGA
  - Seamless migration for existing GTFPGA applications



Blackbox Controller – Procedure

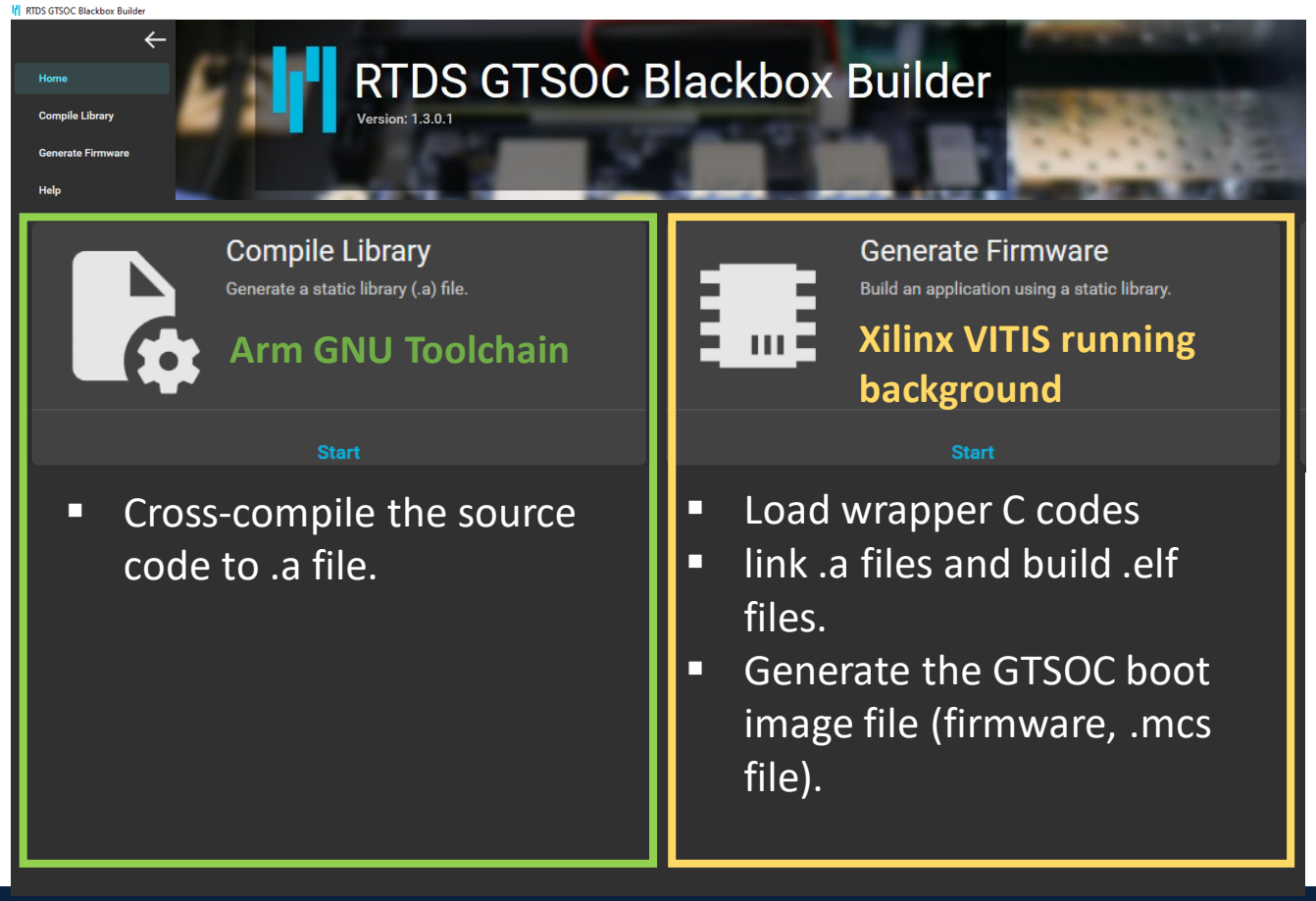
- From MATLAB Simulink
  - Quite straightforward if control is here
  - CBuilder a possibility
  - Cbulider not ideal for complex controllers

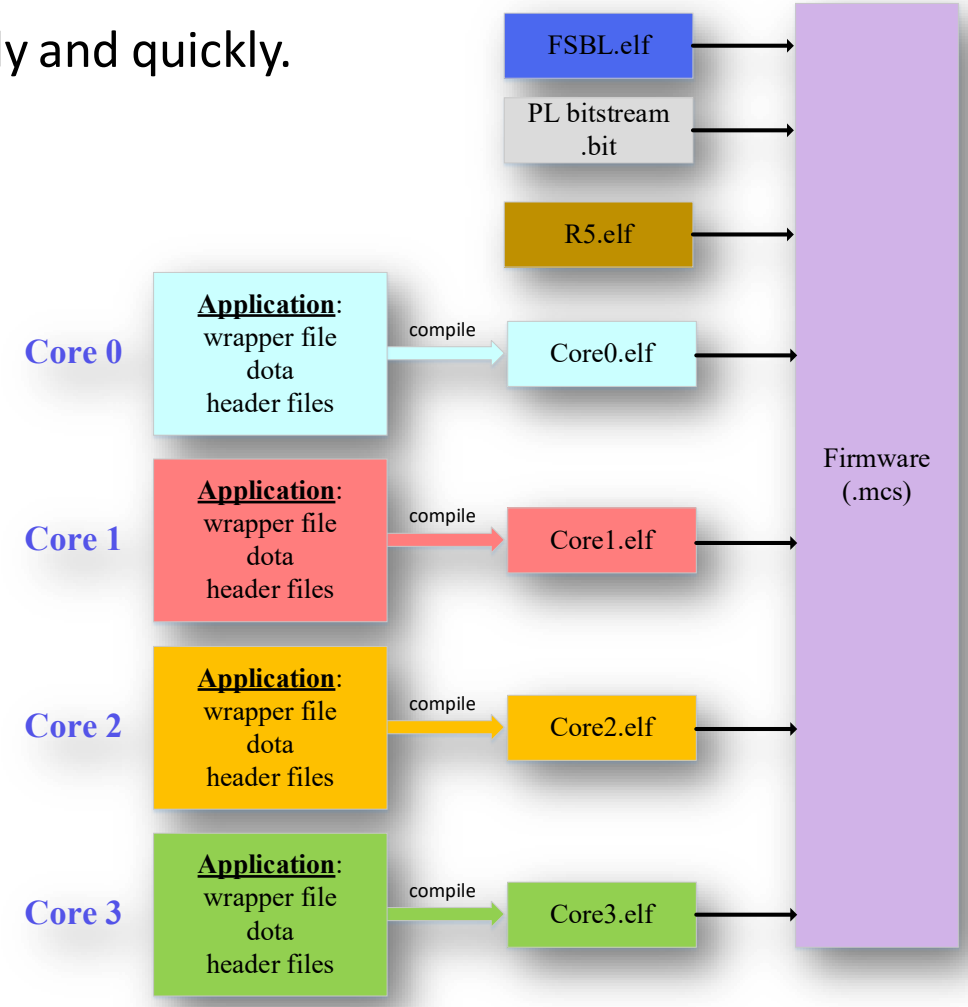
- From source code
  - C/C++/Fortran



Blackbox Controller – GTSOC Blackbox Builder

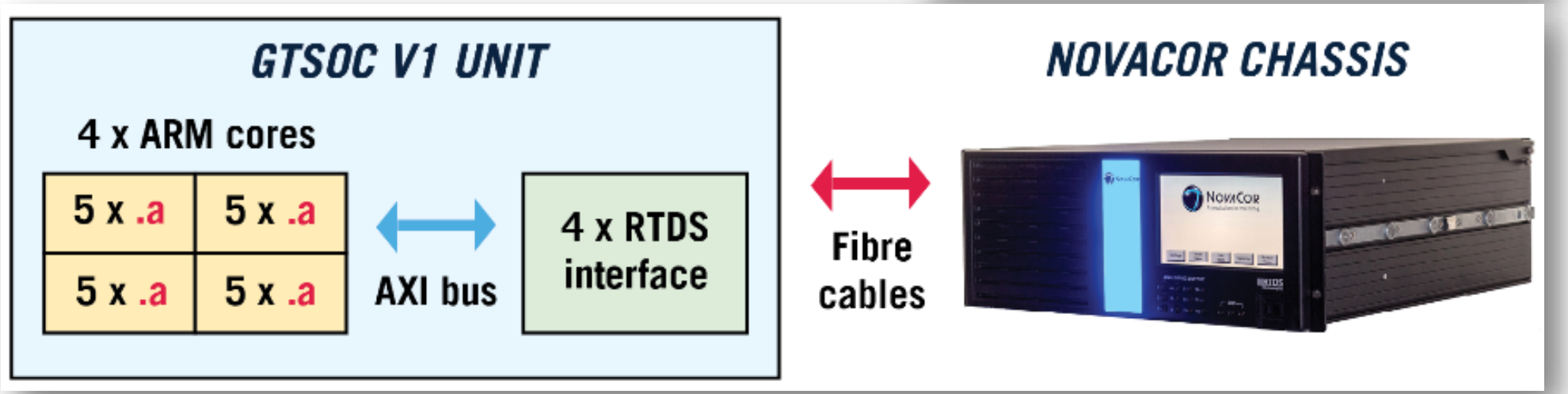
Establish black box controller simulation on GTSOC automatically and quickly.





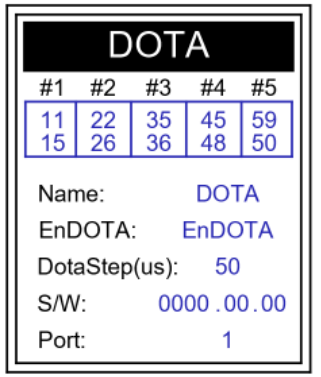
Blackbox Controller – Hardware

- GTSOC
- NovaCor only (Not PB5)
- Standard fibre connection
  - 1 fibre per core
  - Working on one fibre to all cores

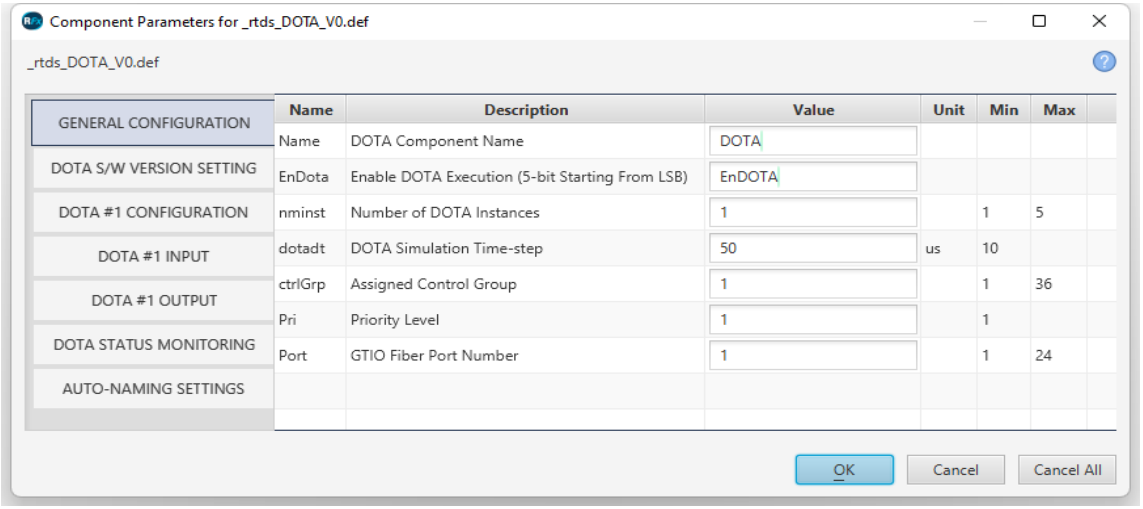


Blackbox Controller – Interface

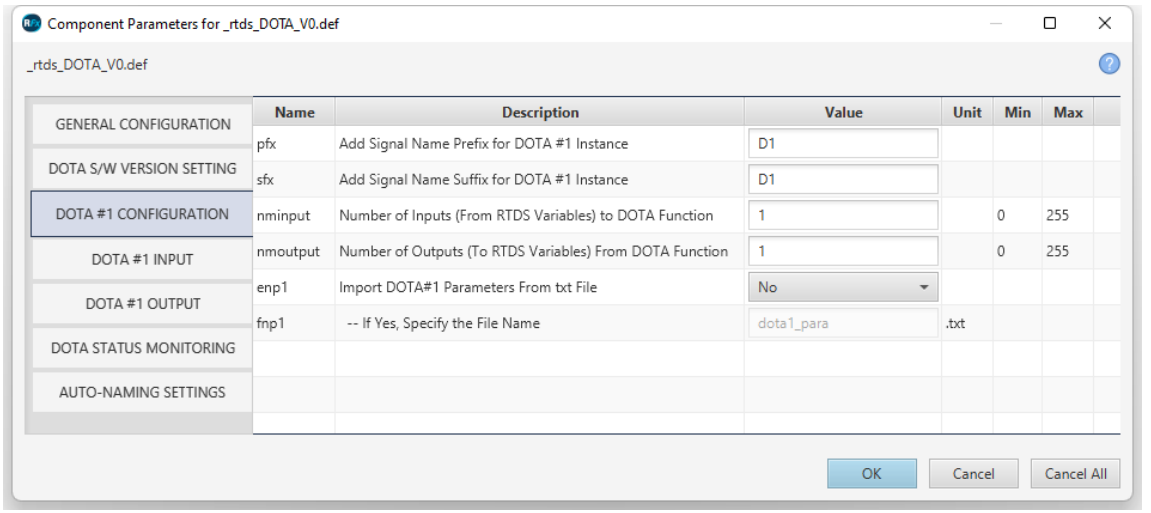
- Each GTSOC core needs one DOTA component (up to 4 DOTA components per GTSOC board)
- Each DOTA component supports up to 5 DOTA instances (up to 20 DOTA instances per GTSOC board)
- Each DOTA instance supports up to maximum 255 inputs and 255 outputs
- Supports **asynchronous** and **synchronous** modes
- Supports **parameter file input for each instance** (vendors can decide which parameters to access)
- All the DOTA could be the same (multi-instance) or different



DOTA component



DOTA Interface Model Configuration



DOTA instance #1 Configuration

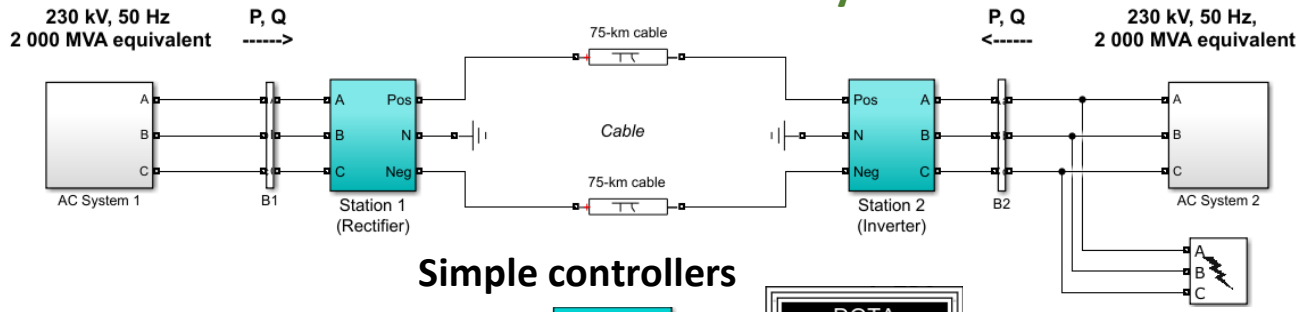
GTSOC Applications

- Renewables
  - SMA – PV and Battery
  - Vestas - Wind
  - Siemens Gamesa - Wind
- HVDC
  - GE eLumina HVDC controller
- Ongoing work with other renewable/HVDC vendors

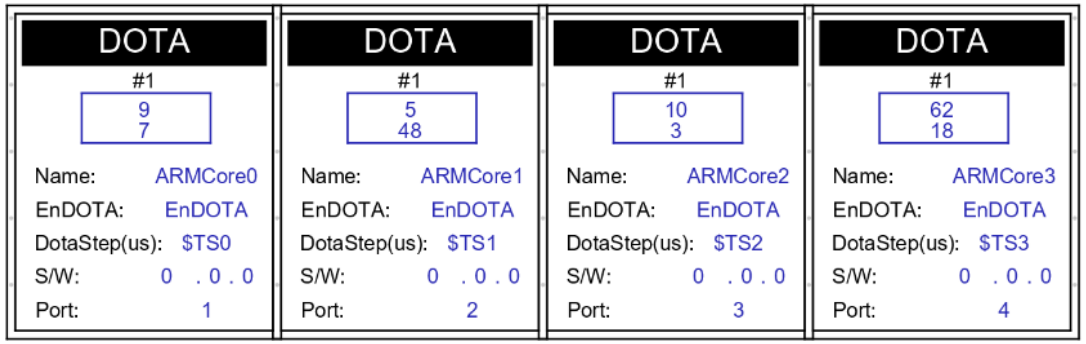
GTSOC APPLICATIONS

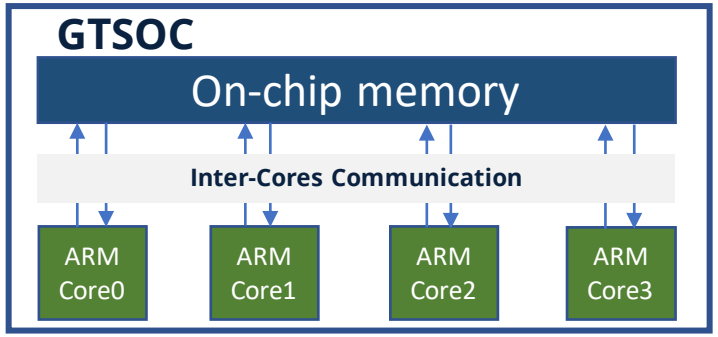
- **Simple controllers:** Implement controllers for multi-terminals in one DOTA component (One ARM core)
- **Complex controllers:** Implement controller for one terminals in multiple DOTA components (up to 4 per GTSOC board) with inter-core communication

Simulink Demo VSC-HVDC System



Complex controllers





Case Study– DFIG System

Multi-Core and Multi-Instance Testing

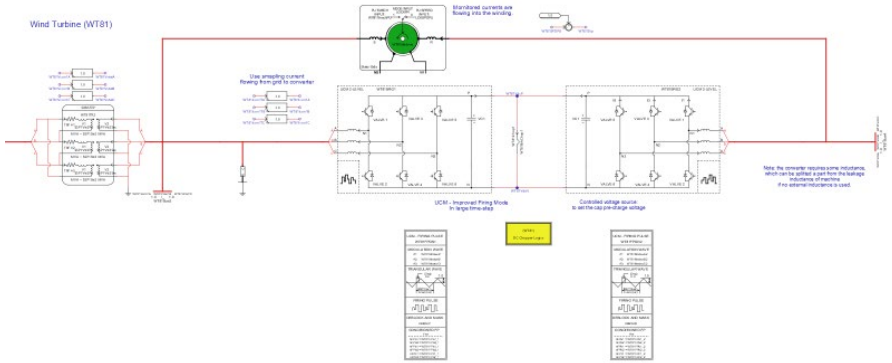
Electrical system :

21 DFIG systems, 2 AC Thevenin networks

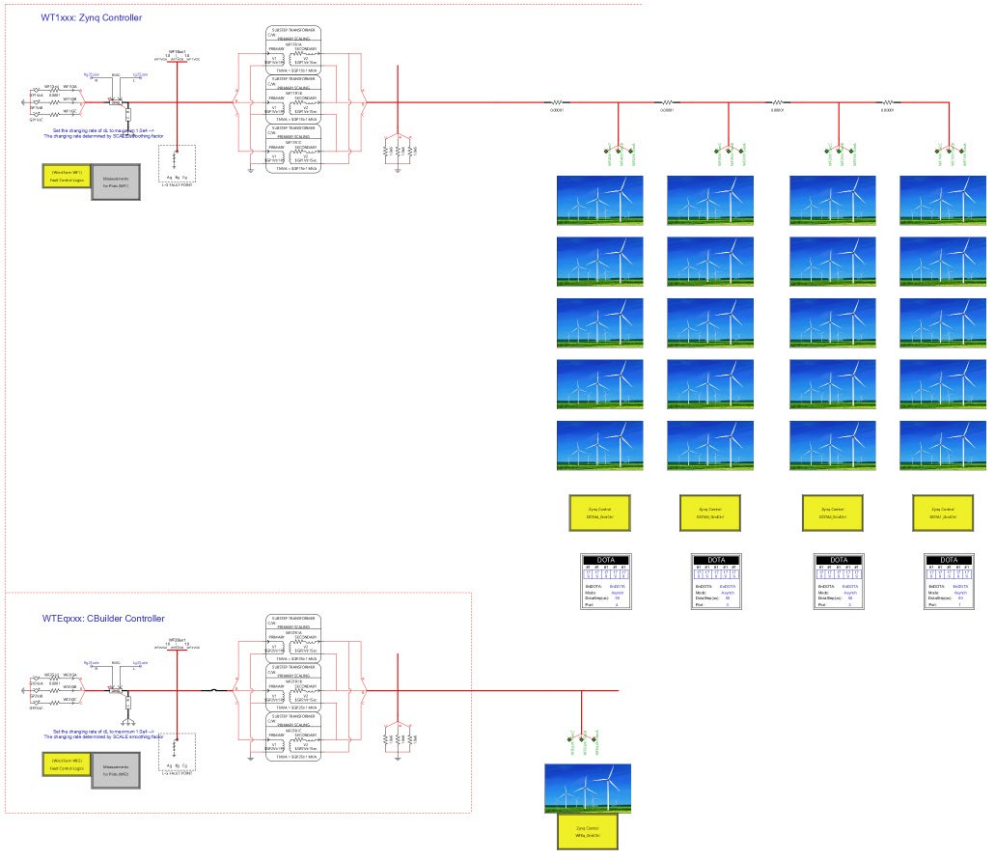
Control system:

20 DFIG controls on 4 GTSOC cores (every 5 DFIGs controls on one GTSOC core)

Four DOTA components (one per GTSOC core, each has 93 outputs and 53 inputs**)**



Single DFIG Electrical System



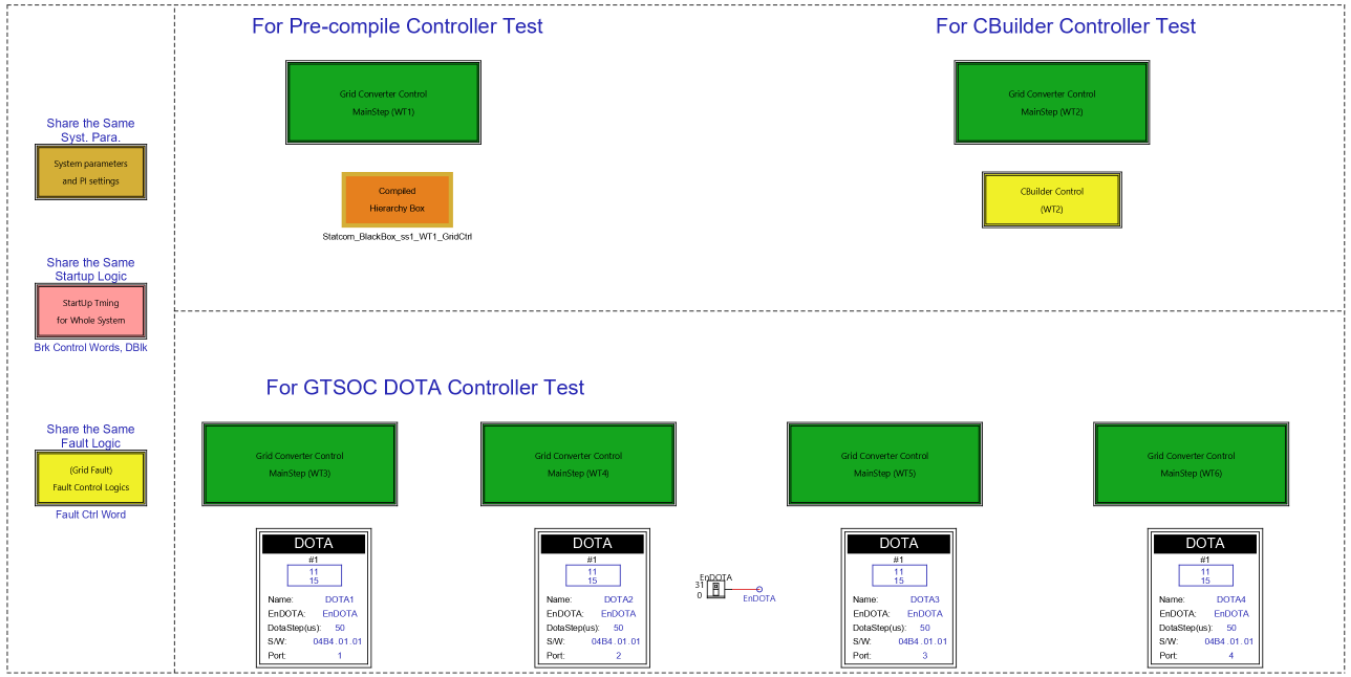
21 DFIG Electrical System

GTSOC Released Sample Case: STATCOM

– Factory Acceptance Test (FAT) case: STATCOM

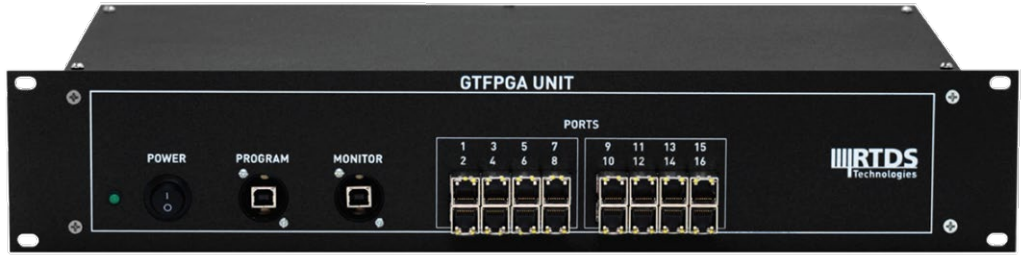
- ❖ Precompile Box
- ❖ CBuilder
- ❖ GTSOC

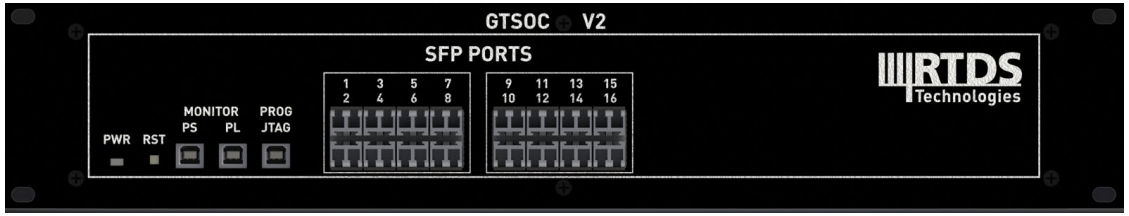
Only one NovaCor core is needed.



GTSOC V2

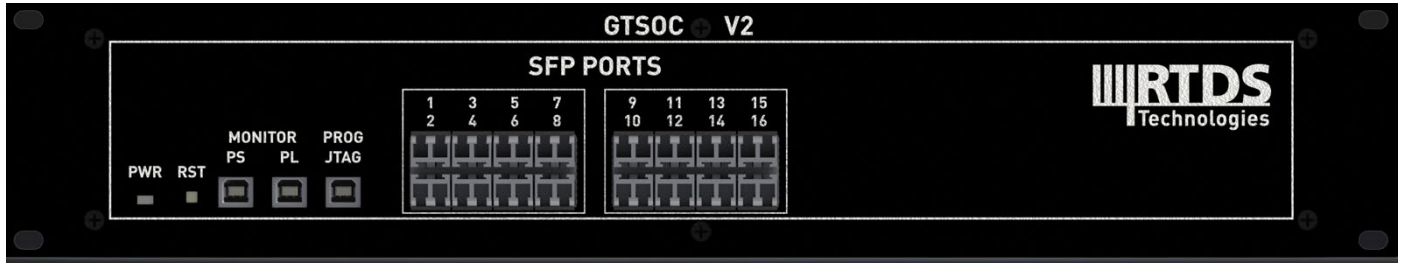
- Replaces GTSOC v1
- Replaces current GTFPGA
  - RTDS-designed board inside
  - VC707 dev boards are end of life
  - Firmwares (SV, MMC, Tline, GPES) are being ported





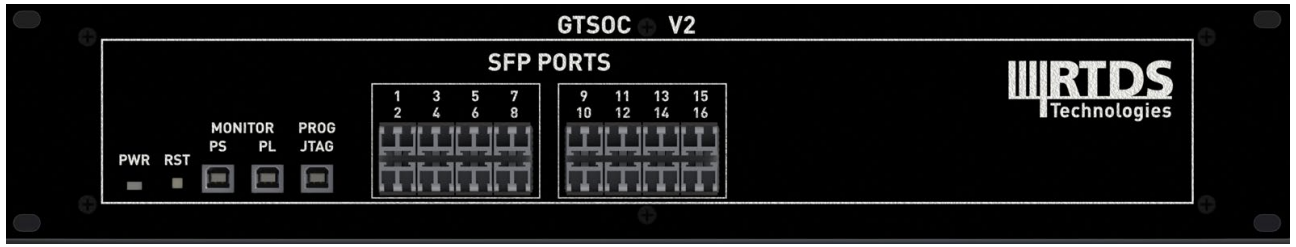
GTSOC V2 PRICING

- For GTFPGA applications, price will be the same as the existing GTFPGA
  - All firmwares will come licensed as they do now
- Price model for GTSOC applications
  - GTSOC v2 will include 1 core licensed at the same price as GTFPGA
  - Cores 2-4 will each be licensed for an additional fee
- Selling now and shipping soon



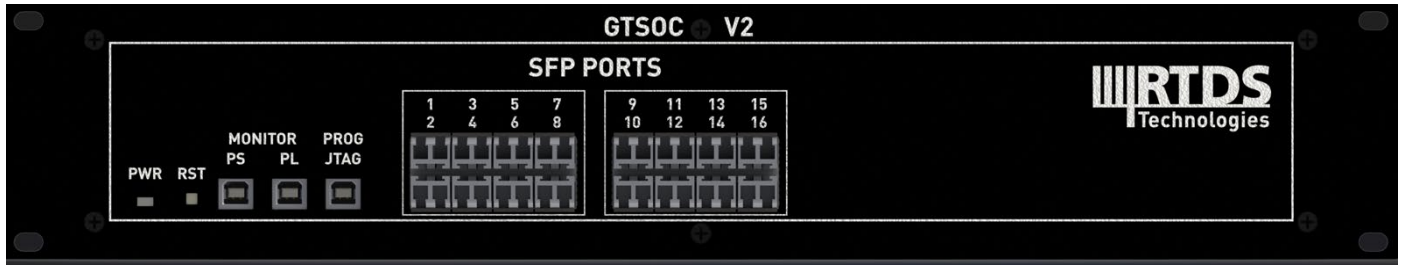
NEEDS AND CHALLENGES

- Customers who are doing HIL testing and need an accurate model of a controller that they cannot get physical access to:
  - HVDC HIL testing has and will continue to be done. Customers want a more accurate model of the wind generation so that can be done with GTSOC
  - HVDC vendors can get started on their projects and provide (simplified) models to their customers earlier without needing to wait to build up control hardware
  - Protective relay testing for large installations of renewables must be done and having a good model of the vendor controls for the renewables can be critical to ensure correct relay operation



NEEDS AND CHALLENGES

- Consider the study: a GTSOC model will never be as detailed as control hardware
- Existing PSCAD DLL models CANNOT be converted to be used with GTSOC
- We see a future where a GTSOC model is provided with documentation and RSCAD case in the same way a DLL model is currently in PSCAD
- RSCAD and an RTDS Simulator are not needed to create the models but are useful for benchmarking.



QUESTIONS?