A MODULAR HARDWARE-IN-THE-LOOP TESTBENCH FOR THE INVESTIGATION OF CONVERTER CONTROL INTERACTIONS AND INTEROPERABILITY

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2023 EUROPEAN RTDS TECHNOLOGIES INC. USER'S GROUP MEETING 2023

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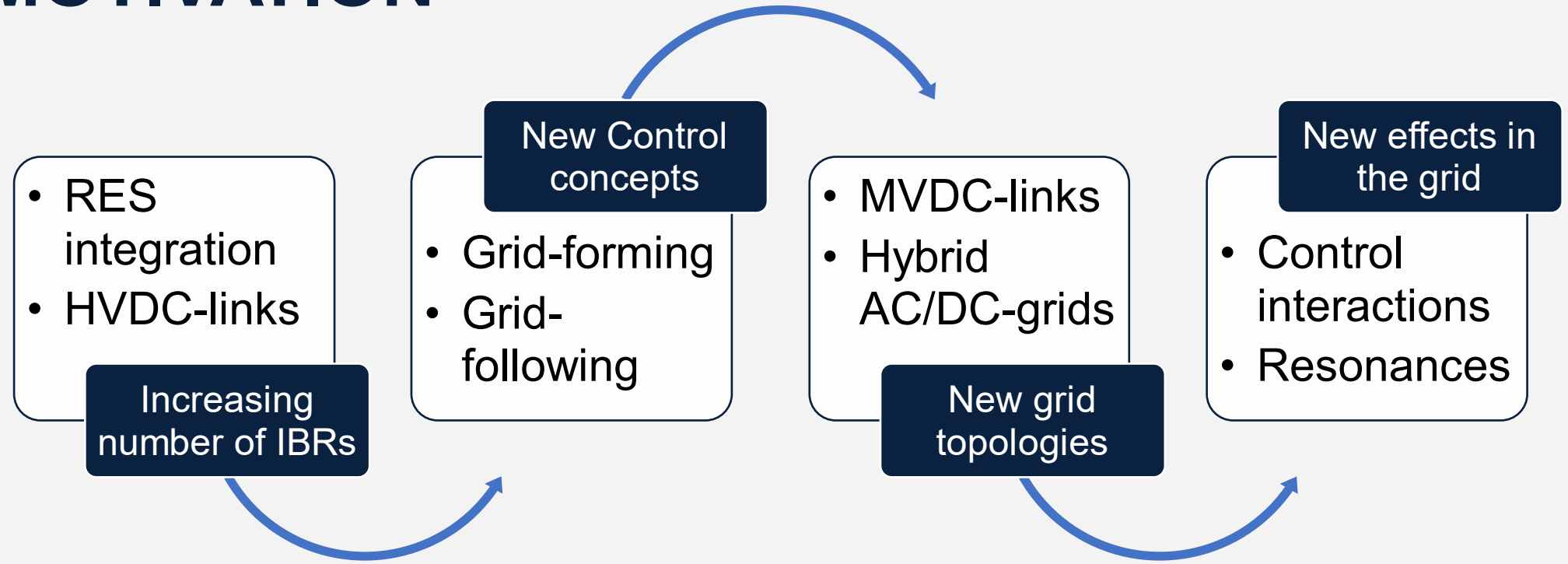
AGENDA

1. Motivation
2. System overview
3. IBR modelling and implemented control schemes
4. Integration of time-varying resources
5. Hardware resources
6. Operation of the testbench
7. Conclusions

MOTIVATION



➔Development of a testbench within the project Kopernikus ENSURE

KOPERNIKUS PROJEKTE
ENSURE
Die Zukunft unserer Energie

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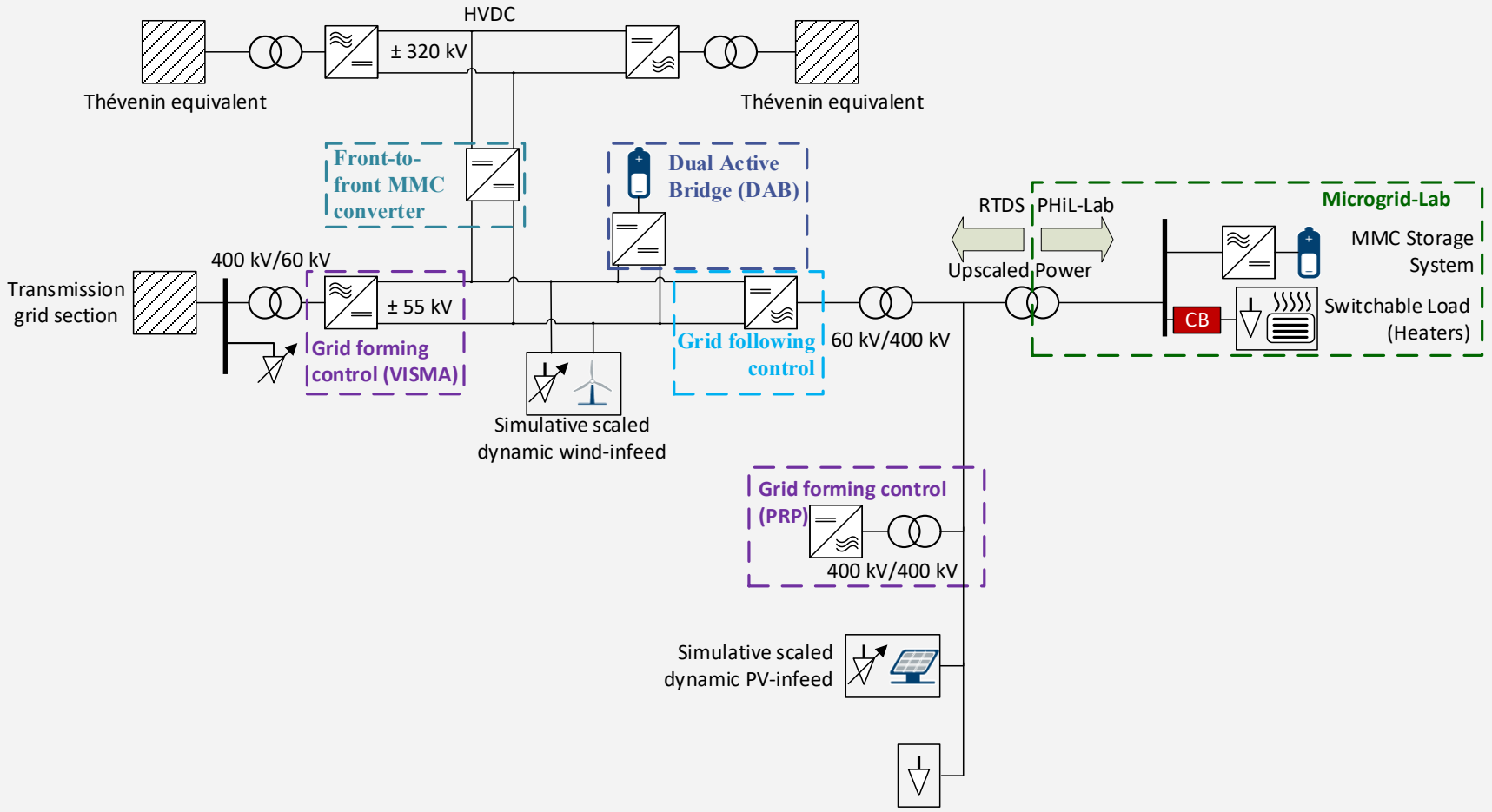
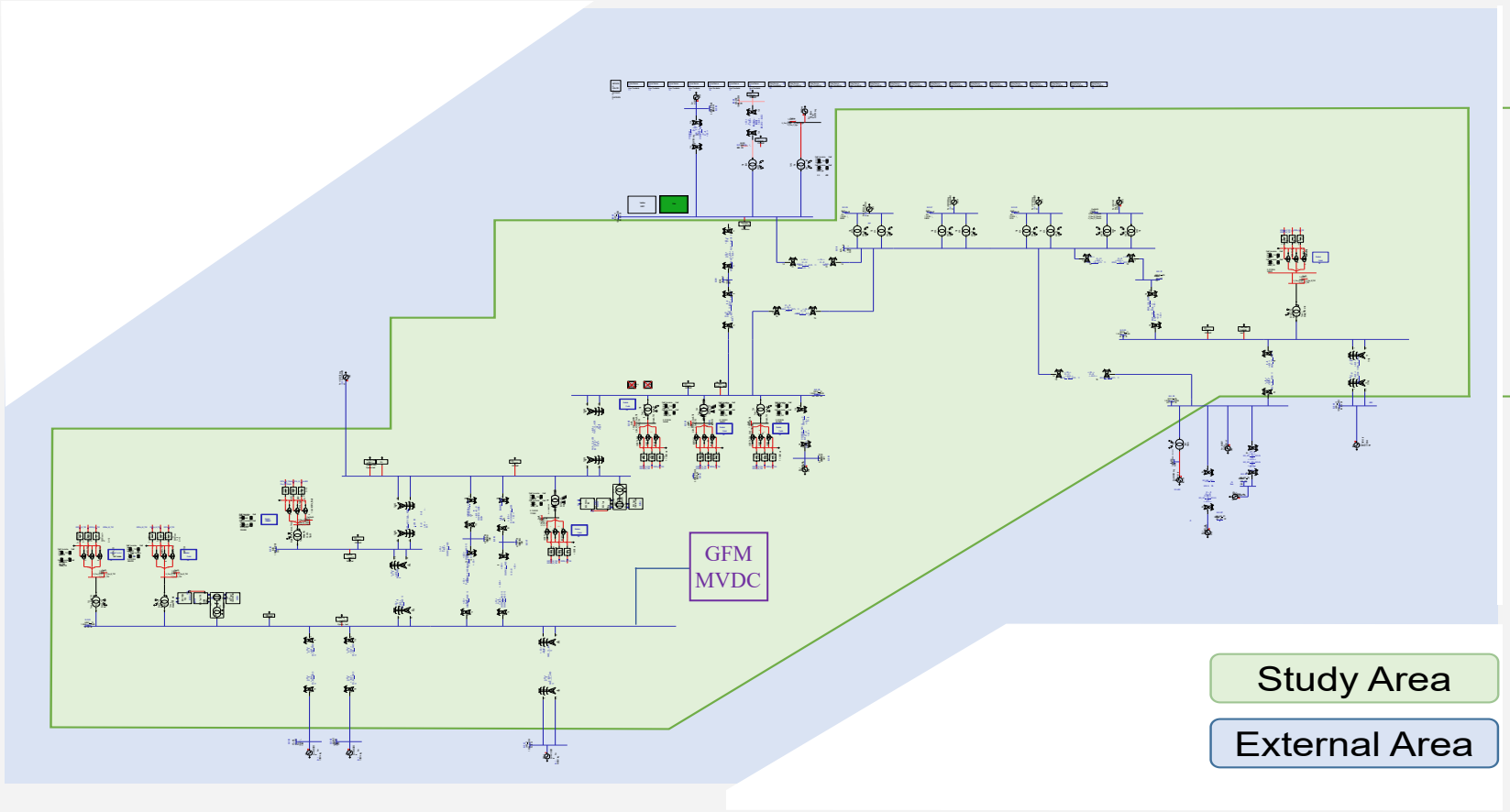
SYSTEM OVERVIEW

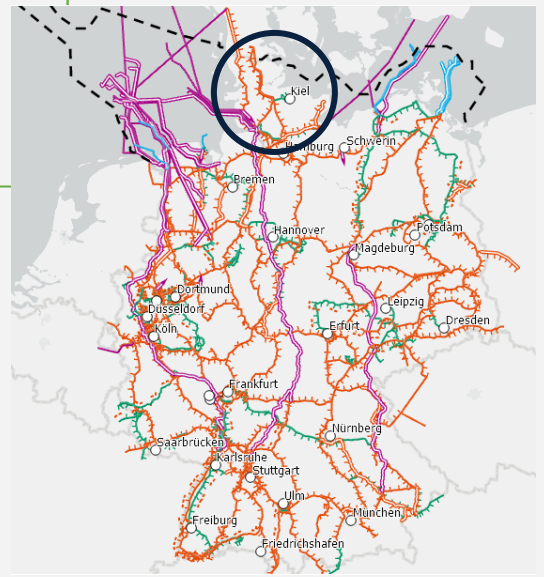
MVDC/HVDC Testbench



SYSTEM OVERVIEW

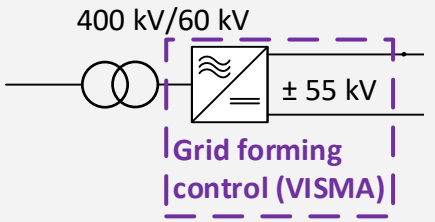
Transmission grid section





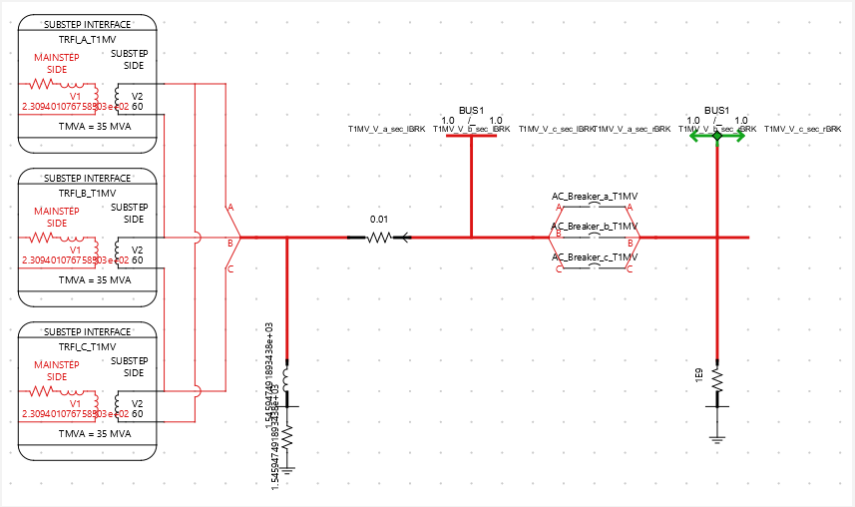
Reference: VDE

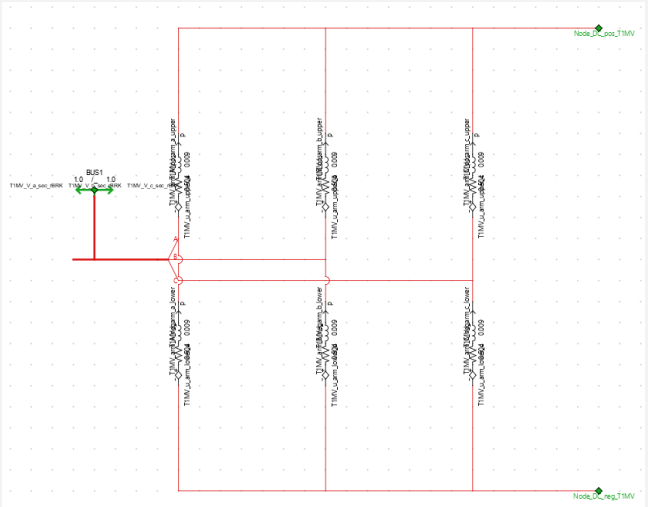
IBR MODELLING AND IMPLEMENTED CONTROL SCHEMES

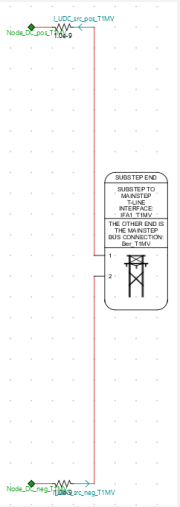


MVDC head stations – VISMA

- Transformer as AC substep interface
- MMC average model
- Tline substep interface on DC-side







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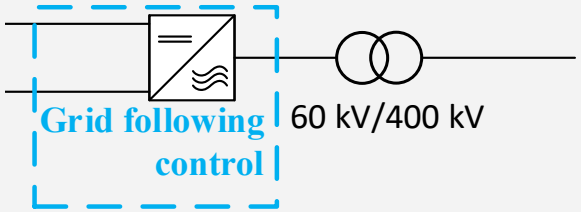
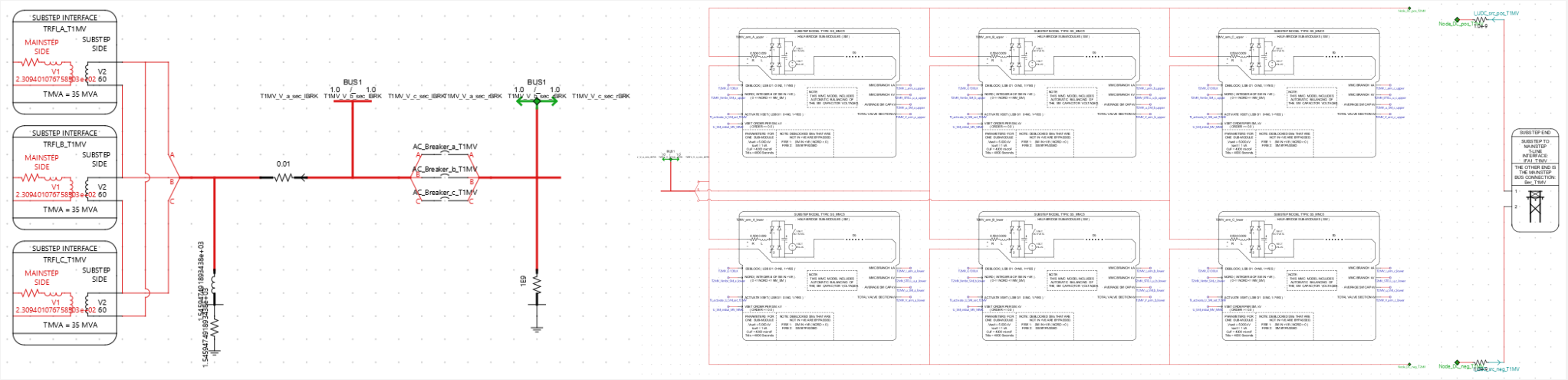


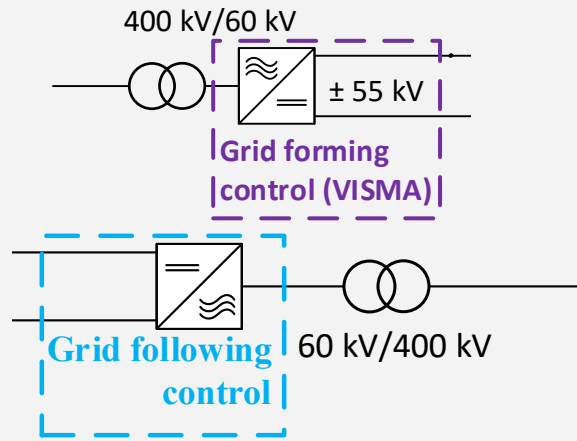
MVDC head stations – Grid following control

- Transformer as AC substep interface
- MMC5 model
- Tline substep interface on DC-side

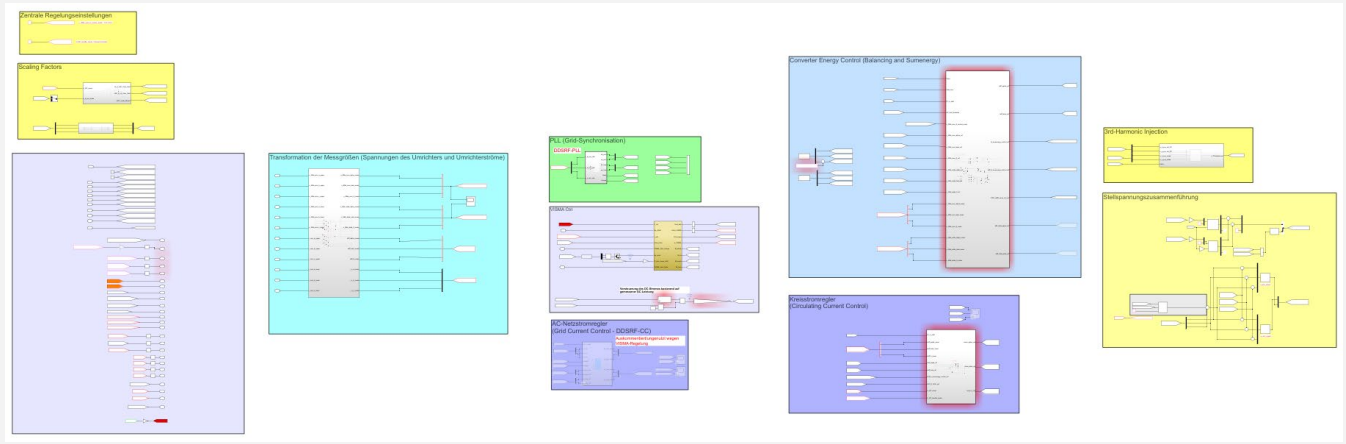


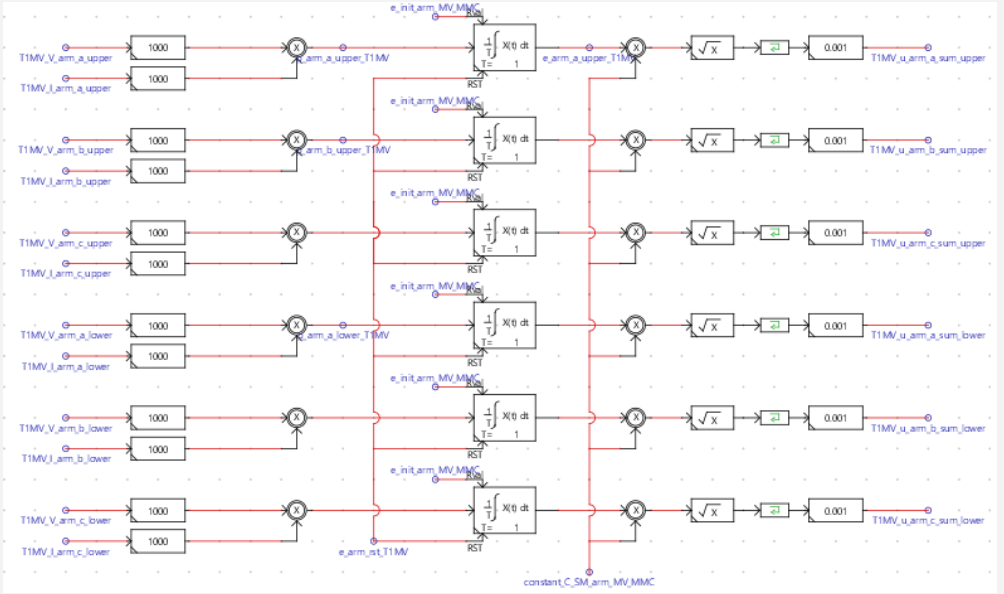
IBR MODELLING AND IMPLEMENTED CONTROL SCHEMES

MVDC head stations – Control integration



- Control development in Matlab/Simulink
- Build control as C-Code
- Calculations with draft variables in RSCAD





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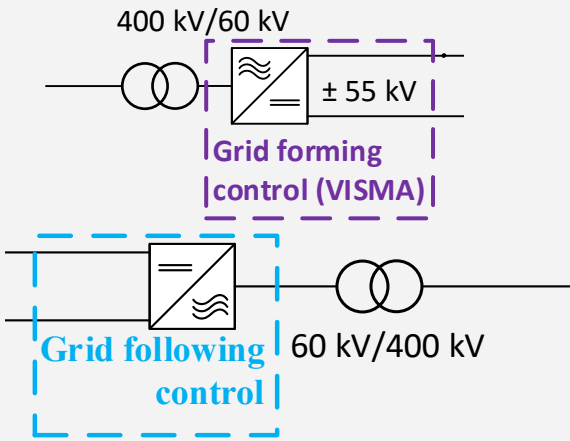
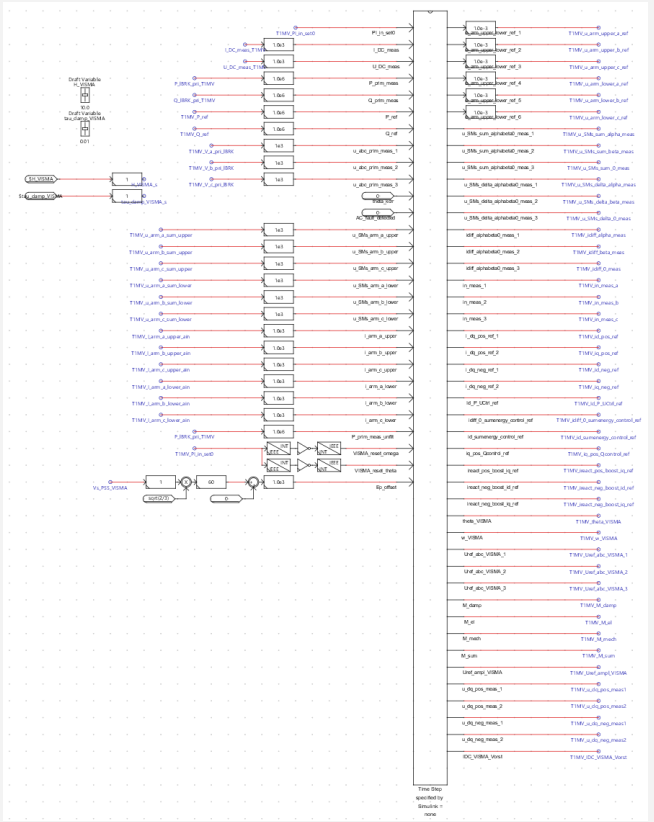


- Import C-Code as block in RSCAD
- Enter values in block mask

CtrlGrp	Assigned Controls Group	1		1	36
Pri	Priority Level	479		1	
Balancing_Ctrl_Activate_m		1.0			
Bool_P_Vorst_VISMA_m		1.0			
H_VISMA_m		$H_VISMA			
Kp_DDSRFPLL_m		229.99999999999997			
Kp_diff_CControl_m		23.80952380952381			
Kp_diff_CControl_circulating_m		18.828451882845187			
Kp_uhor_m		0.0087818181818181823			
Kp_usum_m		0.009859196214702293			
Kp_uvert_m		0.0049295981073511465			



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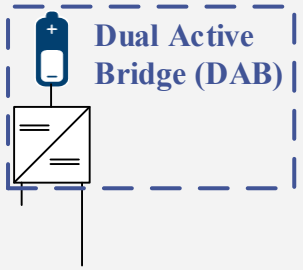
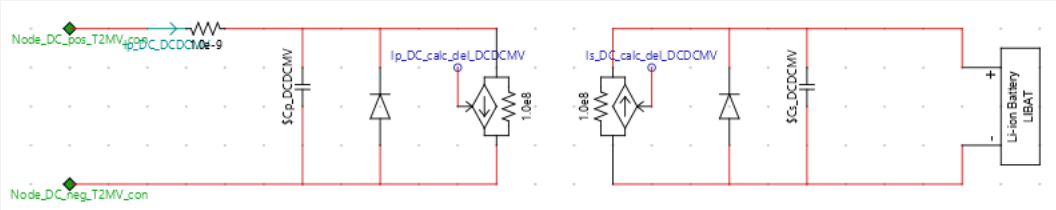
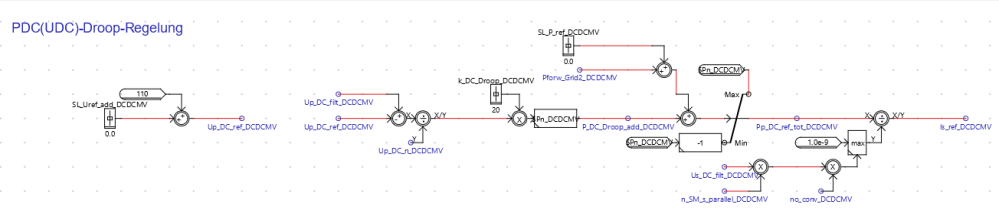


DC/DC converter – Dual Active Bridge

- Emulate the current behavior of a DAB in controlled current sources
- Average model
- Control implemented from literature directly in RSCAD





Reference:
S. P. Engel, N. Soltau, H. Stagge, and R. W. de Doncker, “Dynamic and Balanced Control of Three-Phase High-Power Dual-Active Bridge DC–DC Converters in DC-Grid Applications,”, 2013, doi: 10.1109/TPEL.2012.2209461

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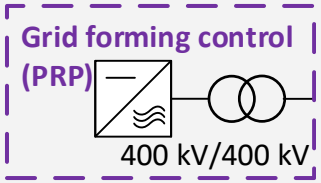
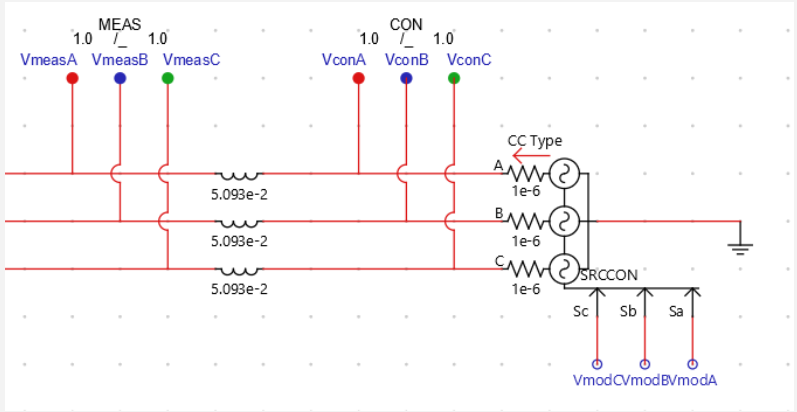
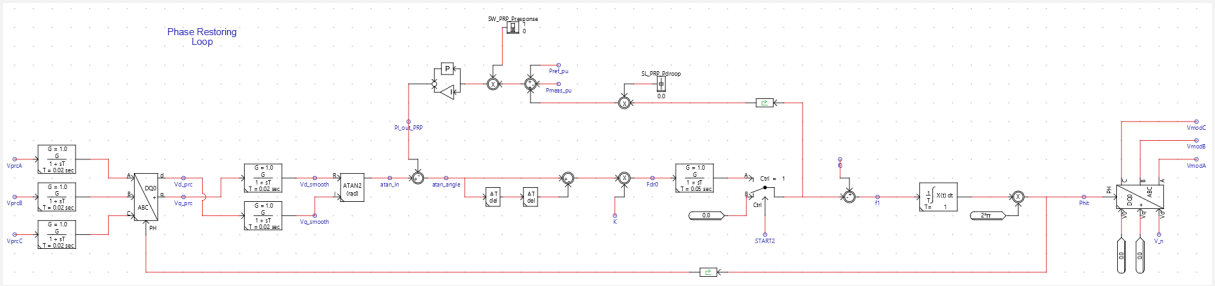


New control concept – Phase Restoring Principle

- Implemented in mainstep with controlled voltage sources and inductors
- Average model
- Control directly implemented in RSCAD

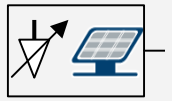




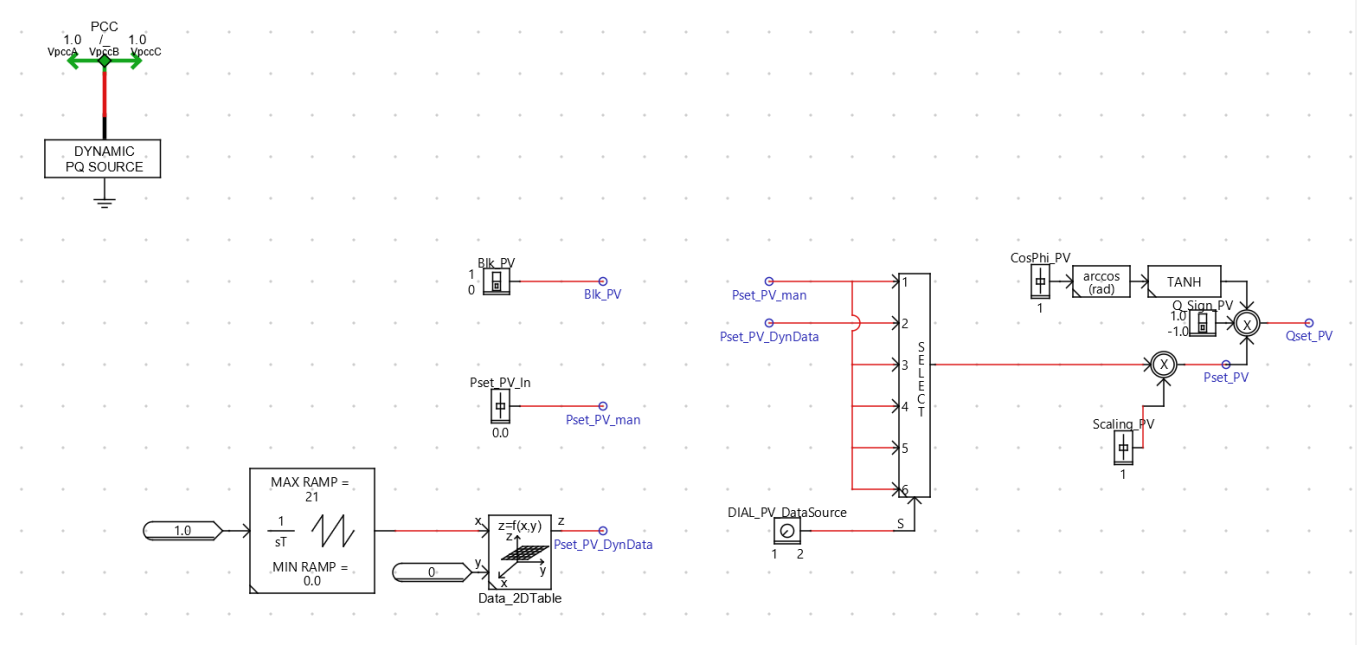
Reference:
A. Kuri, R. Zurowski, G. Mehlmann, D. Audring, and M. Luther, "A Novel Grid Forming Control Scheme Revealing a True Inertia Principle," 2021, doi: 10.1109/TPWRS.2021.3071126

INTEGRATION OF TIME-VARYING RESOURCES

Simulative scaled PV-infeed

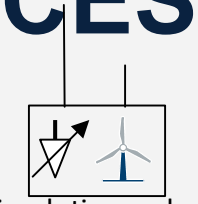
Simulative scaled dynamic PV-infeed 

- Implemented as dynamic PQ source
- Option to either use sliders or predefined dynamic data as input
- Predefined dynamic data:
  - Logged data of the institute‘s PV plant for real world scenario
  - 21 hour period compressed to 21 second period
  - 17 kWp PV plant scaled for transmission grid application



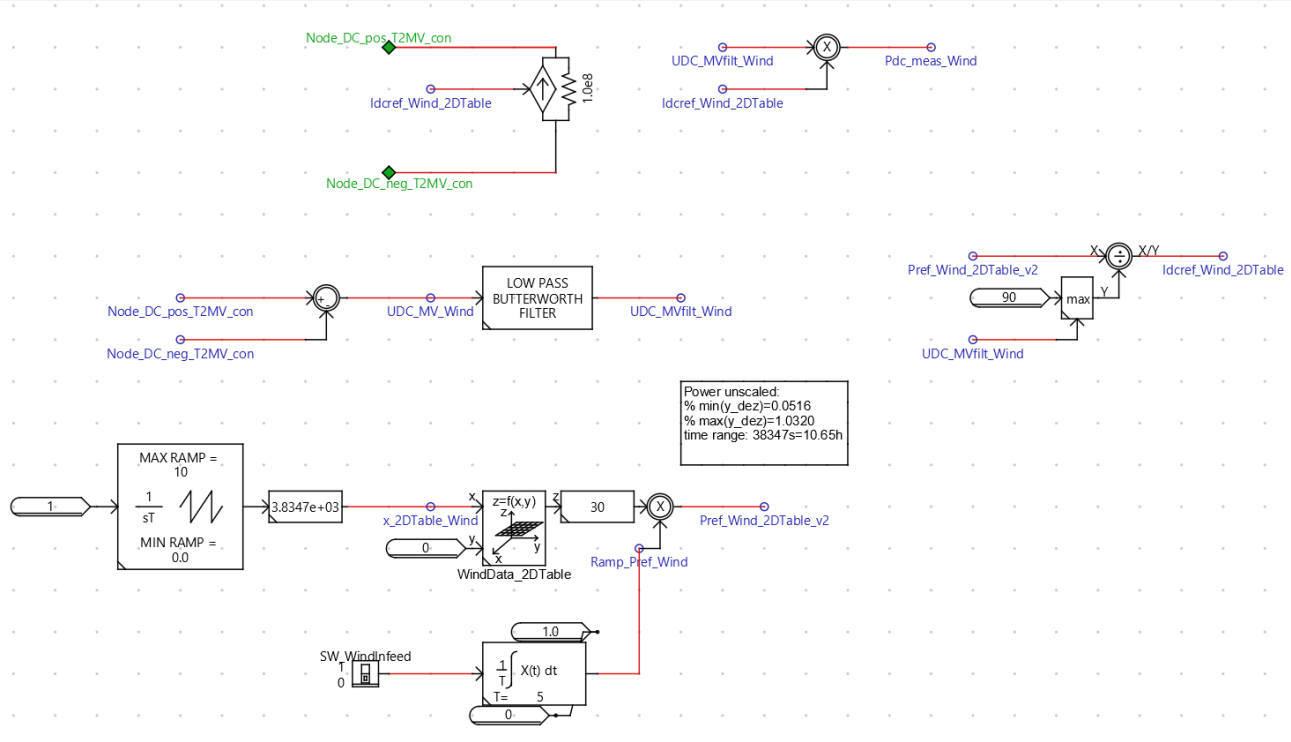
INTEGRATION OF TIME-VARYING RESOURCES

Simulative scaled wind-infeed



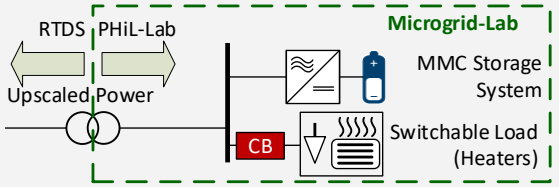
Simulative scaled dynamic wind-infeed

- Implemented as controlled current source
- Predefined dynamic data as input:
  - Typical wind profile for onshore Germany
  - 10 hour period compressed to 10 second period
  - Wind profile scaled for transmission grid application

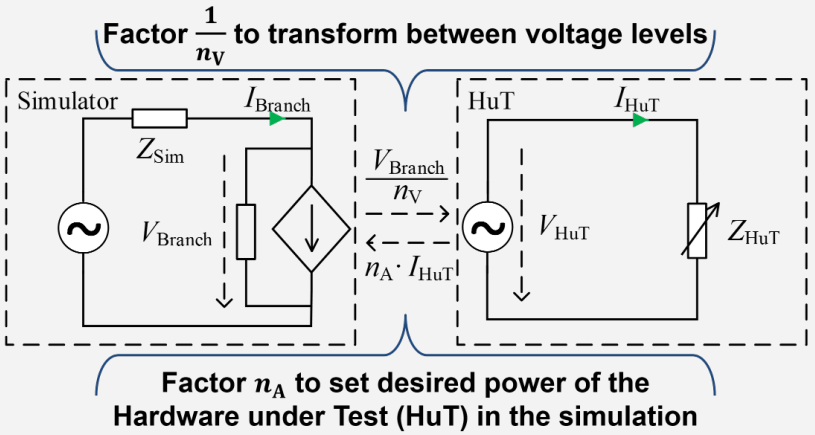


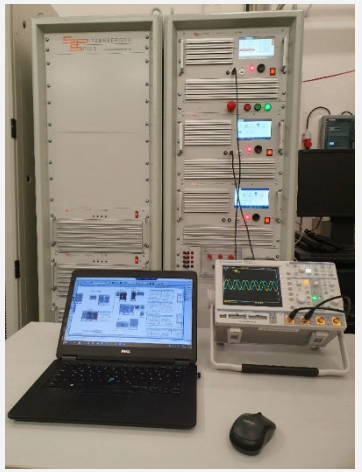
INTEGRATION OF TIME-VARYING RESOURCES

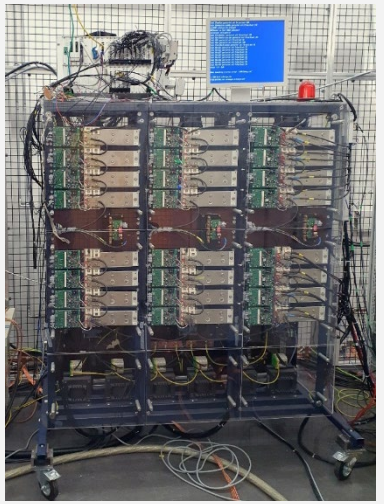
PHiL connection to the Microgrid-Lab



- Enhanced Ideal Transformer Interface to connect LV Microgrid-Lab to simulated Transmission voltage
- So far MMC storage system and switchable loads used as hardware





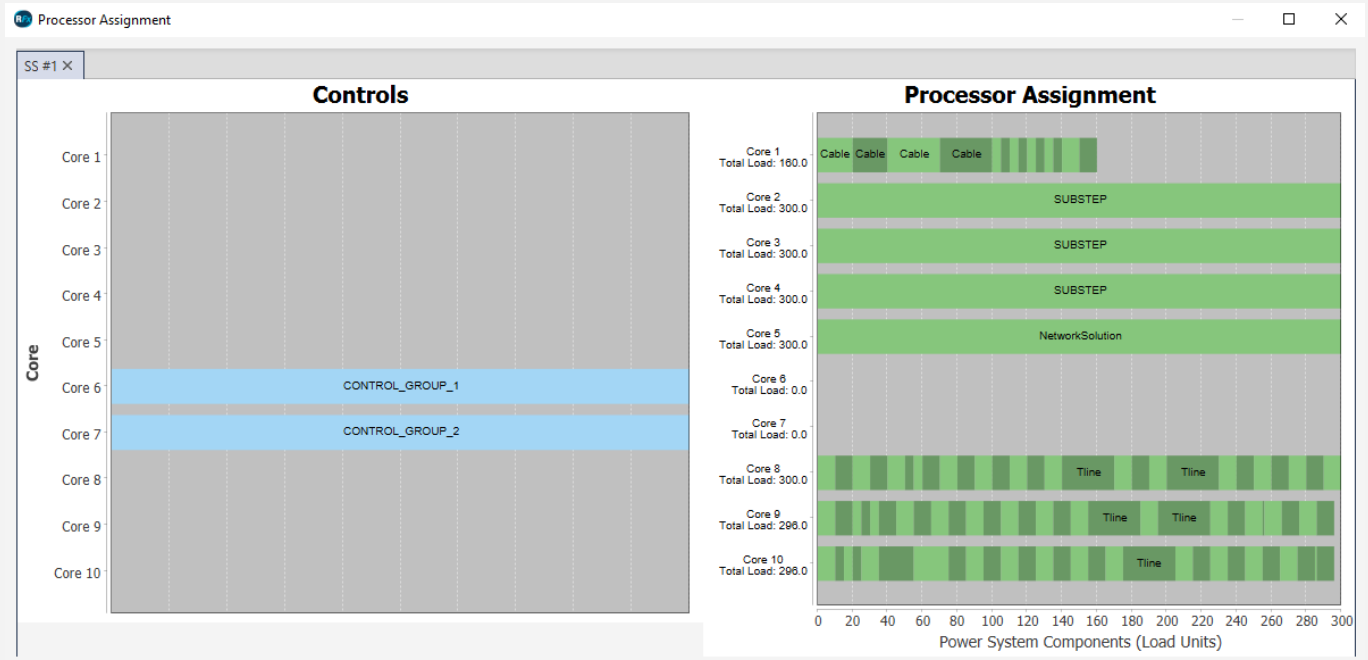


Reference:
J. Richter, S. Resch, G. Mehlmann and M. Luther, "An Enhanced Ideal Transformer Method to Integrate Low-Voltage Power Hardware in Arbitrary Voltage Levels," 2023 IEEE PES General Meeting, 2023

HARDWARE RESOURCES

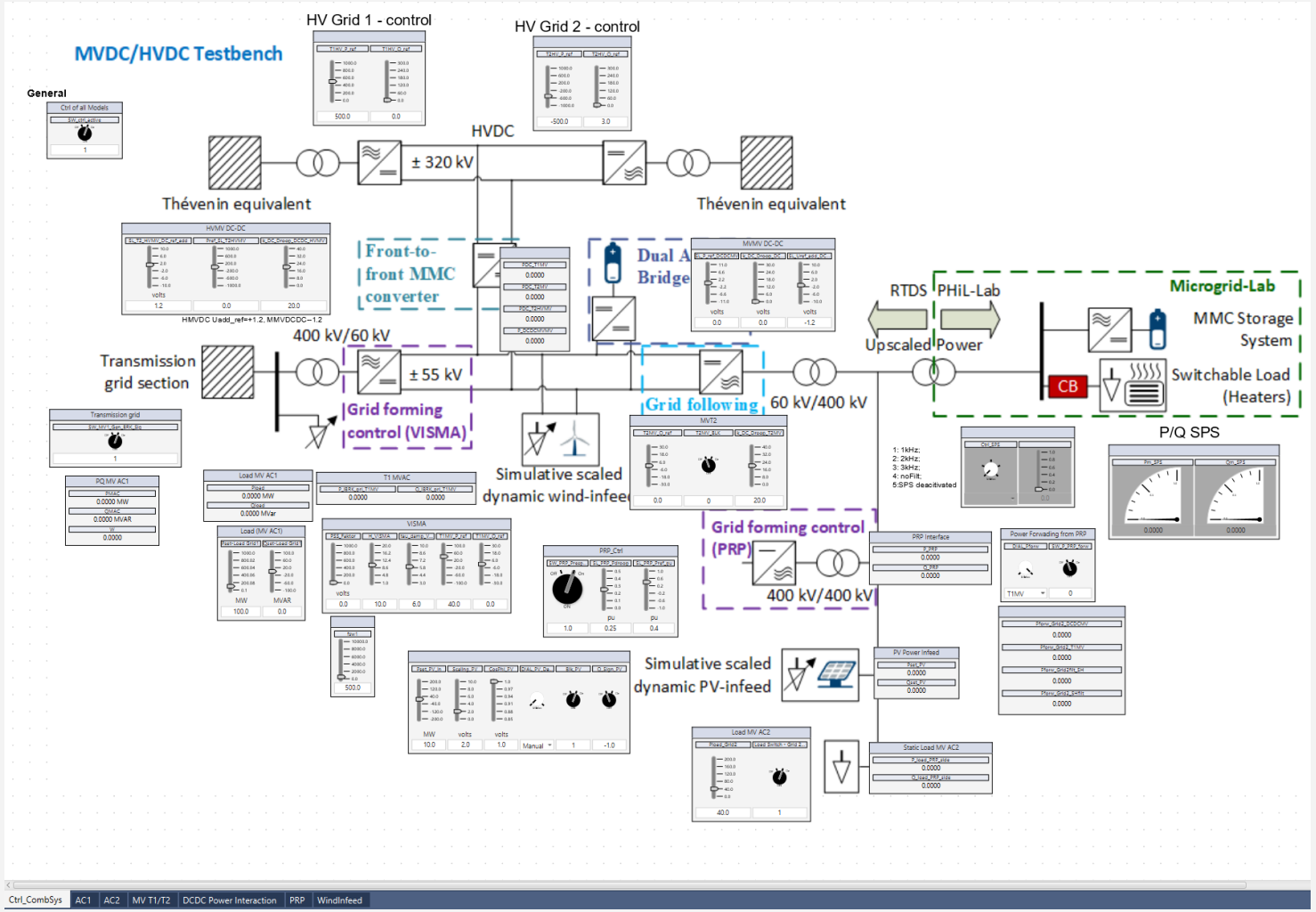
Core allocation

- The entire system can be simulated on one rack
- In order to integrate further components into the testbench, the overall system can be partitioned and simulated on two racks



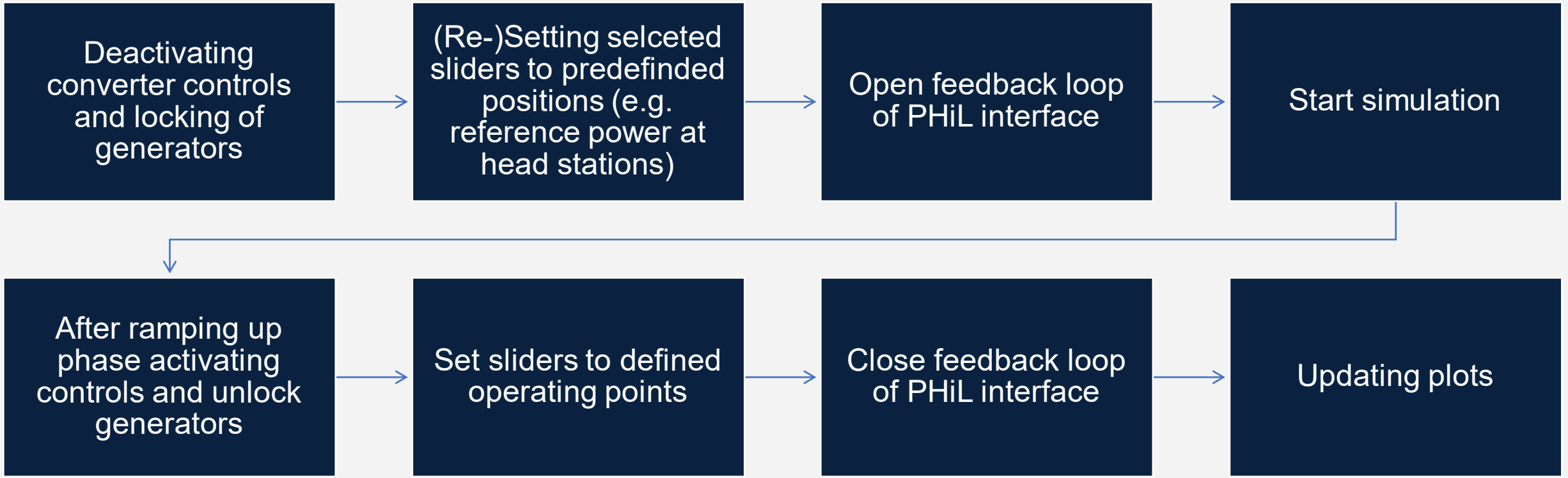
OPERATION OF THE TESTBENCH

Runtime



OPERATION OF THE TESTBENCH

Startup script



CONCLUSIONS