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REDUCED-HARDWARE PHIL FOR REAL-TIME TESTING OF BESS

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2023 EUROPEAN RTDS TECHNOLOGIES INC. USER'S GROUP MEETING 2023

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RTDS Technologies AMETEK

OVERVIEW

- Introduction
- COSTORE Project
- Proposed Reduced Hardware PHIL
- Case Study
  - Loop Delay
  - Performance
  - Loop Stability
- Wind Power Smoothing PHIL
- Conclusions

INTRODUCTION

- Significant efforts across the globe to increase the share of renewable energy sources (RES) on power networks
  - more environmentally sustainable
  - introduce important challenges
    - intermittent and non dispatchable nature affect the reliability of the network
    - excessive generation leads to reverse power flows which may cause voltage violations
- Battery Energy Storage Systems (BESS) increasingly seen as viable solution
  - numerous applications on distribution networks
  - can enhance the stability and reliability of renewable energy generation
  - however requires
    - substantial investment cost

COSTORE PROJECT

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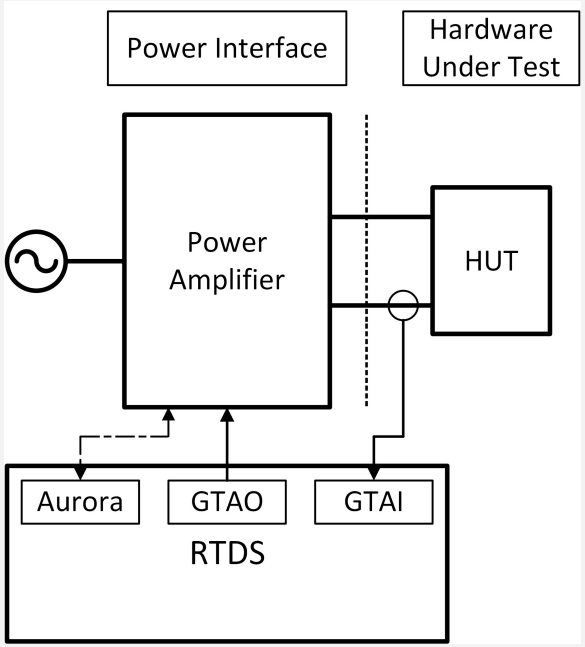
- Coordinated energy storage for low carbon power networks
- Objectives
  - development of optimisation routines for BESS sizing and location
  - study of interaction with other controllable network components
  - examination of BESS operation and control through PHIL simulation
  - evaluation of potential low-carbon scenarios through RTDS

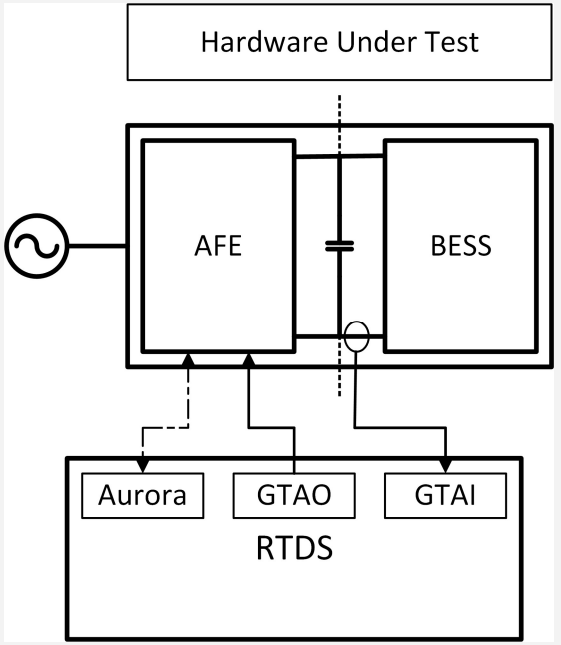
PHIL SIMULATION

- Conventional system
  - power system modelled in RTDS
  - power amplifier to provide power interface to HuT
  - analog or digital communication links
  - feedback of HuT response to RTDS
- Power Amplifier requirements
  - 4 quadrant capability for bidirectional power flow
  - fast dynamics to minimise delay



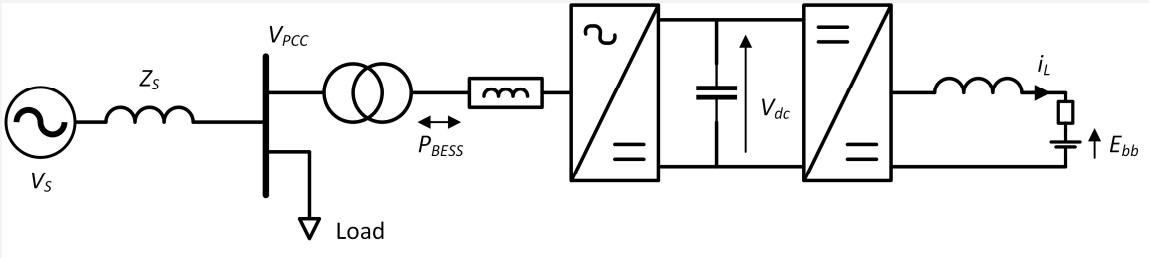
PROPOSED REDUCED HARDWARE PHIL

- AFE used to interface BESS to grid
  - bidirectional power flow capability
  - fast dynamics so as not to affect battery response
  - can be used to perform the duty of power amplifier
- Pros
  - reduced hardware
  - known configuration
- Cons
  - does not allow test of grid-side dynamics



CASE STUDY

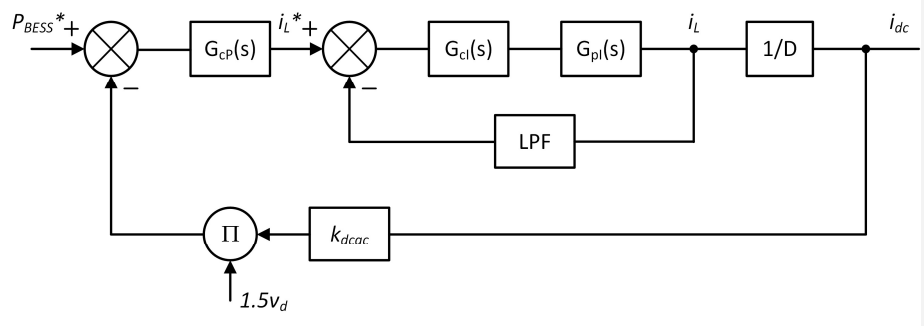
- 2MVA, 0.55kV
- Battery Bank
  - 12S 65P 51.2V 50Ah units
    - E_{bb} = 614.4V, R_{bb} = 0.011Ω[1]
- Control loops
  - AFE
    - synchronised to grid via PLL
    - conventional vector control
      - V_{dc} loop, bandwidth ≈ 30Hz
  - Bidirectional DC DC Converter
    - inner current loop, bandwidth ≈ 200Hz
    - outer P_{BESS} loop, bandwidth ≈ 3Hz



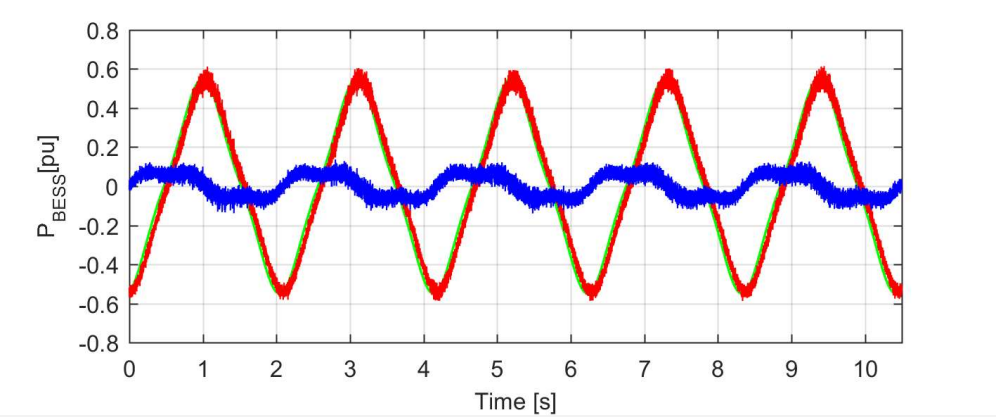
[1] D. Ansean et al., "DC internal resistance during charge: analysis and study on $LiFEPO_4$ batteries," in 2013 World Electric Vehicle Symposium and Exhibition (EVS27), Barcelona, Spain, 2013.

CASE STUDY

- P_{BESS}* set to
  - 1MW 3 rad/s reference with 10% 3rd harmonic distortion

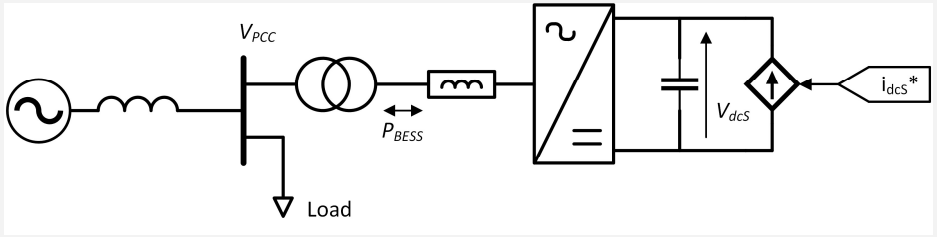


Cascaded control loop schematic for P_{BESS}

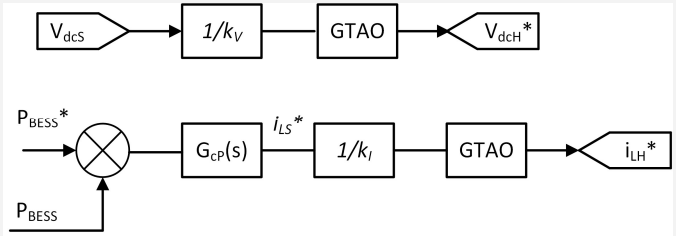


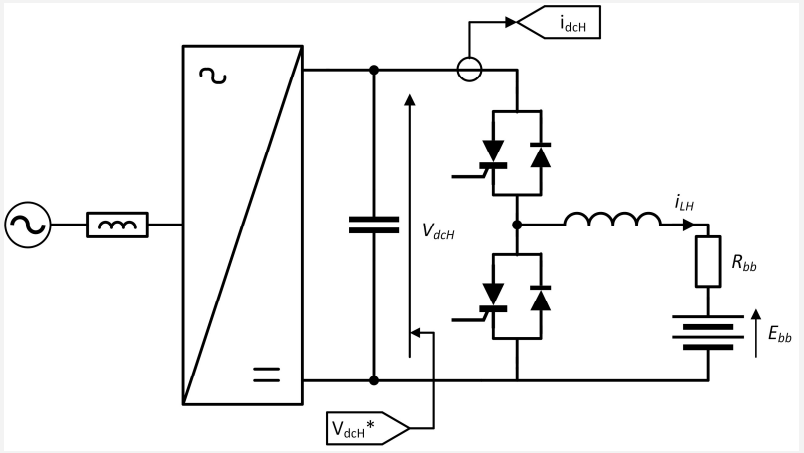
P_{BESS}* (green), P_{BESS} (red) and error (blue)

PROPOSED PHIL



RTDS Model

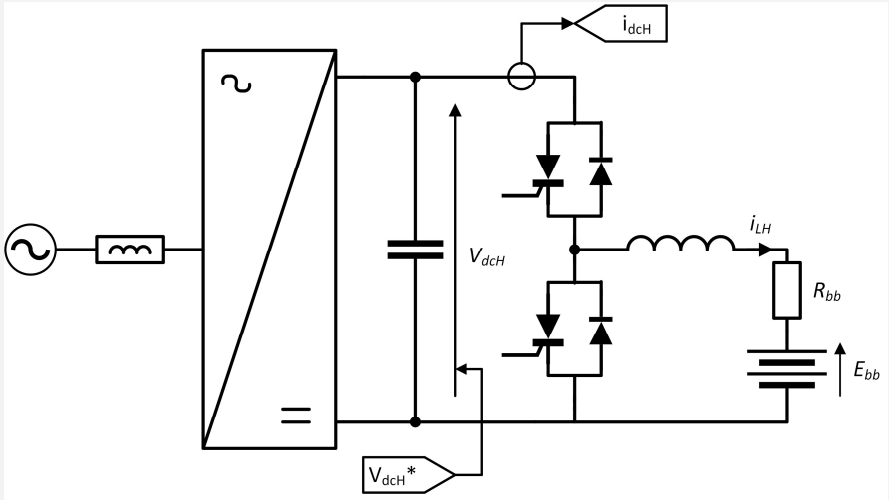




Reduced-scale hardware

HARDWARE SETUP

- 30kVA, 0.275kV
- Battery bank:
  - 6S 2P 51.2V 50Ah units
    - E_{bb} = 307.2V, R_{bb} = 0.1786Ω
- Control loops
  - same BWs as actual system
- Scaling factors
  - k_V = 2
  - k_I = 33.33



Reduced-scale hardware

LOOP DELAY

- Component time delays
  - RTDS platform
    - $T_{RTDS} = \tau_{sS}$
  - Communication delays
    - assume analog channels
      - T_{comSH} (software – hardware): GTAO card
      - T_{comHS} (hardware – software): transducer, filters and GTAI card
      - $T_{com} = T_{comSH} + T_{comHS}$
  - Power interface
    - $T_{PI} \approx 2\,\tau_{sH}$ [2]
  - Filters introduced in the loop: T_{filt}
- Loop delay
  - $T_{dloop} = T_{RTDS} + T_{com} + T_{PI} + T_{filt}$

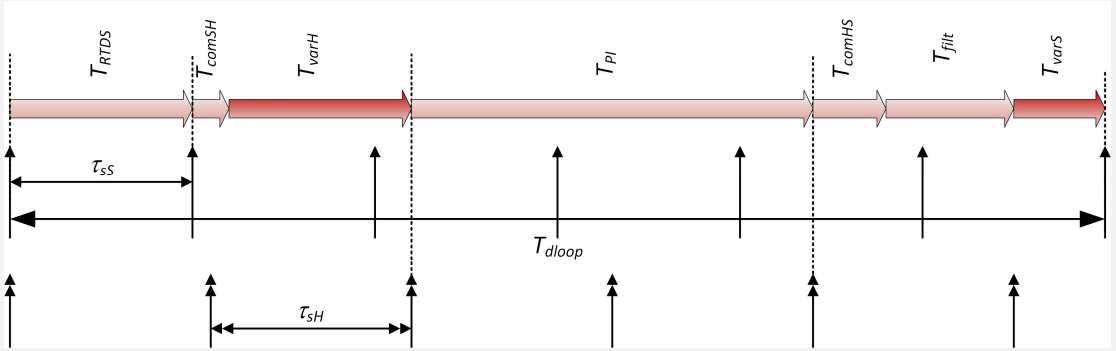
Nomenclature:

d	delay
s	sampling
S	software
H	hardware
τ_s	timestep

[2] M. Zarif and M. Monfared, "Step-by-step design and tuning of VOC control loops for grid connected rectifiers," Electrical Power and Energy Systems, vol. 64, pp. 708-713, 2015.

LOOP DELAY

- Loop delay also depends on interaction between two digital systems[3]
  - RTDS and switched power converter
- Both digital systems sample data once per cycle (τ_{sS} and τ_{sH})
  - sampling time synchronous with timestep
    - Power Interface: $K_H\tau_{sH}$
    - RTDS: $K_S\tau_{sS}$
  - can lead to variable delays
    - sampling by power converter
      - $T_{dvarH} = [0, \tau_{sH}]$
    - sampling by RTDS
      - $T_{dvarS} = [0, \tau_{sS}]$



[3] E. Guillo-Sansano et al., "Characterisation of Time Delay in Power Hardware in the Loop Setups," IEEE Trans. Industrial Electronics, vol. 68, no. 3, pp. 2703-2713, 2021.

SETTING OF TIMESTEPS

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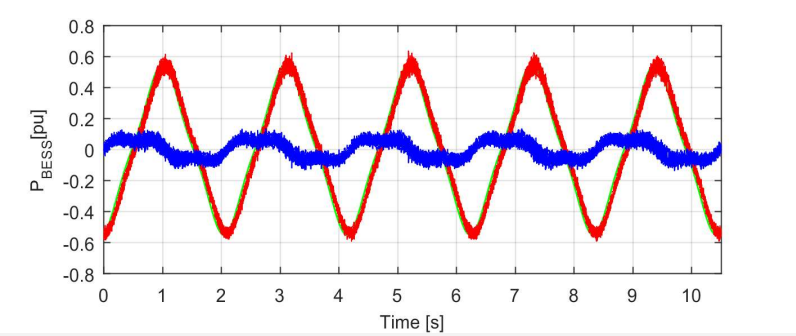
- Due to variable time delays, number of τ_{sS} cycles for PHIL loop varies between [K_{s_min}, K_{s_max}]
  - $K_{s\_min} = ceil\left(\frac{T_{RTDS}+T_{com}+T_{PI}+T_{filt}}{\tau_{sS}}\right)$ $K_{s\_max} = ceil\left(\frac{T_{RTDS}+T_{com}+T_{PI}+T_{filt}+\tau_{sH}}{\tau_{sS}}\right)$
- Time delay calculations
  - assume analog signal of 5V peak with frequency of 3 rad/s
    - $T_{comSH} \approx 4\mu s$, $T_{comHS} \approx 18.6\mu s$
    - $T_{filt} = 400\mu s$
- Timesteps
  - $\tau_{sS} = 50\mu s$
  - 3 τ_{sH} values considered & compared:
    - 40µs, 50µs and 60µs

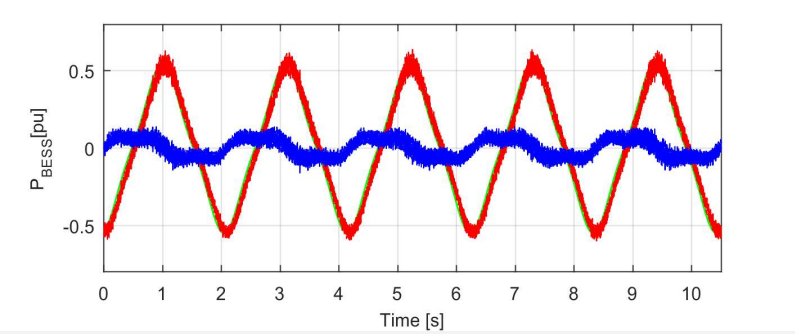
Case	τ_{sS}	τ_{sH}	K_{s_min}	K_{s_max}	Delay
1	50µs	40µs	12	12	[600µs]
2	50µs	50µs	12	13	[600µs, 650µs]
3	50µs	60µs	12	14	[600µs, 700µs]

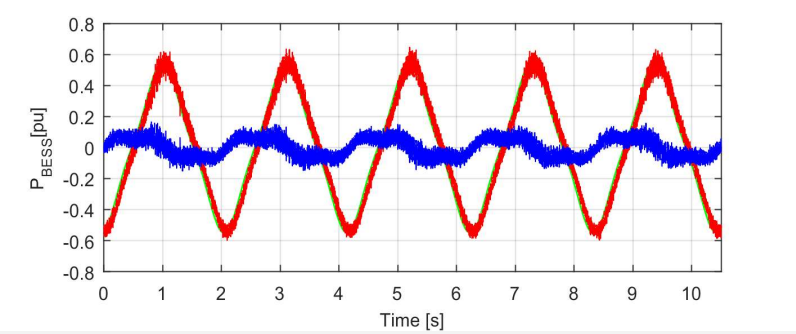
PERFORMANCE

- Case 1: 50µs, 40µs



- Case 2: 50µs, 50µs



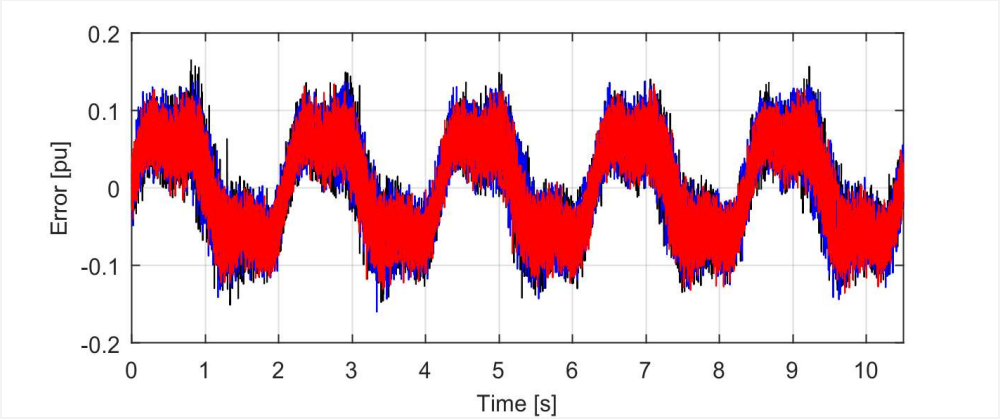


P_{BESS}* (green), P_{BESS} (red) and error (blue)

- Case 3: 50µs, 60µs

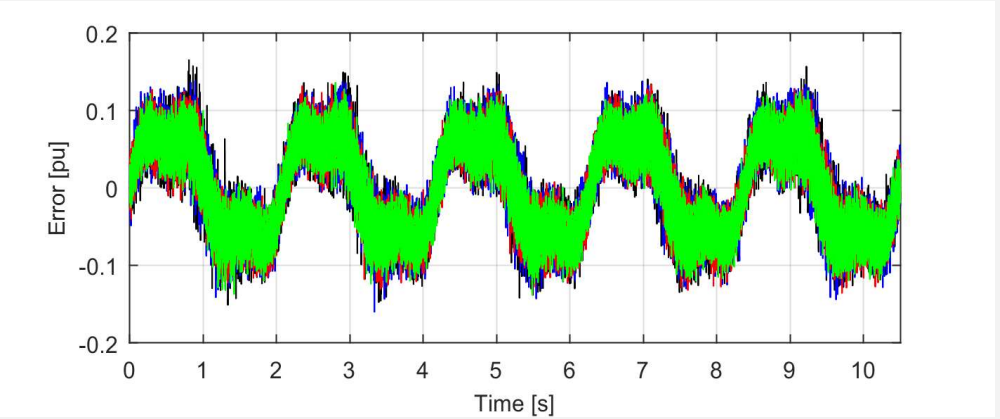
PERFORMANCE COMPARISON

- PHIL Cases 1-3



Case 1 (red), Case 2 (blue) and Case 3 (red)

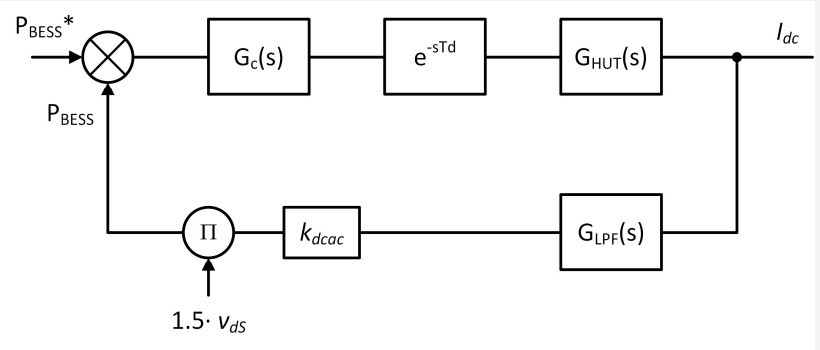
- with Actual



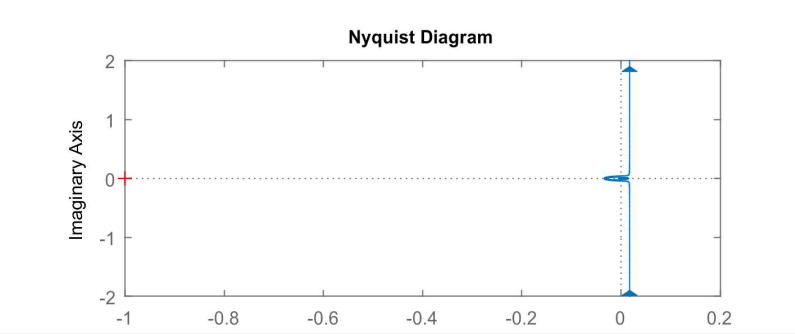
Actual (green)

LOOP STABILITY

- Block diagram of the PHIL loop
  - T_d is the total loop delay



PHIL loop block diagram



- Nyquist plot
  - 700μs loop delay
  - LPF

WIND POWER SMOOTHING

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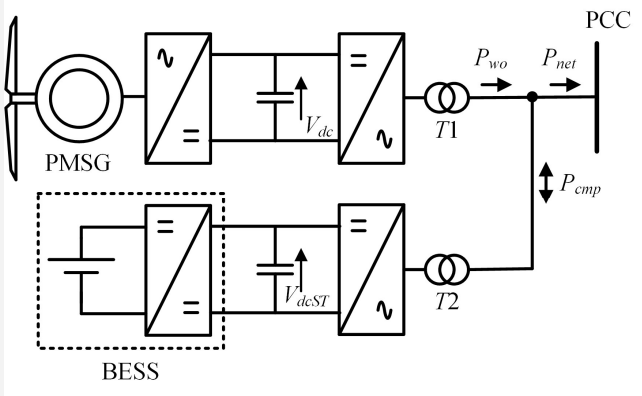
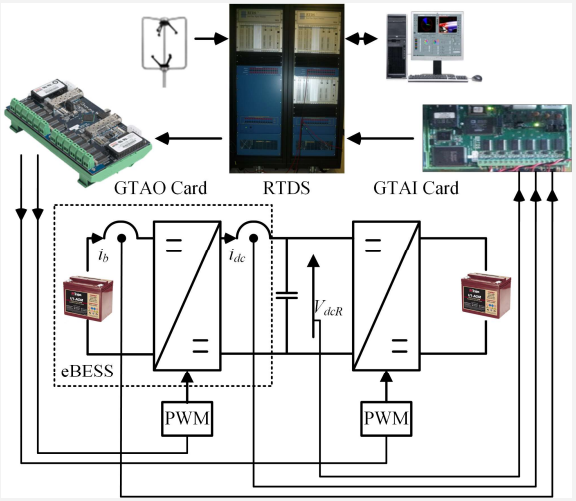


BESS integration at PCC



Schematic diagram of PHIL Loop.

A. Sattar et al., "Testing the performance of battery energy storage in a wind energy conversion system," IEEE Transactions on Industry Applications, vol. 56, no. 3, pp. 3196-3206, 2020.

WIND POWER SMOOTHING

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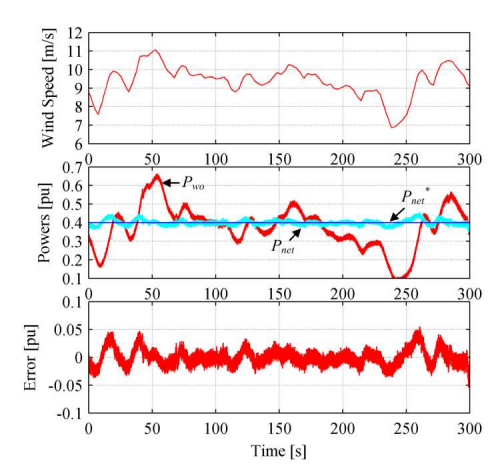
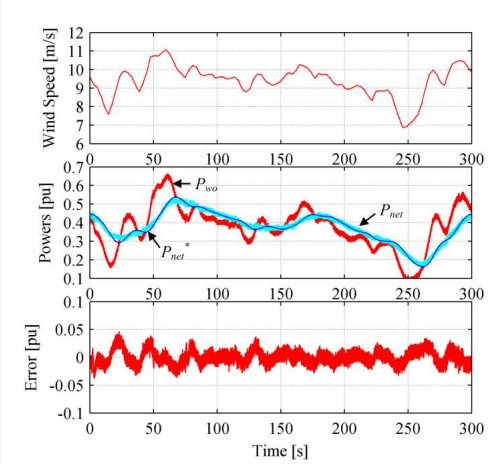
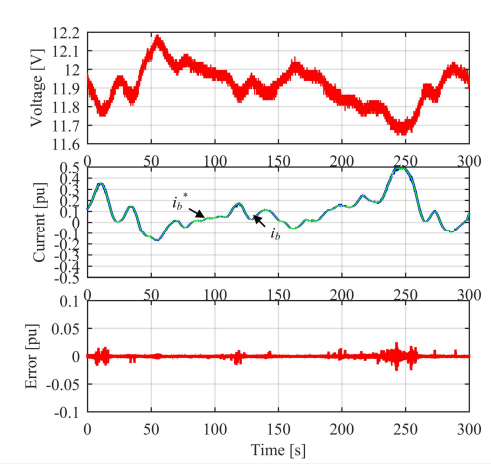
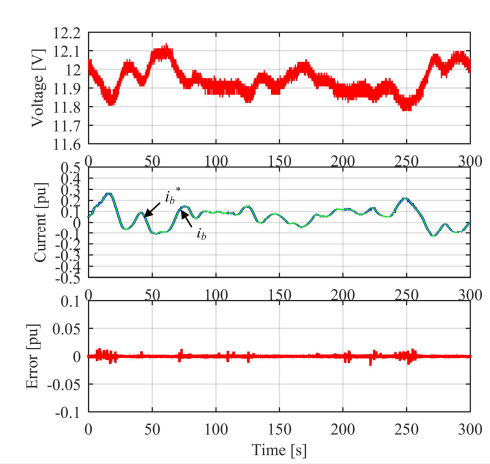




1st plot - wind speed; 2nd plot - P_{wo}, P_{net}* and P_{net}; 3rd plot – error between P_{net}* and P_{net}.





1st plot – battery voltage; 2nd plot – current i_b* and i_b; 3rd plot – error between i_b* and i_b.

CONCLUSIONS

- Proposed the use of AFE as PI for Reduced Hardware PHIL
- Case study with reduced-scale hardware
    - effect of timestep interaction on the loop delay
    - loop stability
- Wind power smoothing
- Effective way for testing BESS

Thank you for your attention!

Contact: cedric.caruana@um.edu.mt

The authors would also like to acknowledge the project: “Setting up of transdisciplinary research and knowledge exchange (TRAKE) complex at the University of Malta (ERDF.01.124)” which is being co-financed through the European Union through the European Regional Development Fund 2014 – 2020. www.eufunds.gov.mt.