RTDS Technologies

AMETEK

Implementation of GE Vernova MMC HVDC Controls on GTSOC platform

With the modernization of the grid, there is growing demand for HVDC projects throughout the world. Real time simulation has been used for the development, testing, validation as well as long term maintenance of HVDC controls for many years via hardware in the loop (HIL) simulation. The interoperability of devices from different vendors can also be validated using real time simulation and HVDC replica controls via HIL testing. At early stages of projects, such replicas are not available and prevent real time simulation testing to take place.

RTDS Technologies have developed the GTSOC platform to model vendor controls for a software in the loop application. The GTSOC allows for convenient and deterministic integration of black box controls into a real time simulation environment and ensures vendor IP is secure. It allows the end user to use the GTSOC hardware to emulate real vendor equipment for different projects and from different vendors, provided the vendor control model is available. GTSOC is not a replacement for replica controls as the full scope of tests cannot be performed with the GTSOC version of the controls. However, they can act as a good representation when replica controls are not available and are suitable for multiple types of investigations.

Figure 1. GTSOC V1 unit

The GTSOC includes four application ARM cores which are used to run the vendor controller as well as FPGA fabric used to provide a communication interface between the GTSOC and the NovaCor unit. RTDS Technologies has also developed a GTSOC Black Box builder tool to assist the vendor in developing the wrapper application and firmware that runs on the GTSOC. The GTSOC only models the vendor controls while the power system circuit is modelled on the NovaCor chassis. GTSOC and NovaCor chassis are connected via fibre.

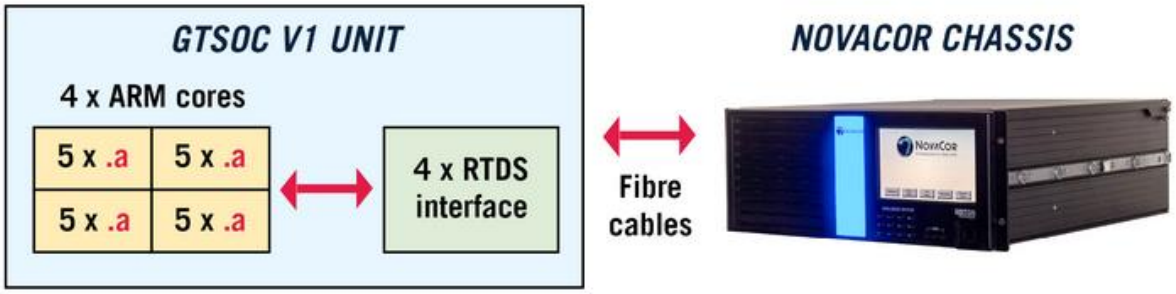

Figure 2. NovaCor chassis and GTSOC

RTDS Technologies has worked with **GE Vernova (GE)** to model their MMC HVDC control and protection solution, eLumina™, on the GTSOC units. Due to the complexity of HVDC control and protection, multiple ARM cores on the GTSOC unit are used, distributing the different tasks of GE's source code. Through testing it was determined the best way to distribute the task across the GTSOC ARM cores. The GTSOC platform also supports inter-core communication between ARM cores which means if tasks on different ARM cores need to send/receive data, the data can be communicated directly between ARM cores without the need to route through NovaCor which would add additional delays.

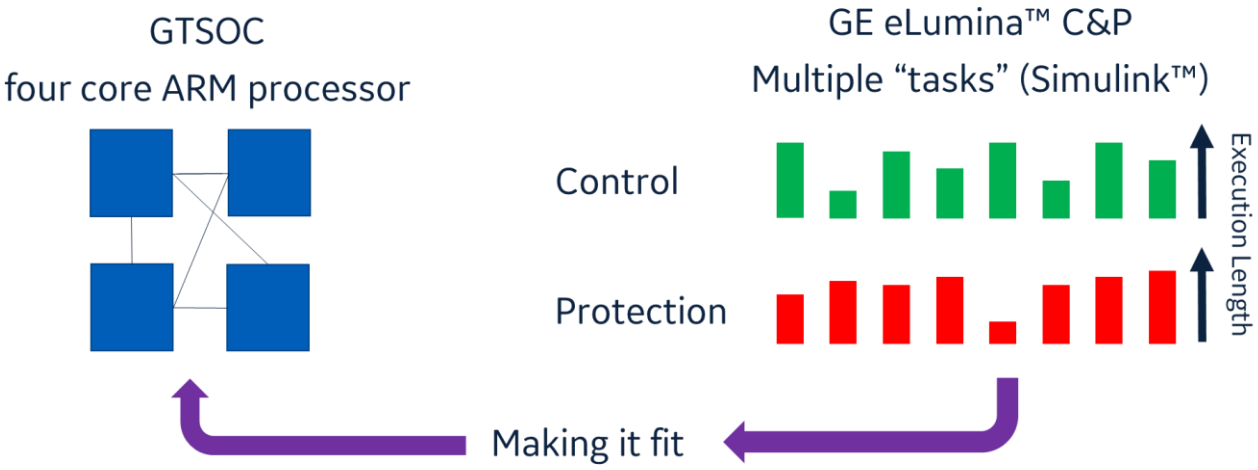

Figure 3. Distributed GE controls across the GTSOC's four available ARM cores

For the design, two GTSOC units each utilizing all four ARM cores are required to model one monopole station's control and protection. One GTSOC is dedicated for the control unit and a second GTSOC is dedicated for the protection unit.

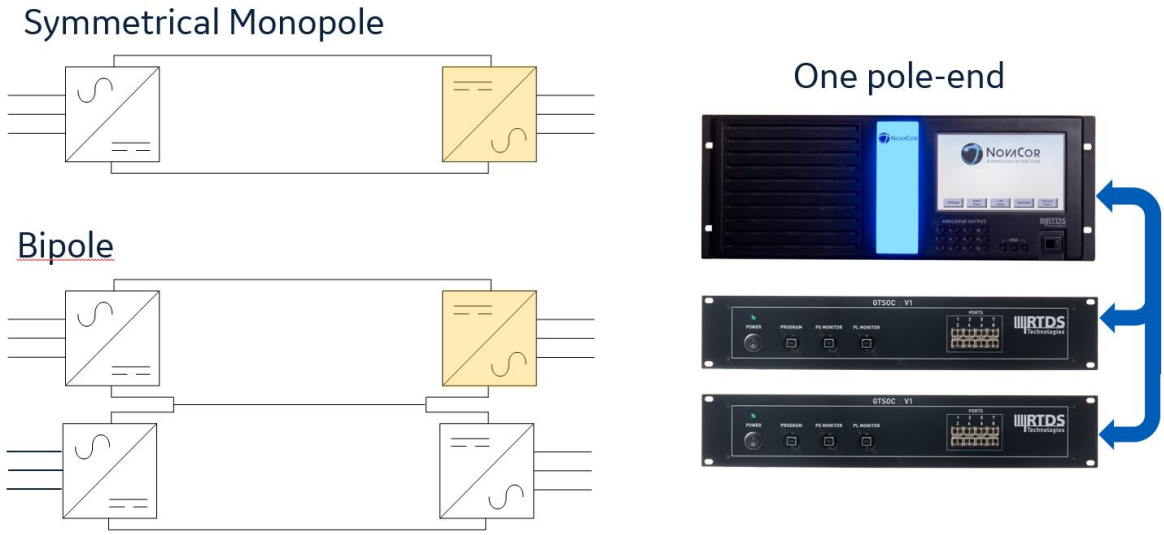

Figure 4. Two GTSOC units required to model one Monopole terminal.

The code running on the GTSOC units include a full implementation of the control and protection while the valve base electronics are simplified, as the lower level firing are not modelled on the GTSOC units and not included in the simulation model. In RSCAD, the simplified MMC5 converter valve model is used where the input is the SM insertion number i.e. the number of SMs to be inserted. This level of detail is suitable for the system level studies which are being targeted for the software in the loop applications.

To validate the controls and protection code running on the GTSOC units, a single monopole onshore converter is used as the test circuit. On the DC side, a DC cable is included, and the offshore terminal is simplified as a DC current injection. The case runs on 1 NovaCor chassis (1 core) and 2 GTSOC units. NovaCor simulation time step is 25 µsec.

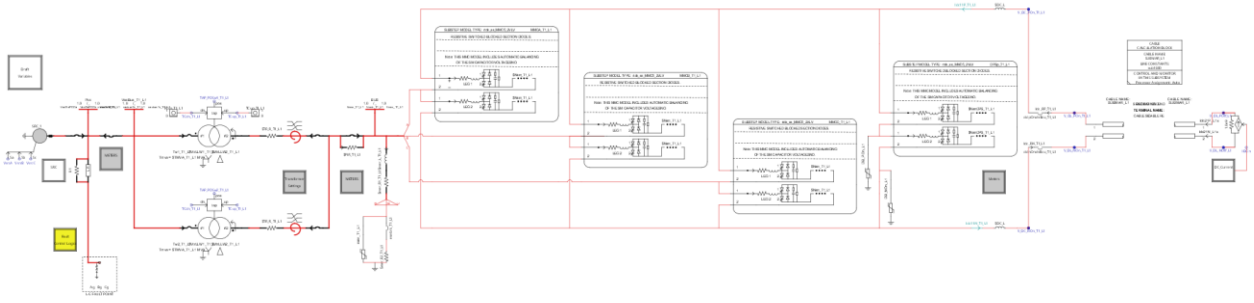

Figure 5. Model of single Monopole HVDC terminal with DC current injection

The DOTA component in RSCAD FX is used to create the interface to each GTSOC core. As a result, 8 DOTA components are configured.

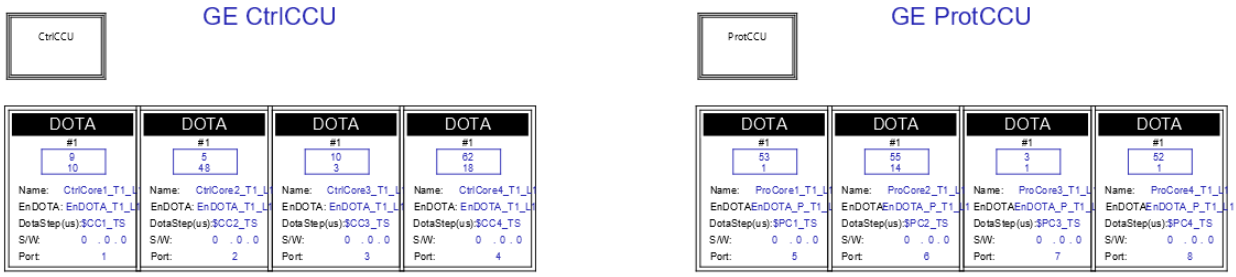

Figure 6. GTSOC interface for each of 8 cores across 2 GTSOC modelling Control and Protection.

The RTDS simulation results are compared with results obtained in the offline tool PSCAD running the same GE Vernova control and protection code. Results show very good comparison between both platforms which helps to validate both the power system model built on NovaCor and MMC HVDC controls running on the GTSOC. Slight differences in some of results are due to minor differences in how the controls are implemented in RSCAD and PSCAD. However, as you can see from the results, the comparison results are very good.

Simulation Results

The performance analysis is done on the following list of validation signals:

Onshore DC PCC:

- Positive terminal DC voltage
- Negative terminal DC voltage
- Positive terminal DC current
- Negative terminal DC current

Onshore AC Point of Common Coupling (PCC):

- RMS voltage
- Phase A AC voltages
- Phase A AC currents
- Active power
- Reactive power

Onshore AC Point of Common Coupling (PCC):

- Three phase AC voltage (each phase on own plot)
- Three phase AC current (each phase on own plot)

The following dynamic performance tests are provided:

1- Energization

2- Power ramp

3- DC voltage step at onshore station (-0.1 p.u)

4- AC voltage step at onshore station (-0.01 p.u)

5- Single phase fault at onshore PCC *

6- Three phase fault at onshore PCC*

*DC side results are not included for AC fault tests at the request of GE Vernova.

The PSCAD plots are in blue and the RTDS results are overlayed in green.

1. ENERGIZATION

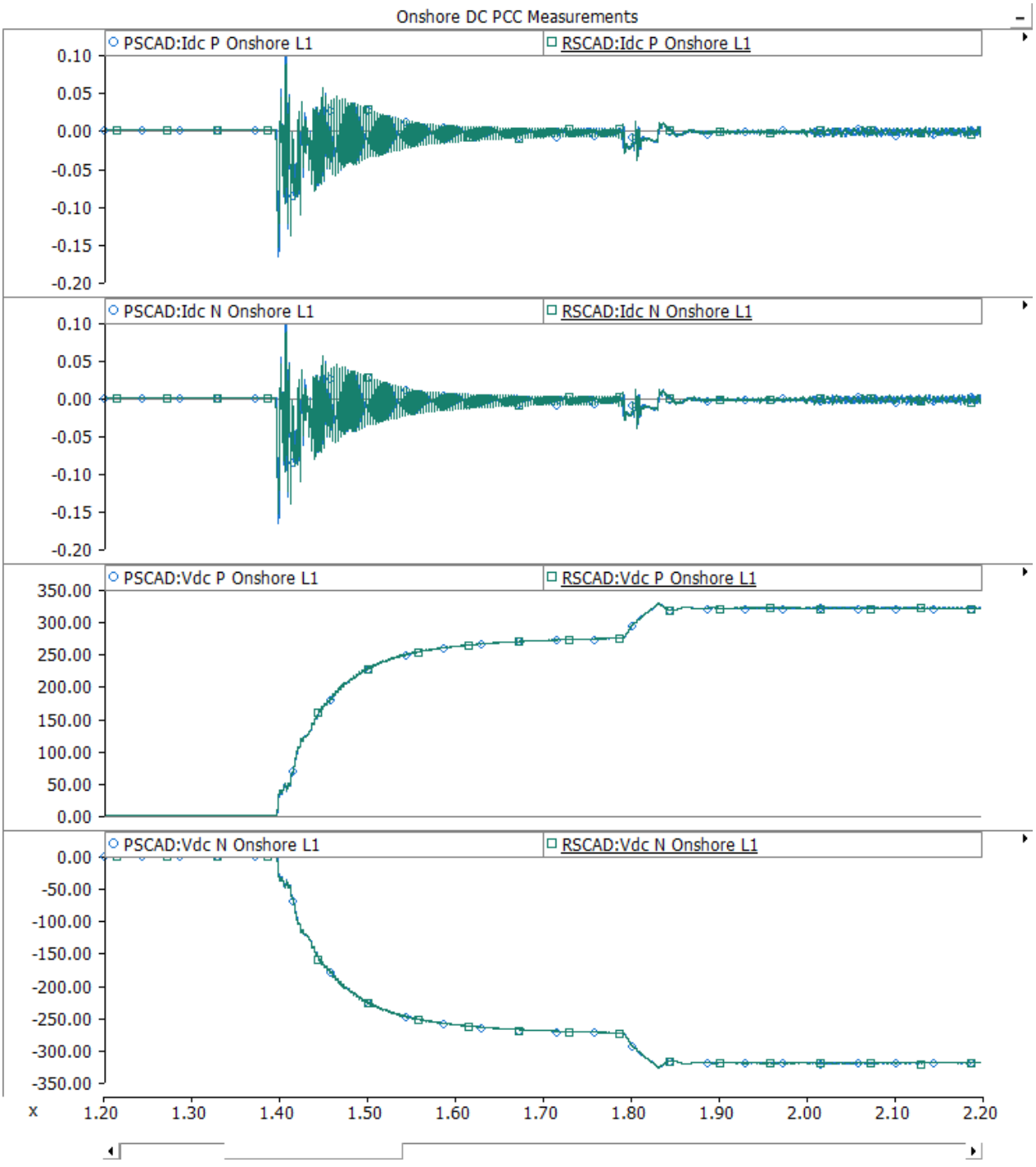

Figure 7. Energization - Onshore DC PCC Measurements

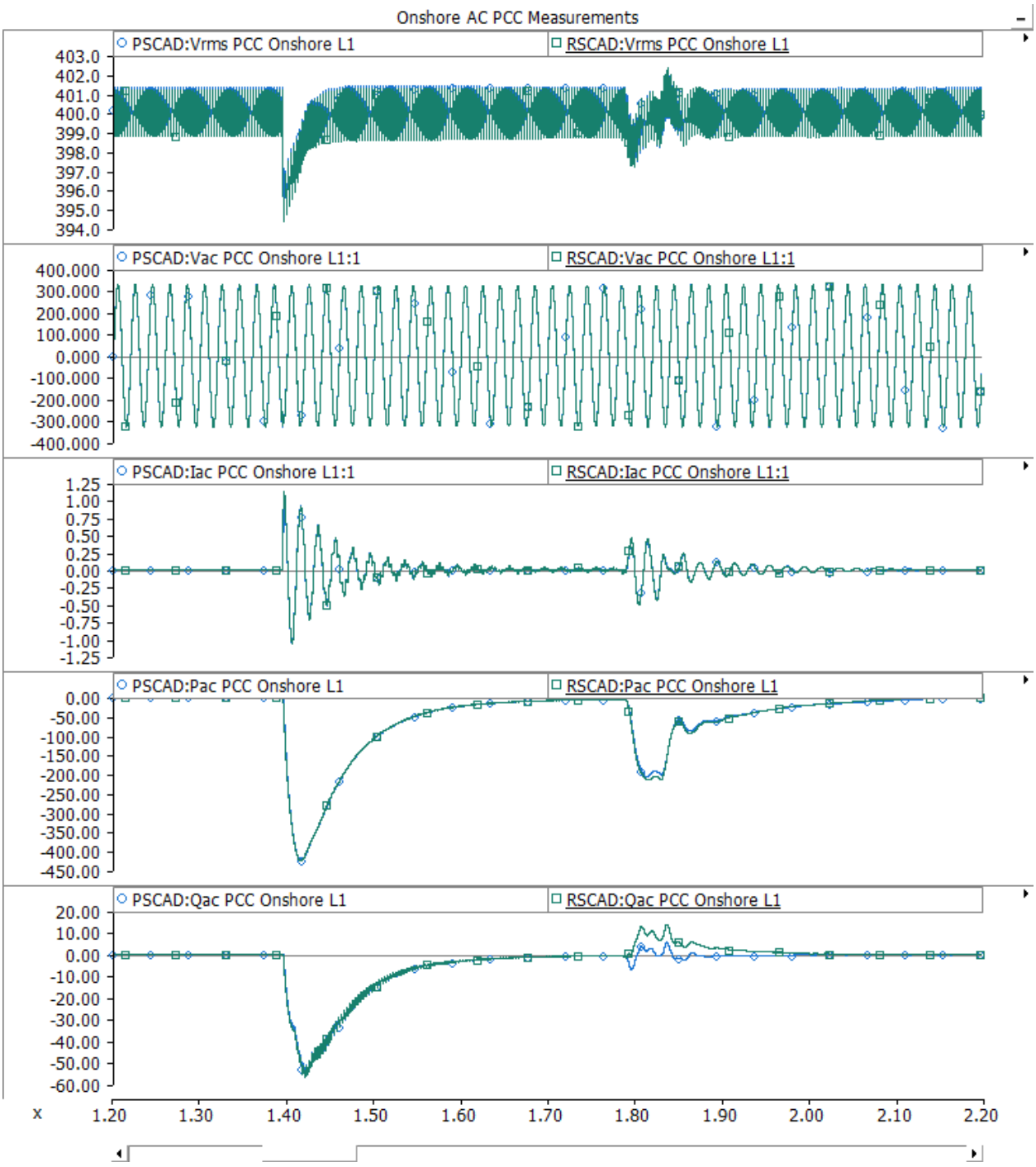

Figure 8 Energization - Onshore AC PCC Measurements

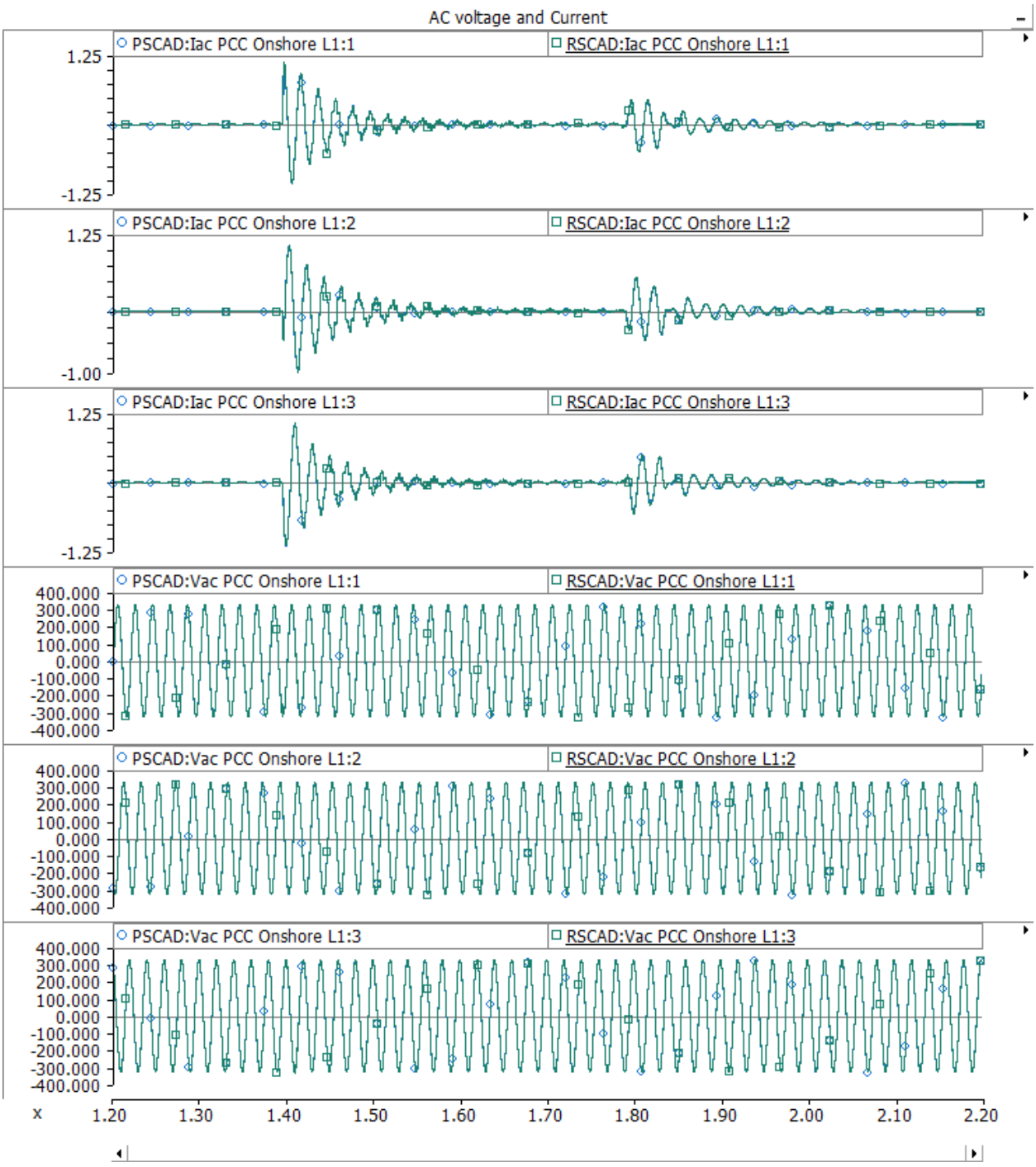

Figure 9 Energization – AC voltage and Current

2. POWER RAMP (0 to 320 MW)

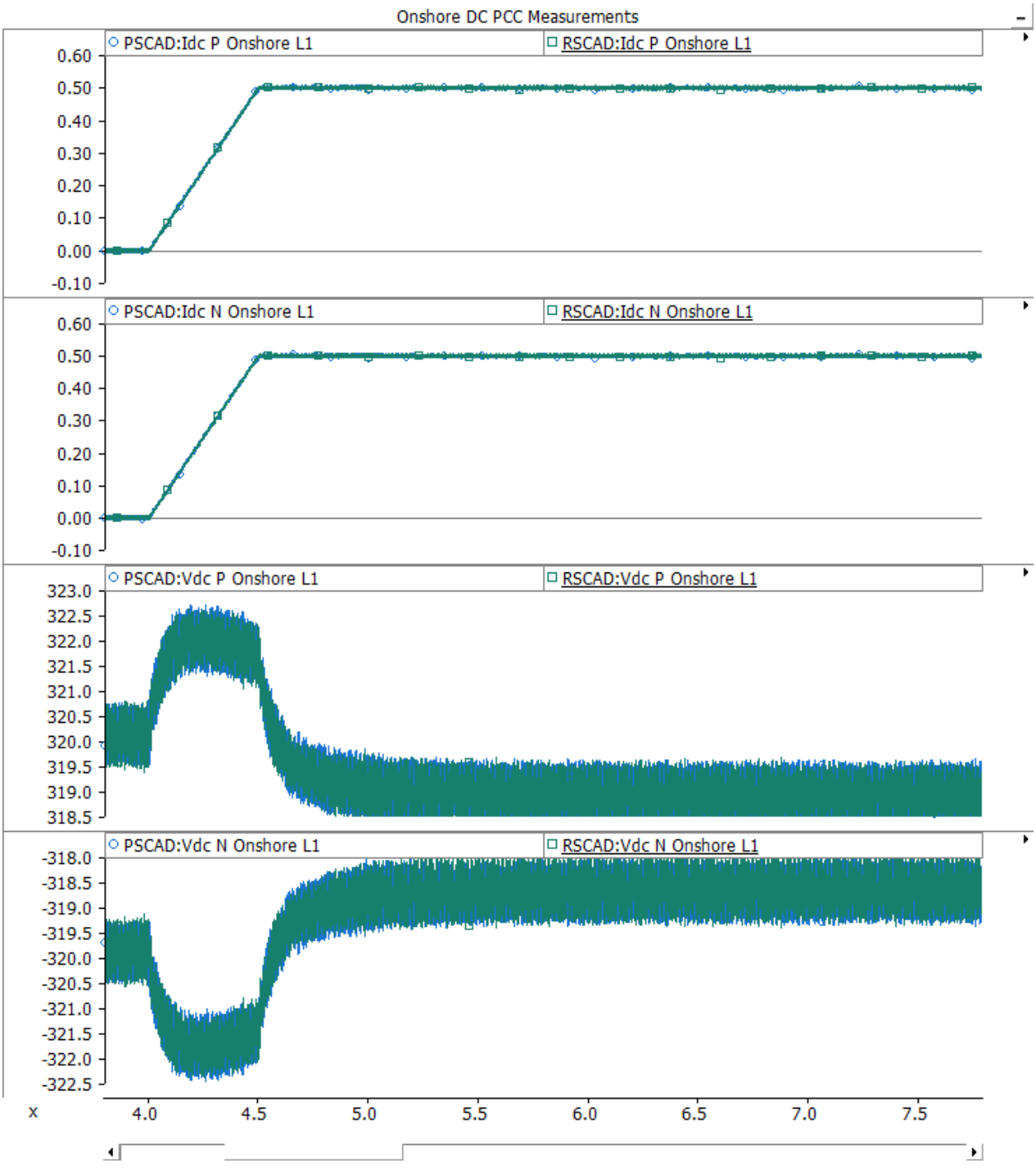

Figure 10. Power Ramp- Onshore DC PCC Measurements

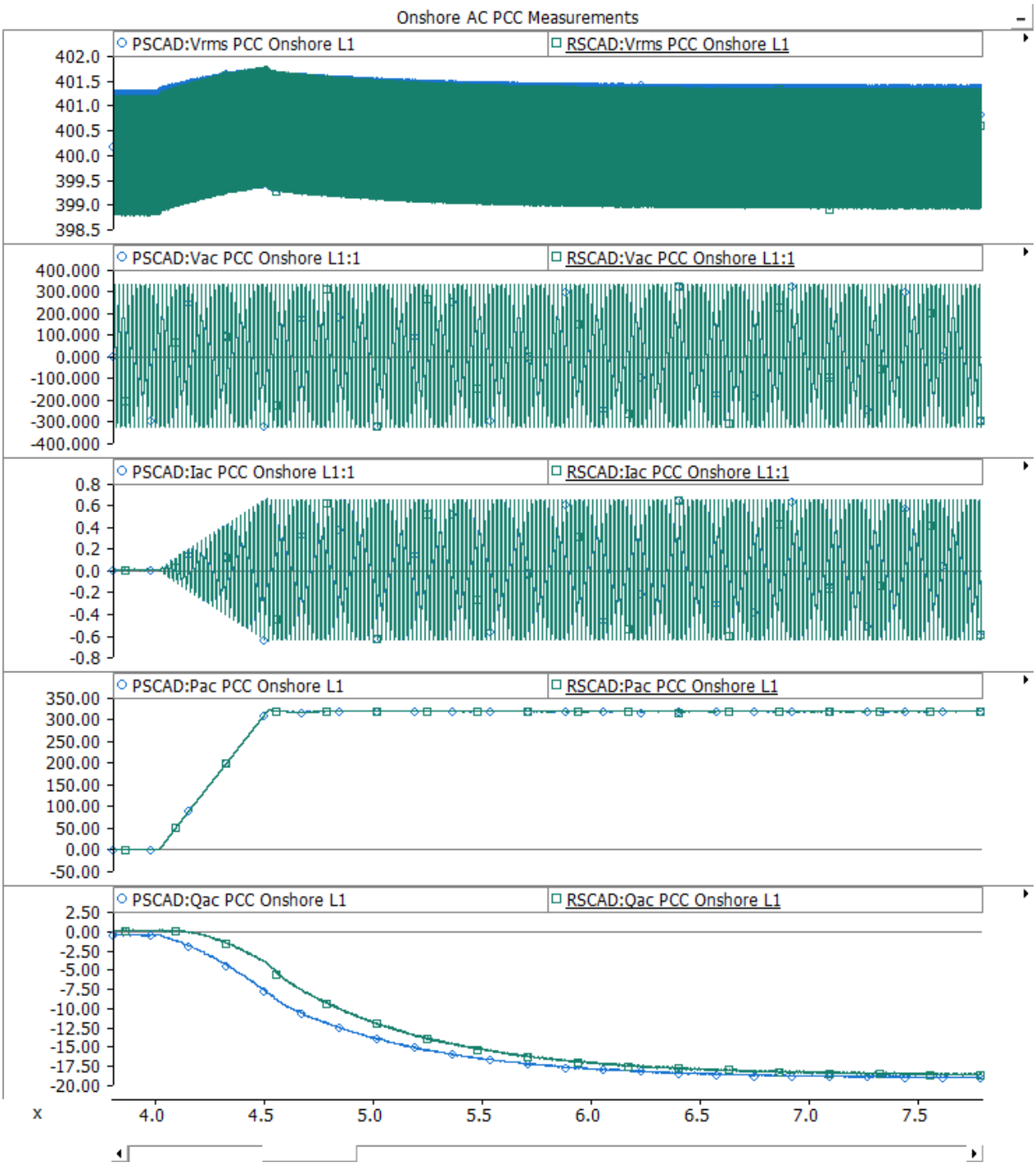

Figure 11. Power Ramp- Onshore AC PCC Measurements

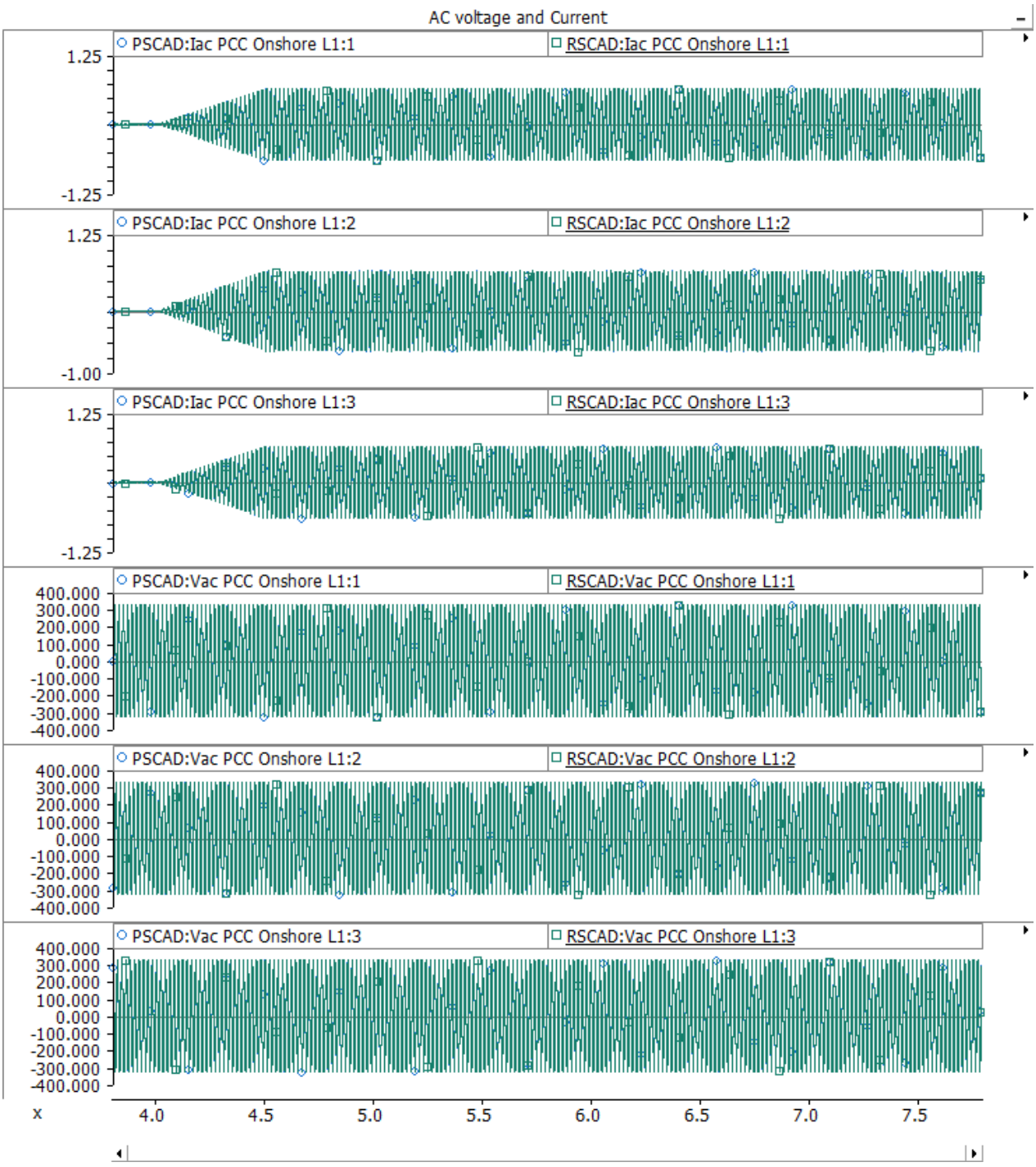

Figure 12 Power Ramp- AC voltage and Current

3. DC VOLTAGE STEP (-0.1 P.U)

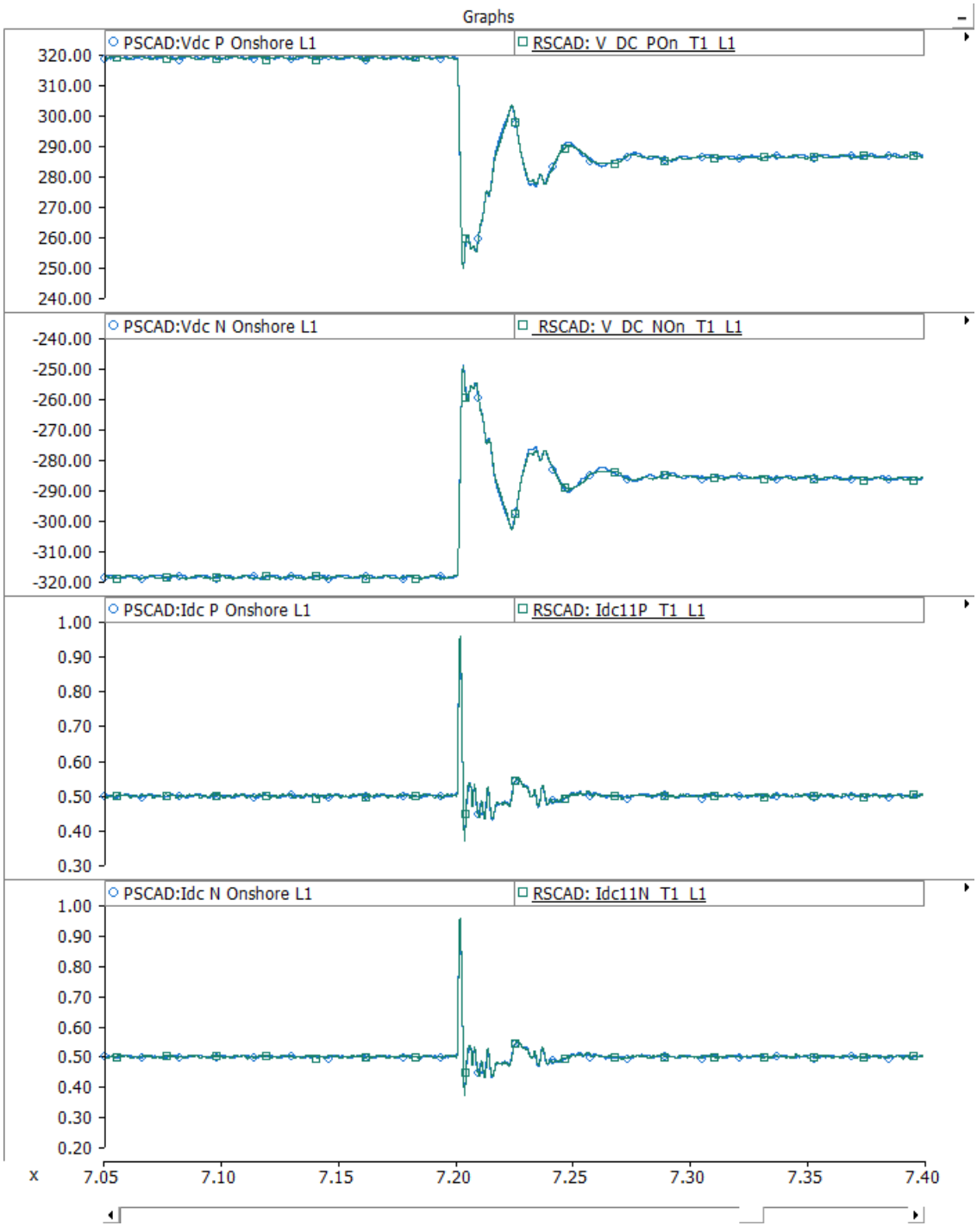

Figure 13. DC Voltage Step- Onshore DC PCC Measurements

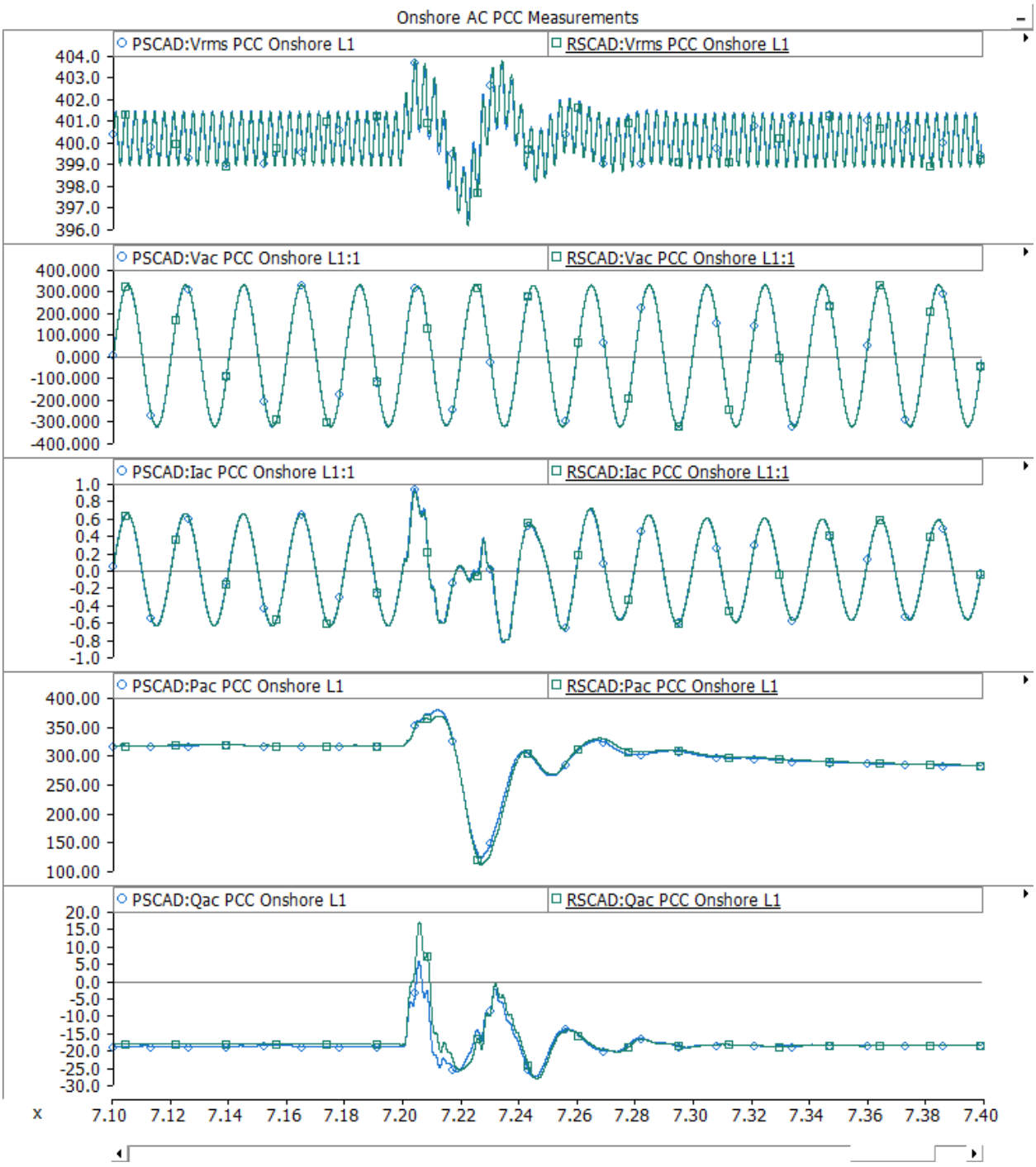

Figure 14 DC Voltage Step- Onshore AC PCC Measurements

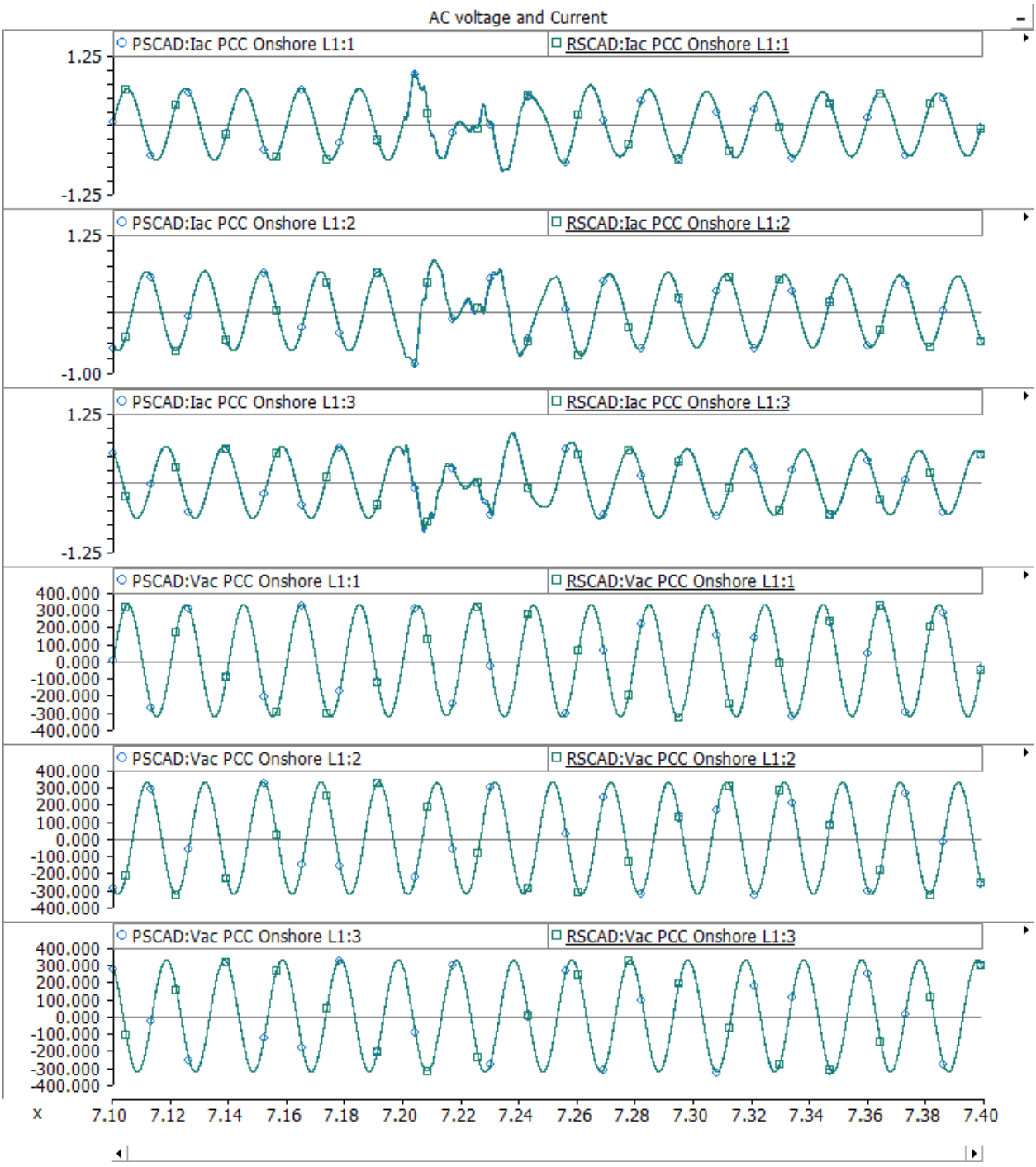

Figure 15 DC Voltage Step - AC voltage and Current

4. AC VOLTAGE STEP (-0.01 P.U)

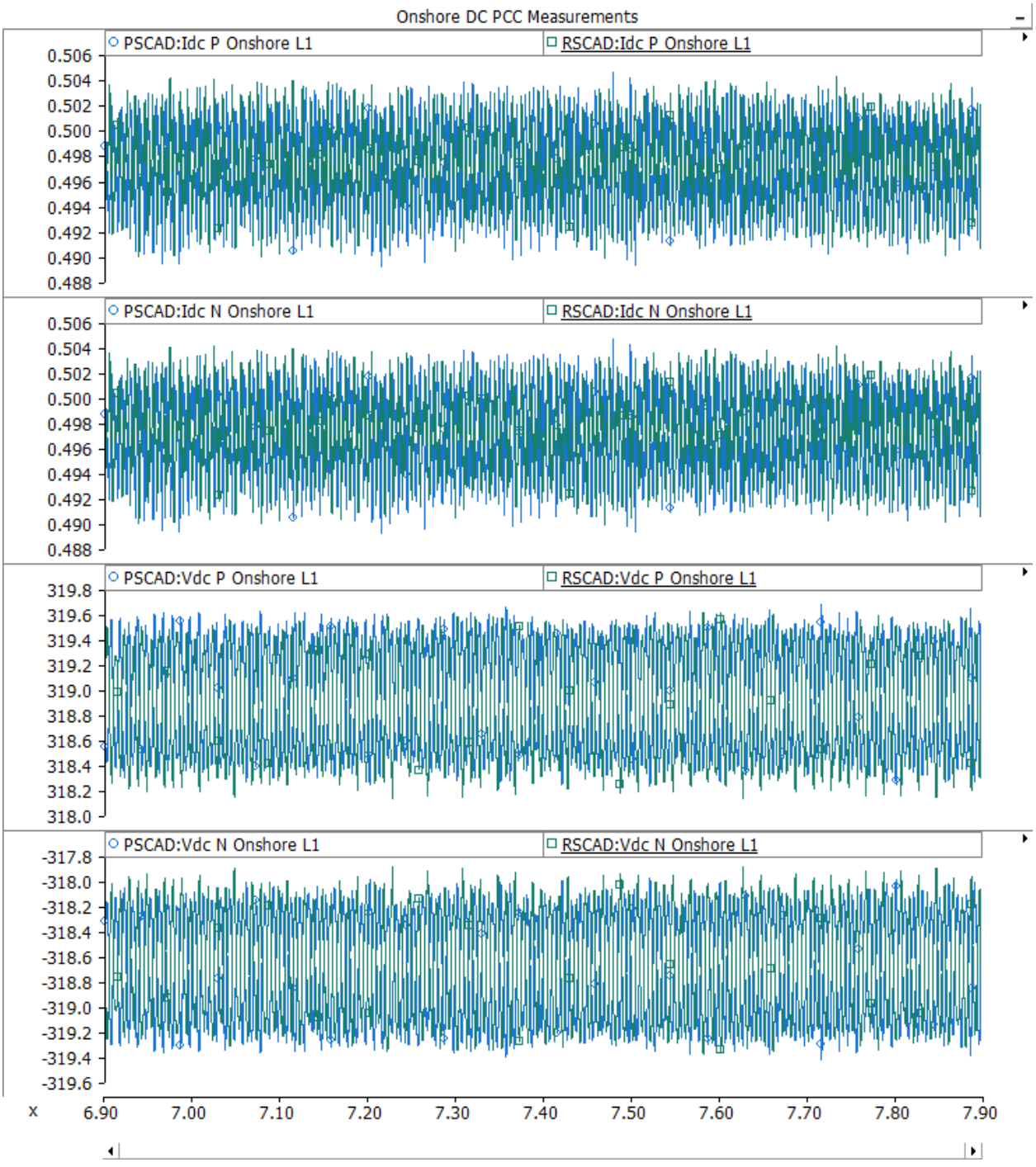

Figure 16 AC Voltage Step - Onshore DC PCC Measurements

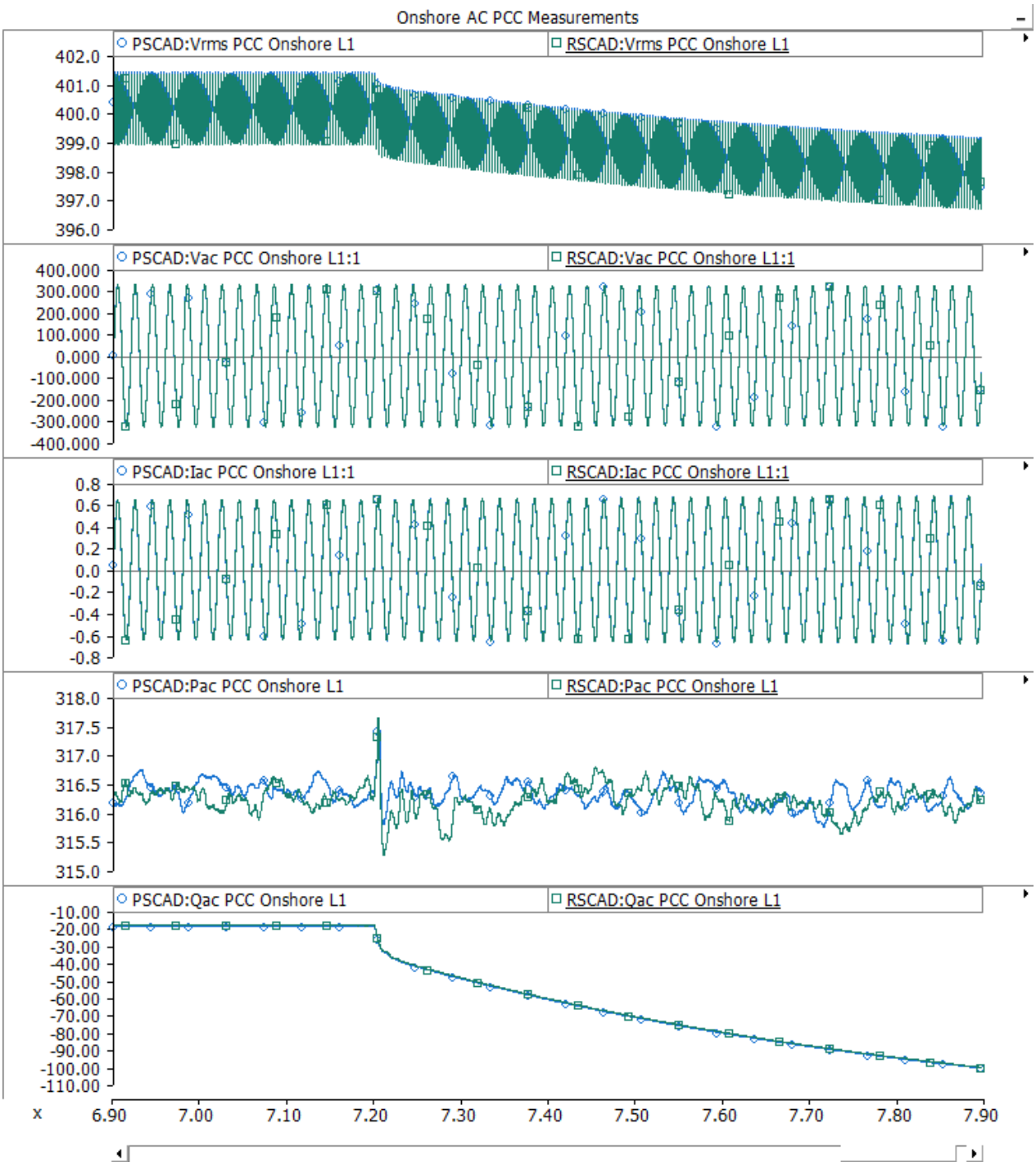

Figure 17 AC Voltage Step - Onshore AC PCC Measurements

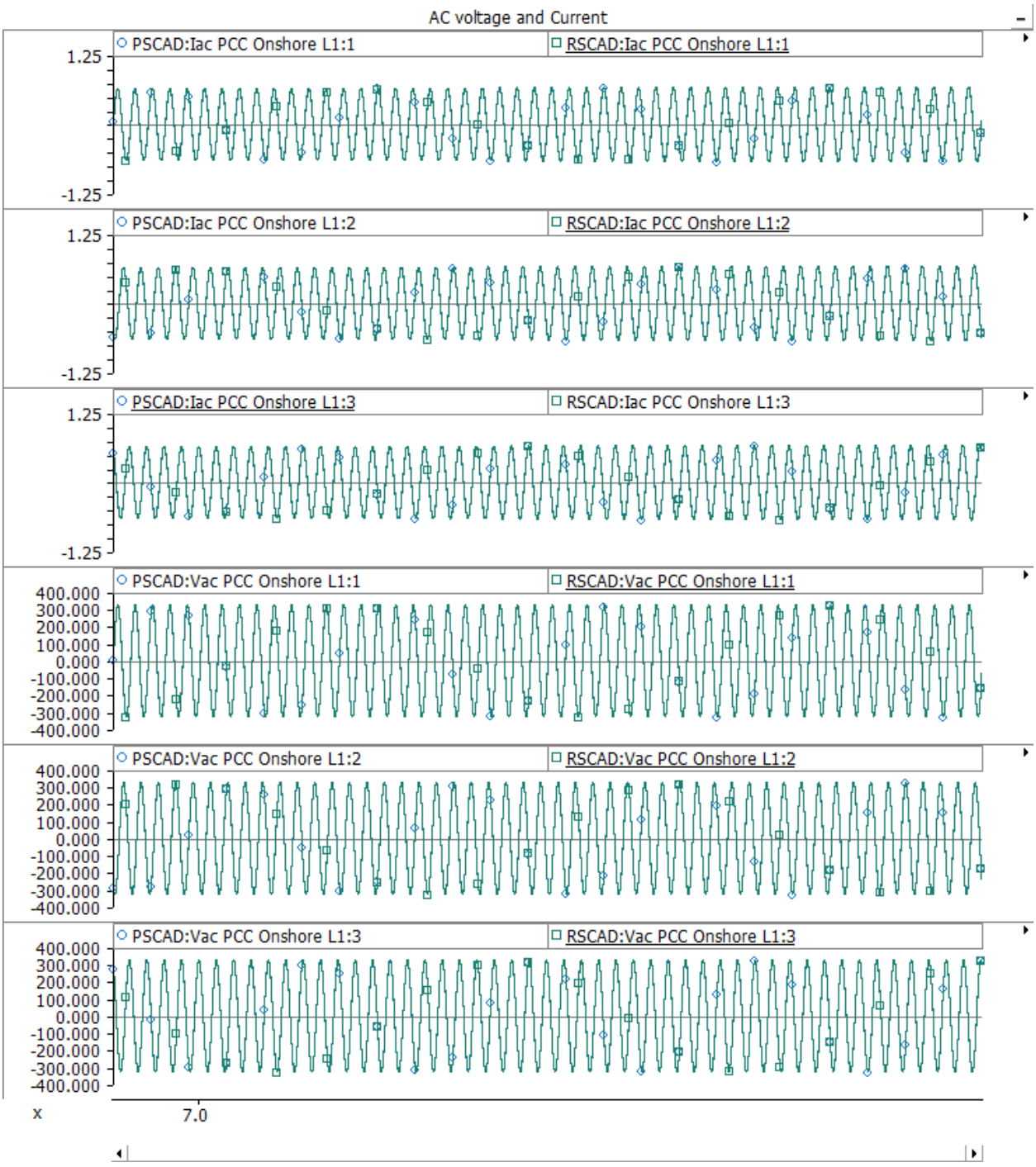

Figure 18 AC Voltage Step - AC voltage and Current

5. SINGLE PHASE FAULT (PHASE A)

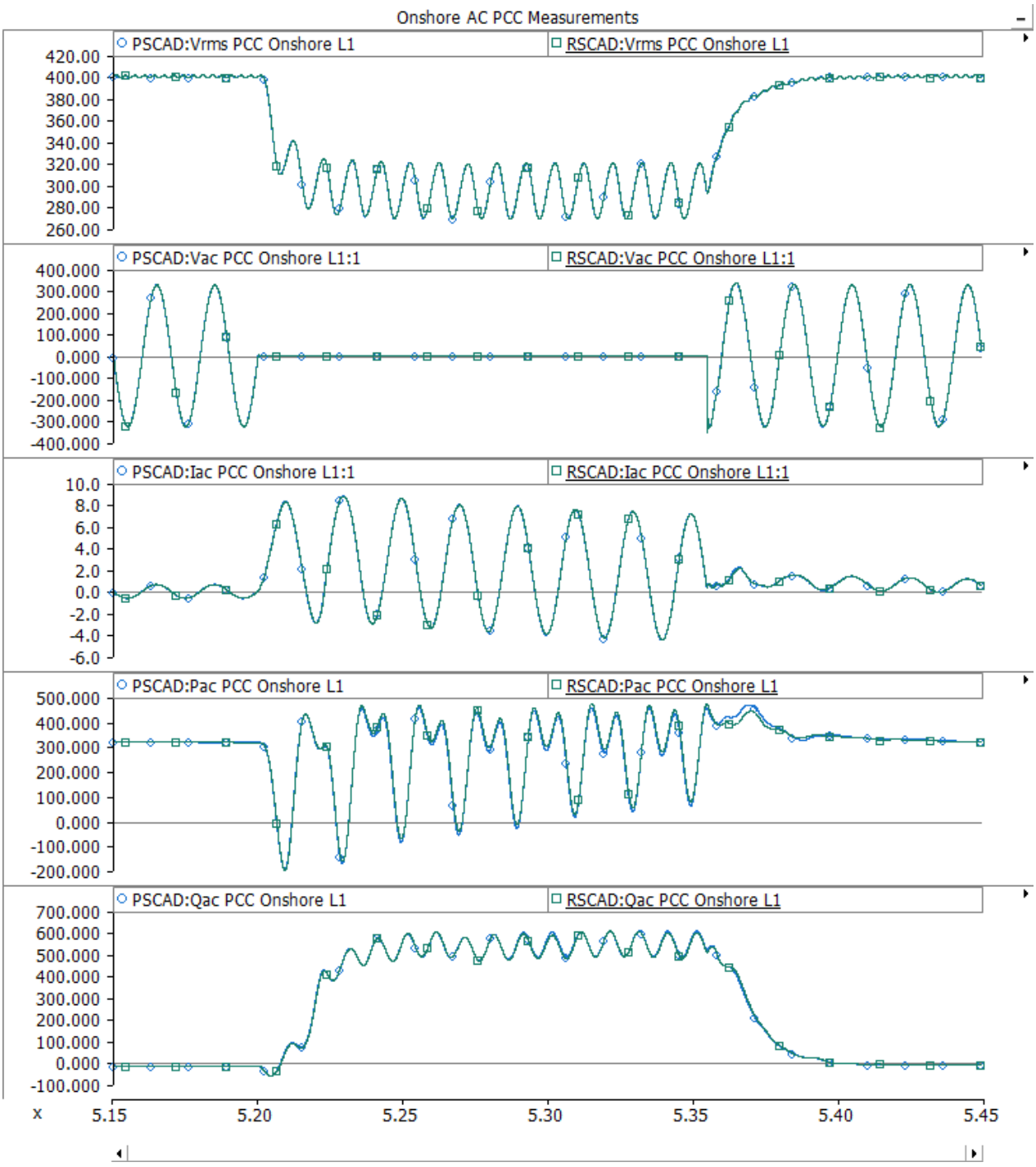

Figure 19 Single Phase Fault - Onshore AC PCC Measurements

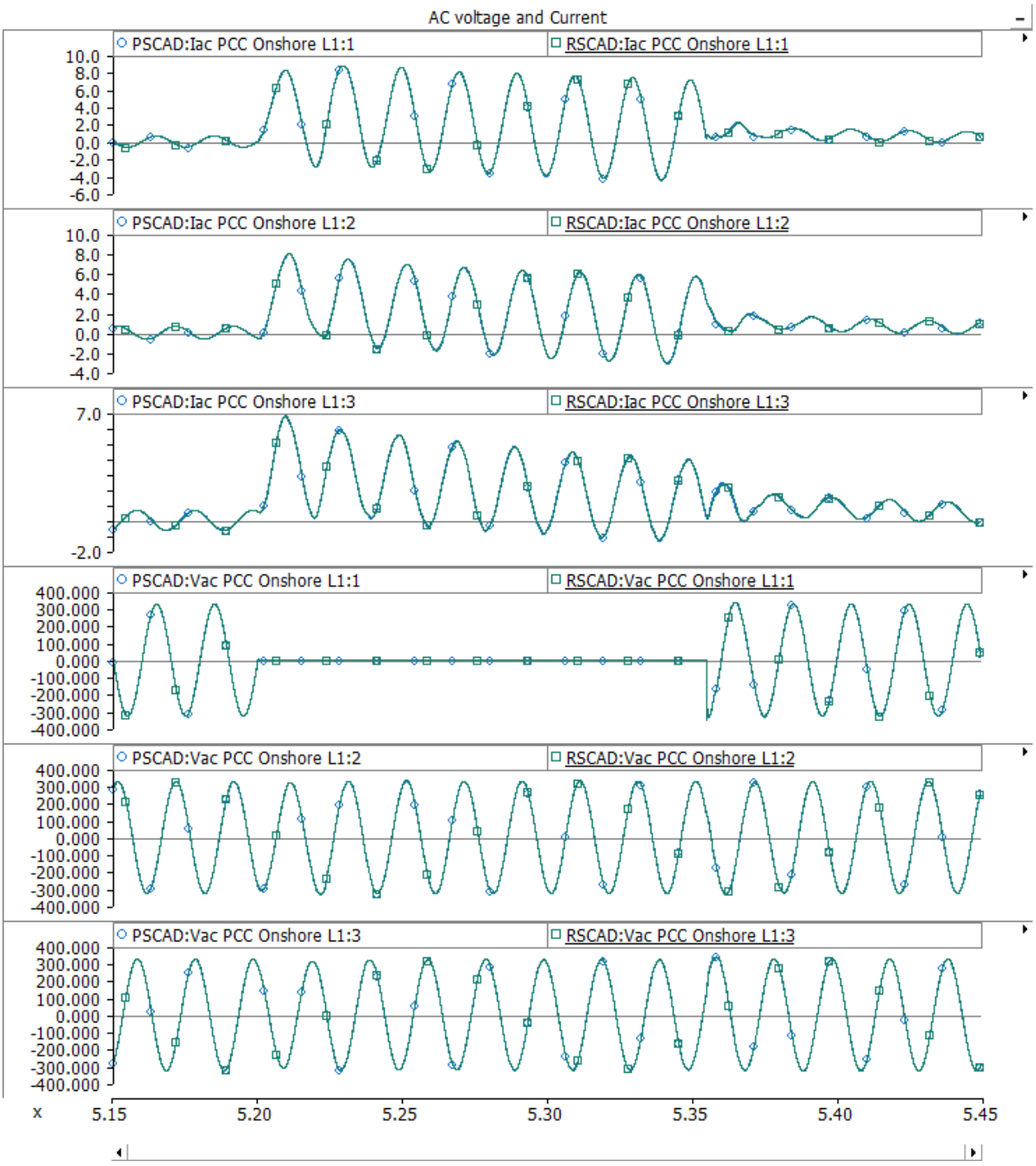

Figure 20 Single Phase Fault - AC voltage and Current

6. THREE PHASE FAULT (PHASES A-B-C TO GROUND)

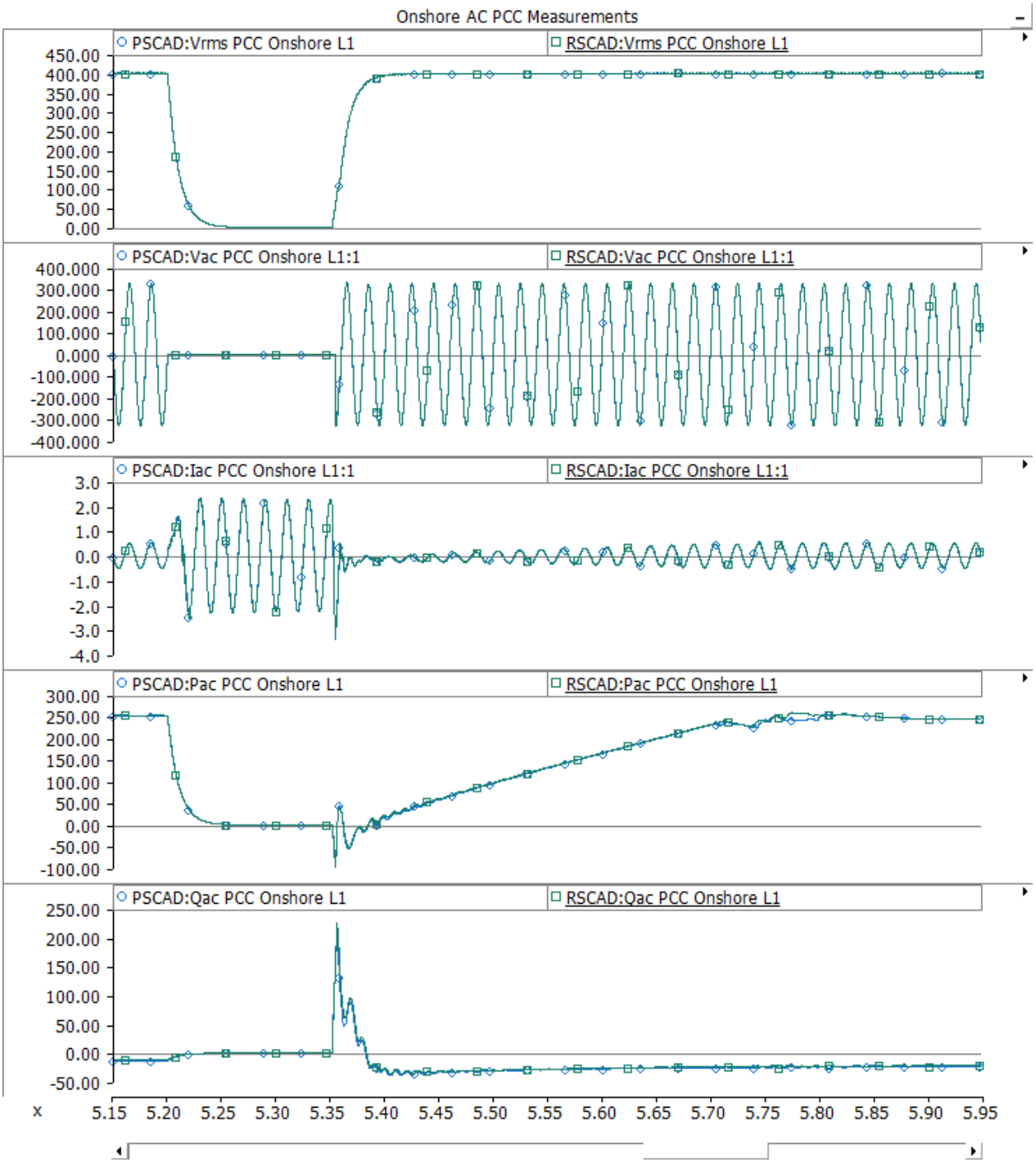

Figure 21 Three Phase Fault - Onshore AC PCC Measurements

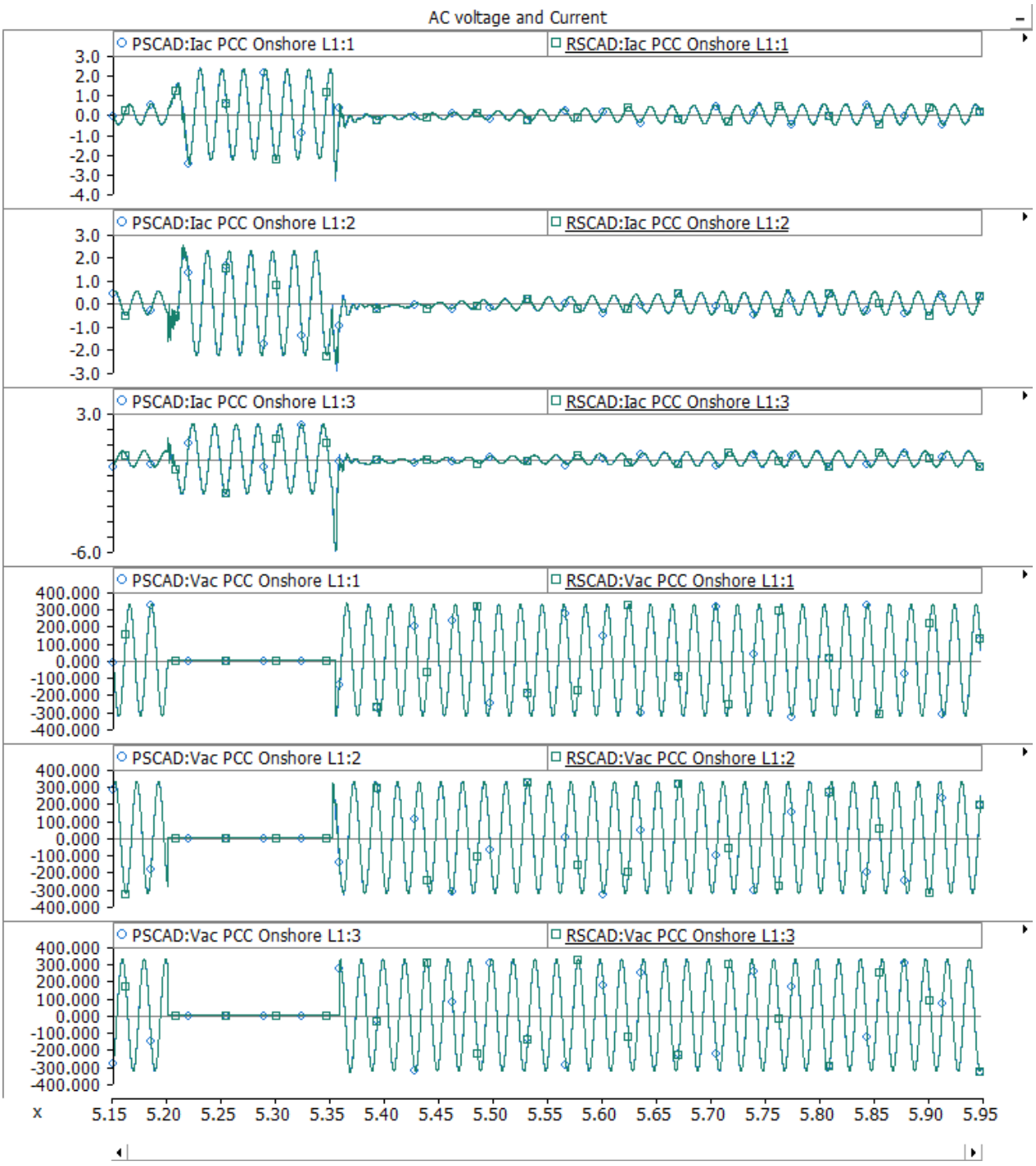

Figure 22 Three Phase Fault - AC voltage and Current