FREEDM SYSTEMS CENTER

New York Power Authority

# *Real Time C-HIL Implementation of 100 MVA Convertible Static Compensator (CSC) for New York Power Authority*

Semih Isik, Harshit Nath, Dr. Subhashish Bhattacharya

# *Outline*

I. The Convertible Static Compensator (CSC) at New York Power Authority (NYPA)
II. RSCAD setup of the CSC
III. PSCAD setup of the CSC
IV. Transient Network Analyzer (TNA)
V. C-HIL Implementation

# *What is CSC?*

- The Convertible Static Compensator (CSC) at NYPA is power electronic-based equipment that provides dynamic voltage regulation of the Marcy Substation 345 kV bus, and controls the electric power flow in the New Scotland and/or the Coopers Corner 345 kV transmission lines as seen in Fig. 1

- The CSC employs two identical voltage-sourced Gate Turn off (GTO) thyristor-based inverters, each with a nominal steady state rating of ±100 MVA, and each capable of full 4-quadrant operation.

- Four three level NPC converter, which can be seen in Fig. 3, are used for CSC. Therefore, their square wave outputs are combined electromagnetically to generate a 48 pulse output voltage waveform as described in Fig. 4.

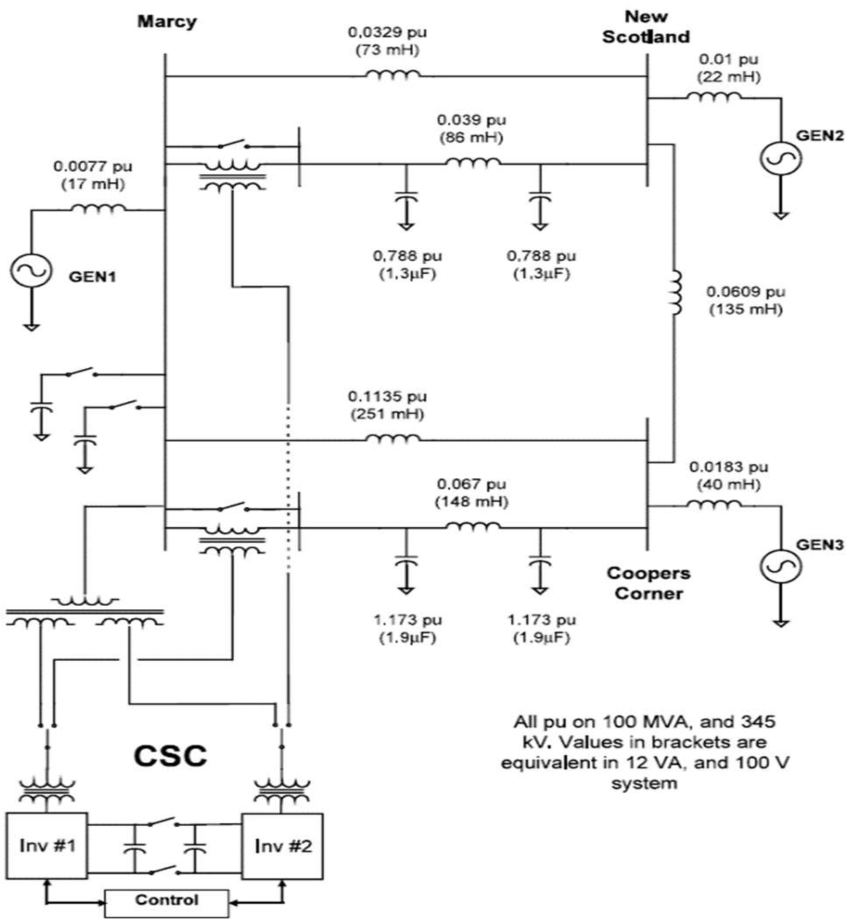



Figure 1: NYPA CSC Oneline Diagram

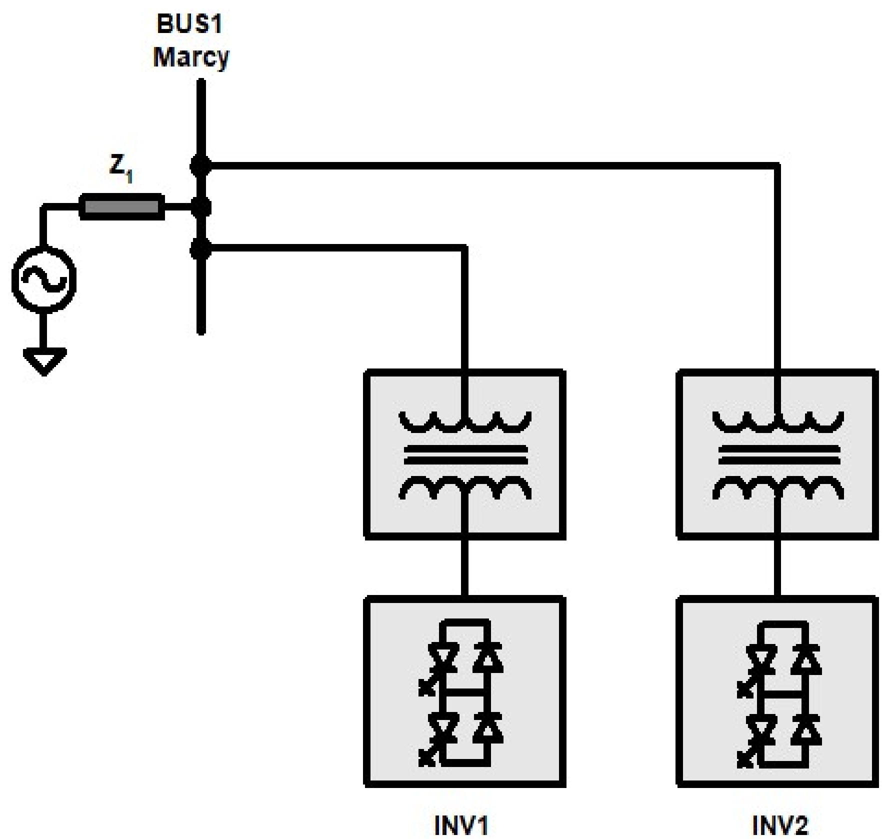



Figure 2: STATCOM Model of the CSC

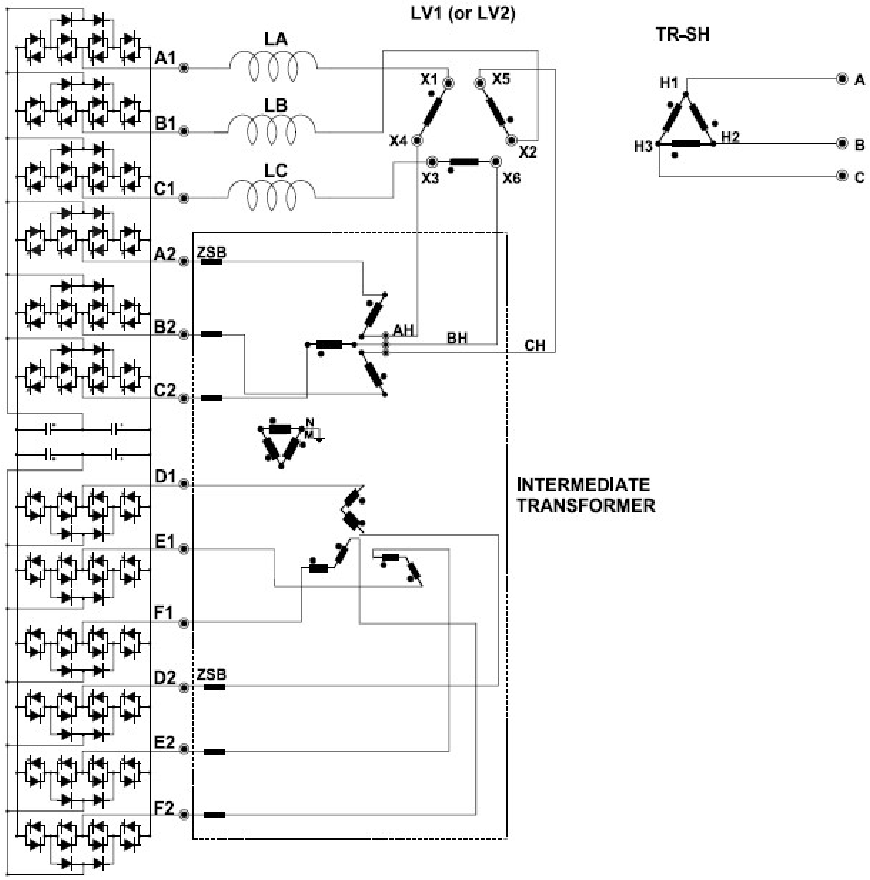



Figure 3: NYPA CSC Single Inverter Power Circuit

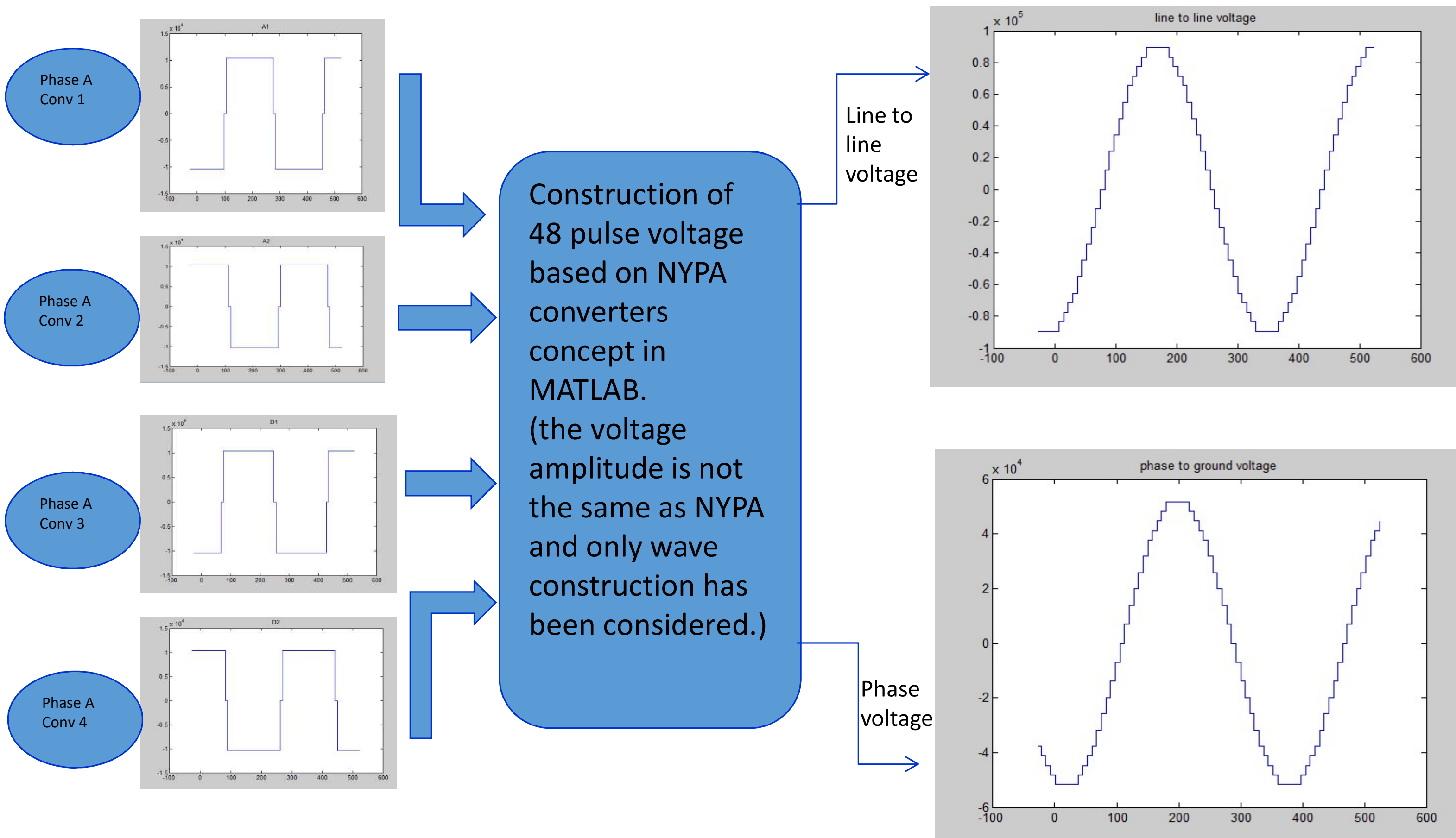



Figure 4: 48 Pulse Generation in MATLAB

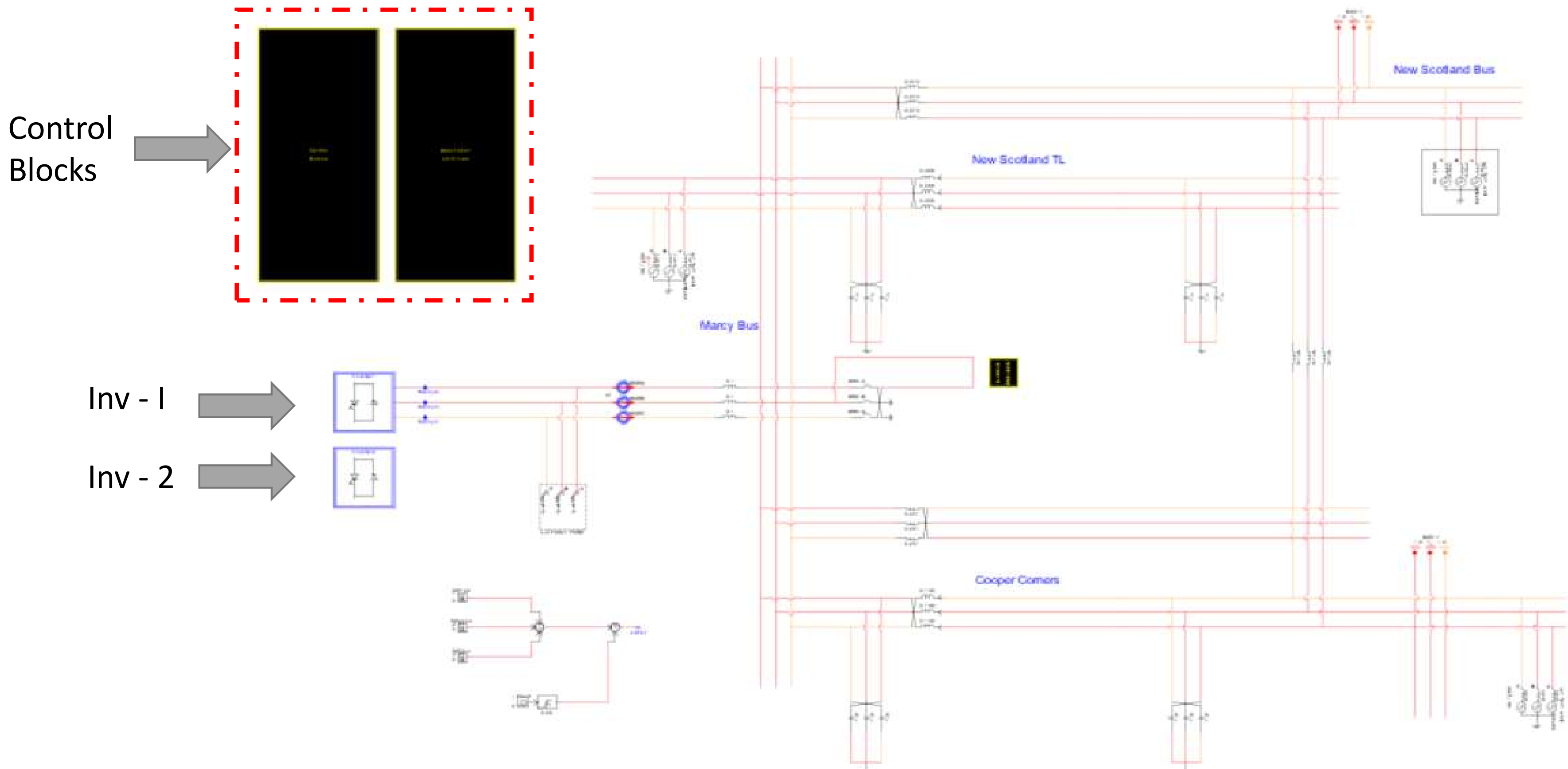



Figure 5: NYPA 3 Bus System with STATCOM in RSCAD

NC STATE UNIVERSITY

***Inv – I inside the small step bridge box***

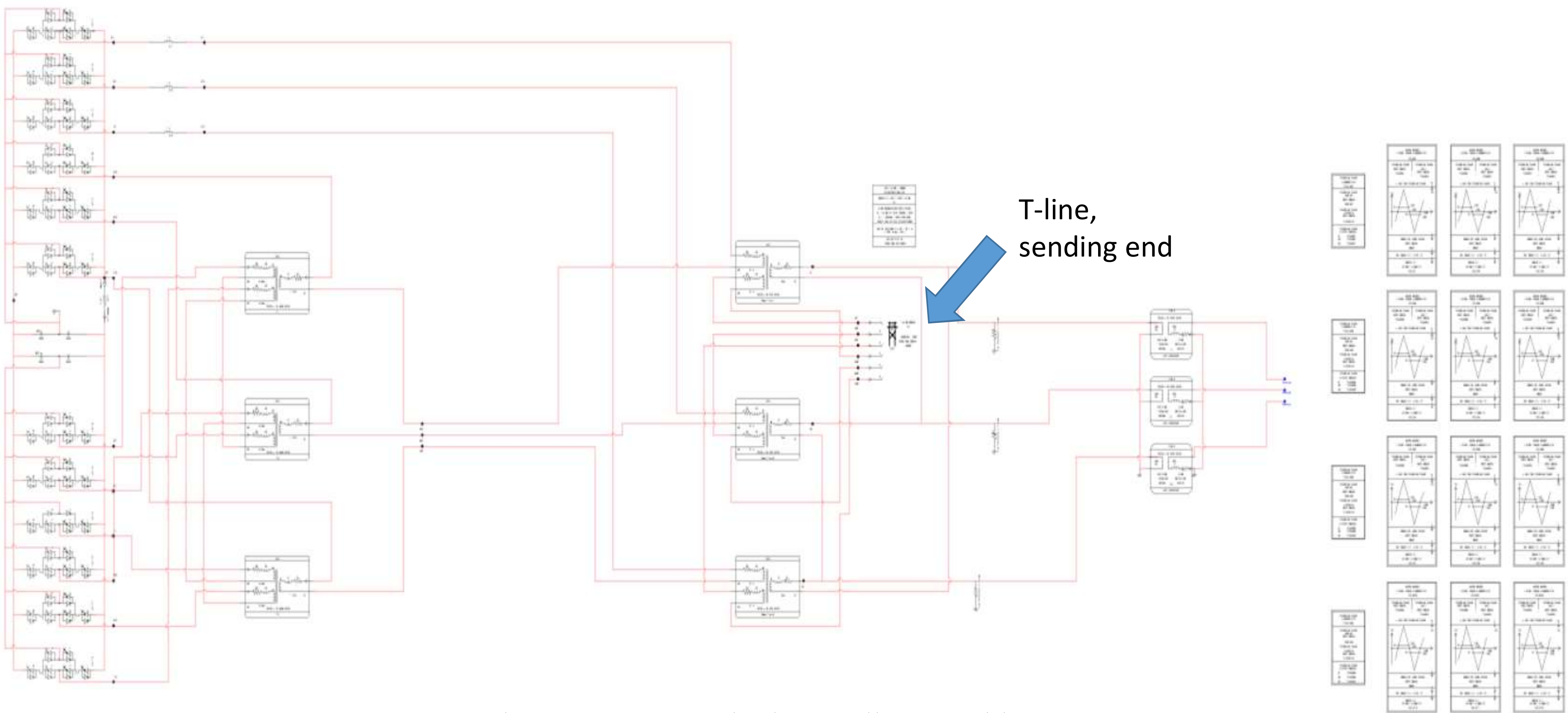



Figure 6: Inverter I in the Small Step Bridge Box

*Inv – II inside the small step bridge box*

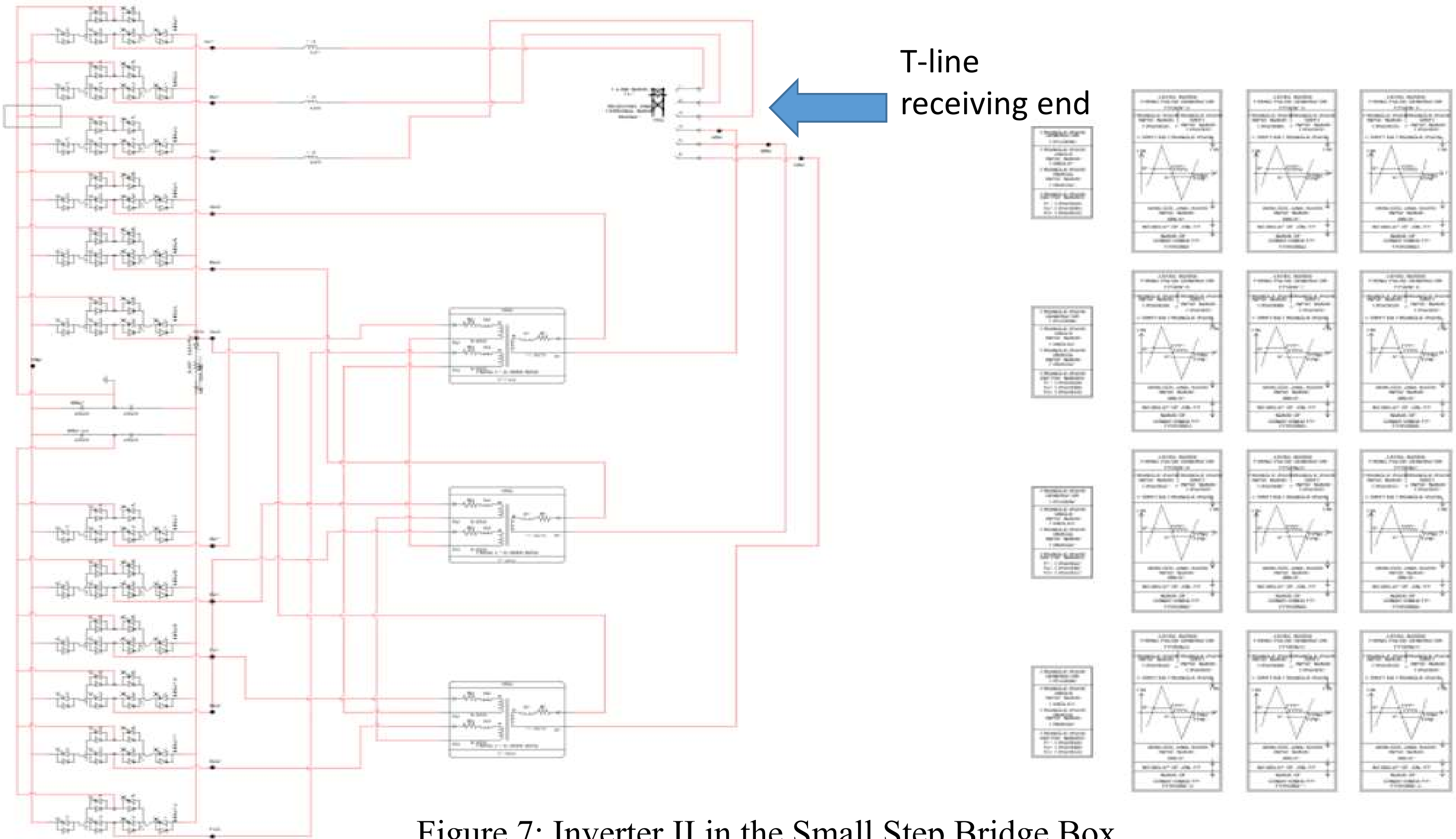
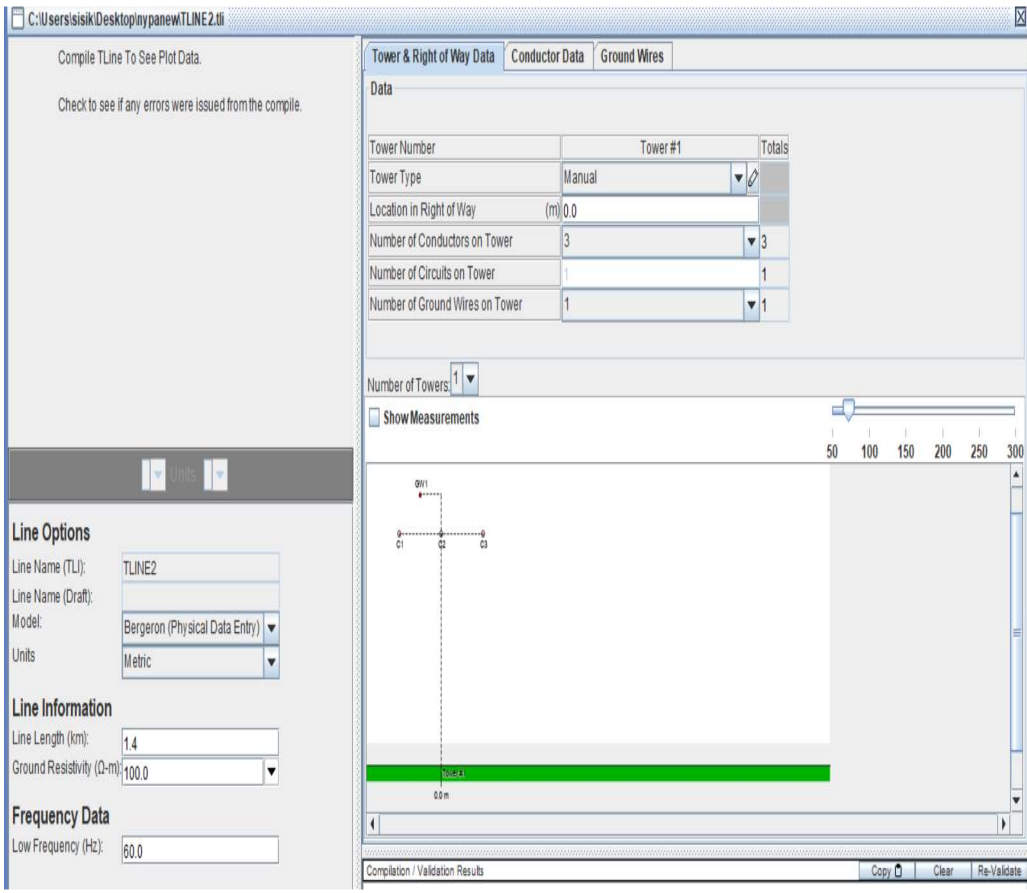
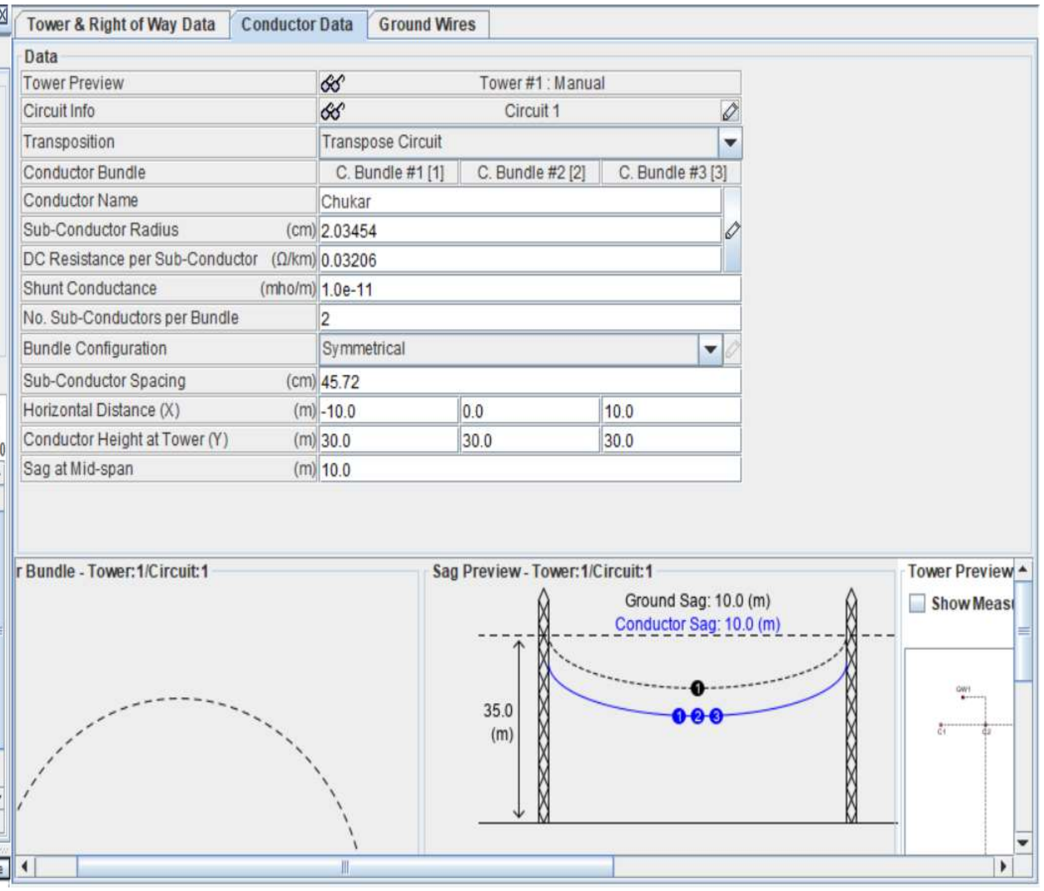


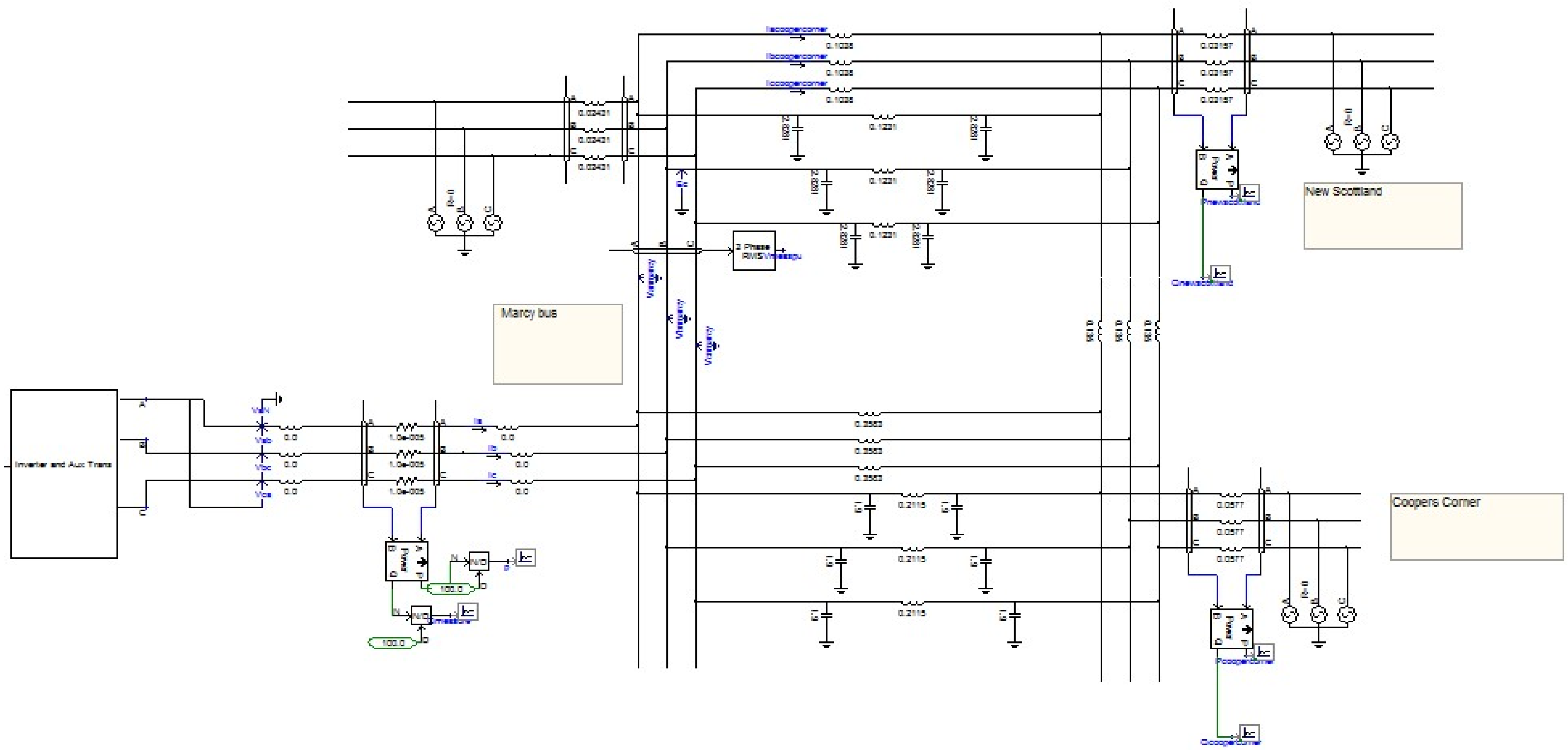

Figure 7: Inverter II in the Small Step Bridge Box

# T-line Parameters

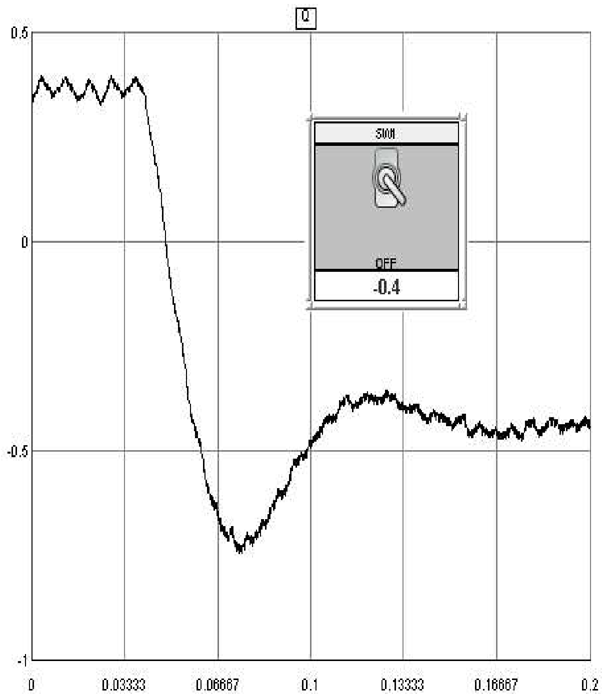


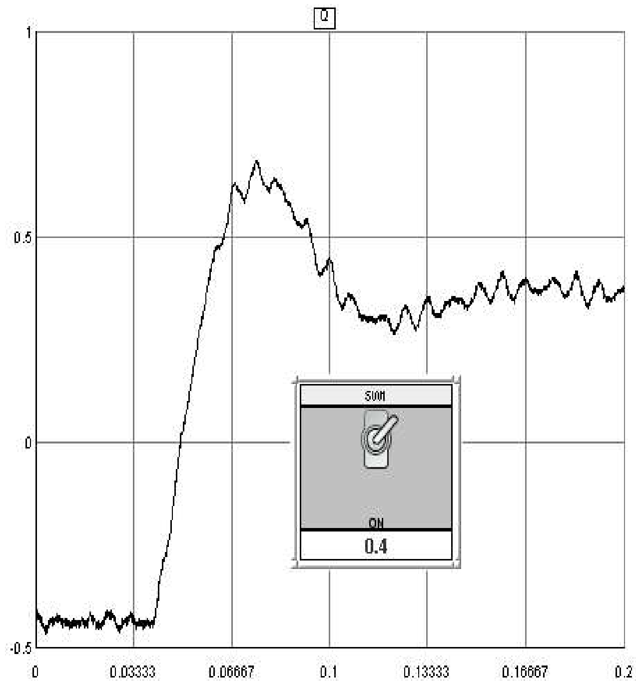
# NYPA STATCOM Connected to NYPA 3 Bus AC System in PSCAD



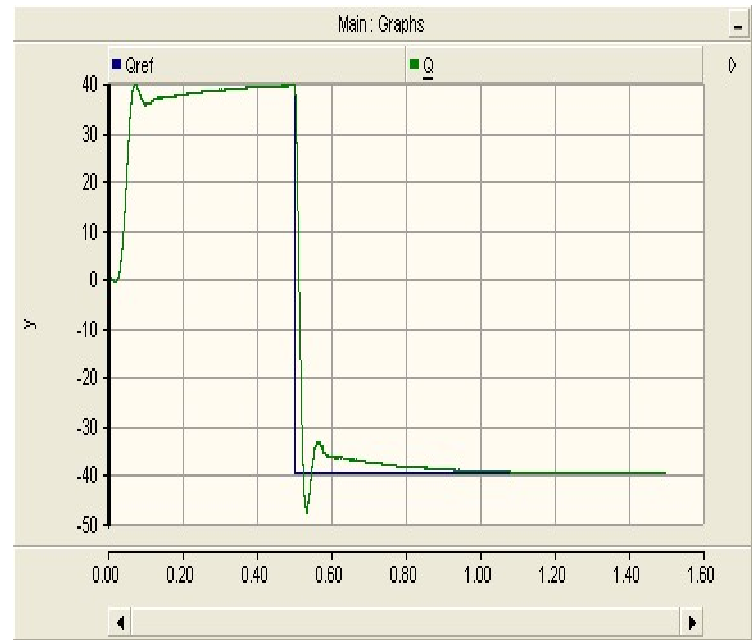
# Controller Performance in RSCAD and PSCAD

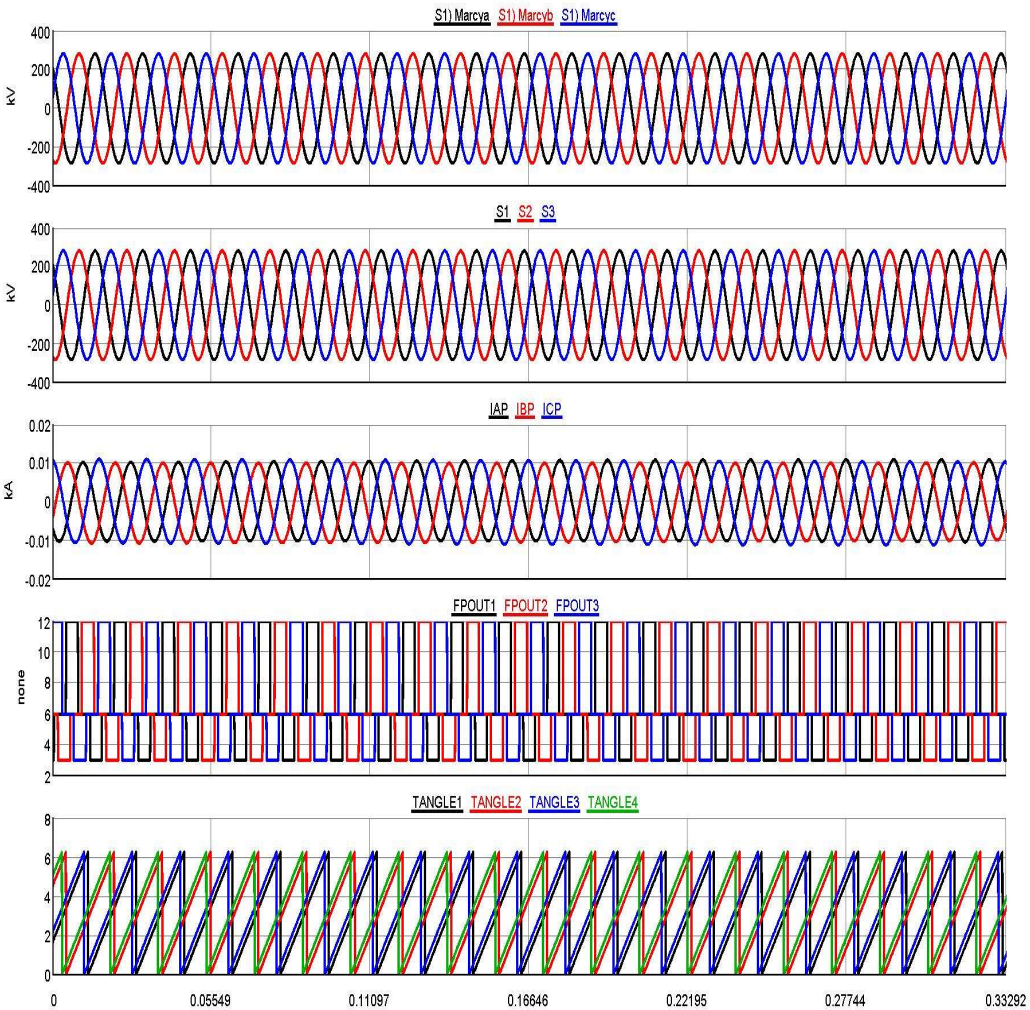



Injected reactive power to the bus after flipping the switch from 0.4pu to -0.4pu.

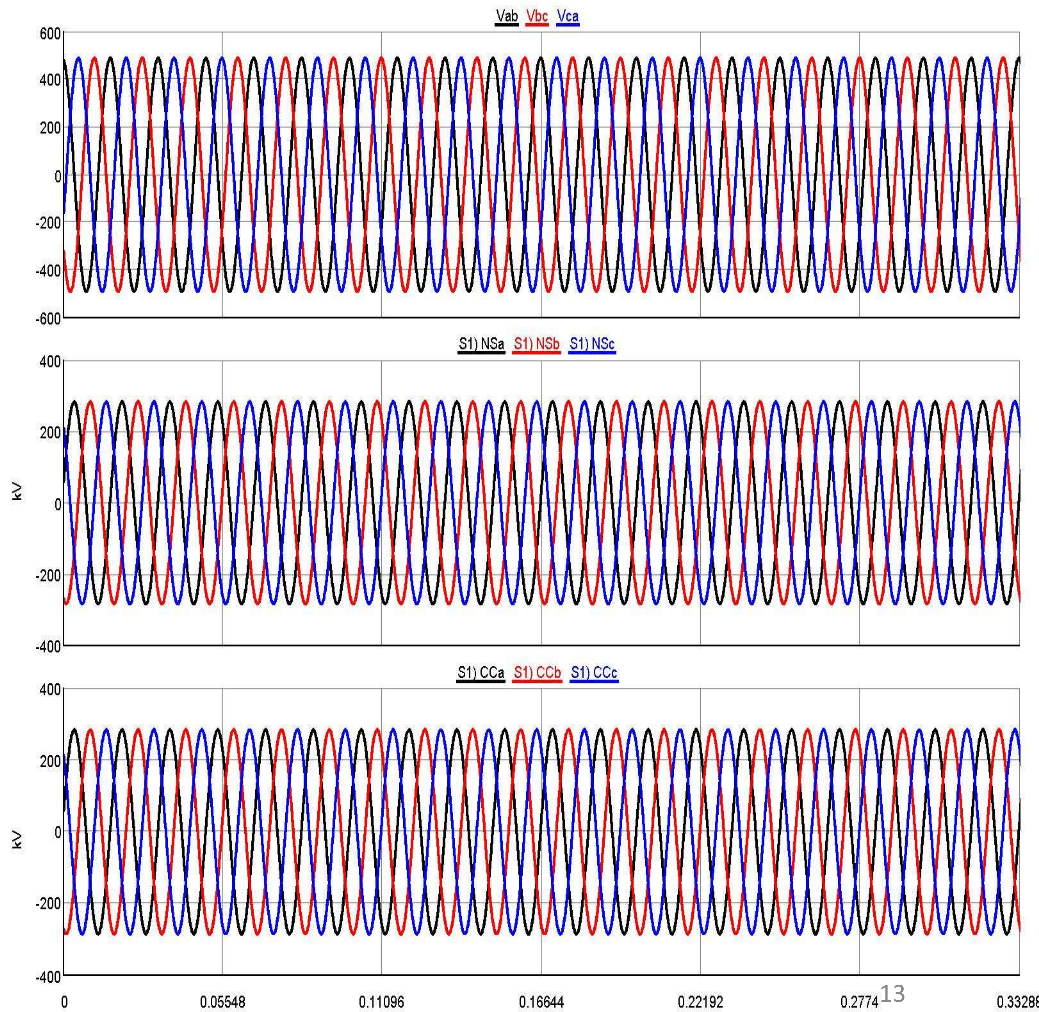



Injected reactive power to the bus after flipping the switch from -0.4 pu to 0.4pu.





S1) Marcya S1) Marcyb S1) Marcyc
kV
S1 S2 S3
kV
IAP IBP ICP
kA
FPOUT1 FPOUT2 FPOUT3
none
TANGLE1 TANGLE2 TANGLE3 TANGLE4
0
0.05549
0.11097
0.16646
0.22195
0.27744
0.33292

Vab Vbc Vca
S1) NSa S1) NSb S1) NSc
kV
S1) CCa S1) CCb S1) CCc
kV
0
0.05548
0.11096
0.16644
0.22192
0.2774
0.33288

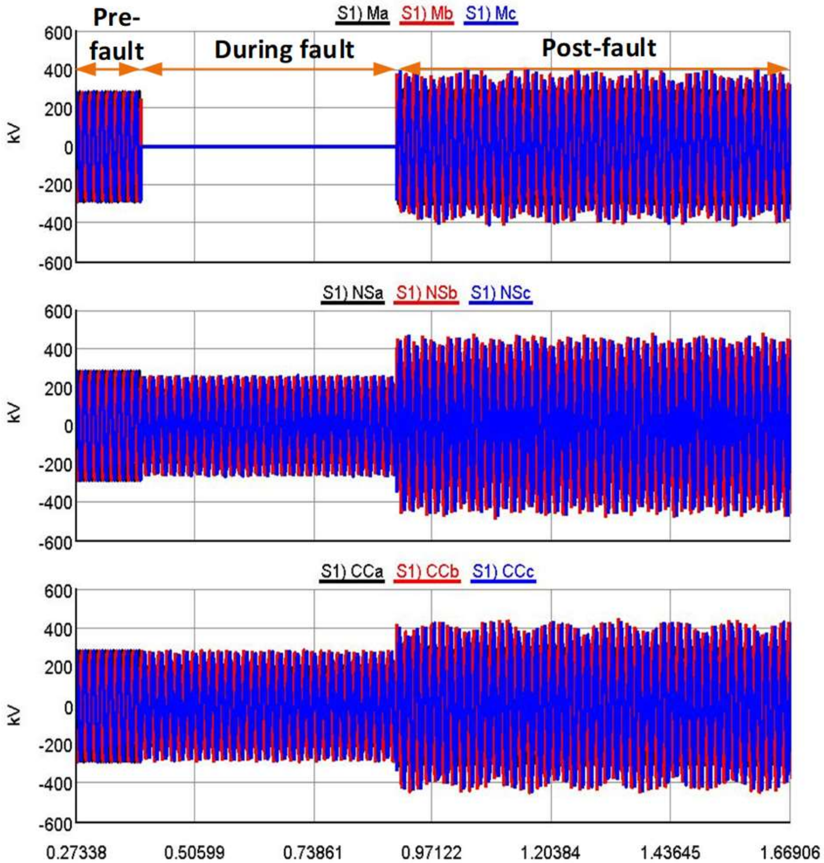



Figure 8: Three Phase to Ground Fault Condition with NPC STATCOM

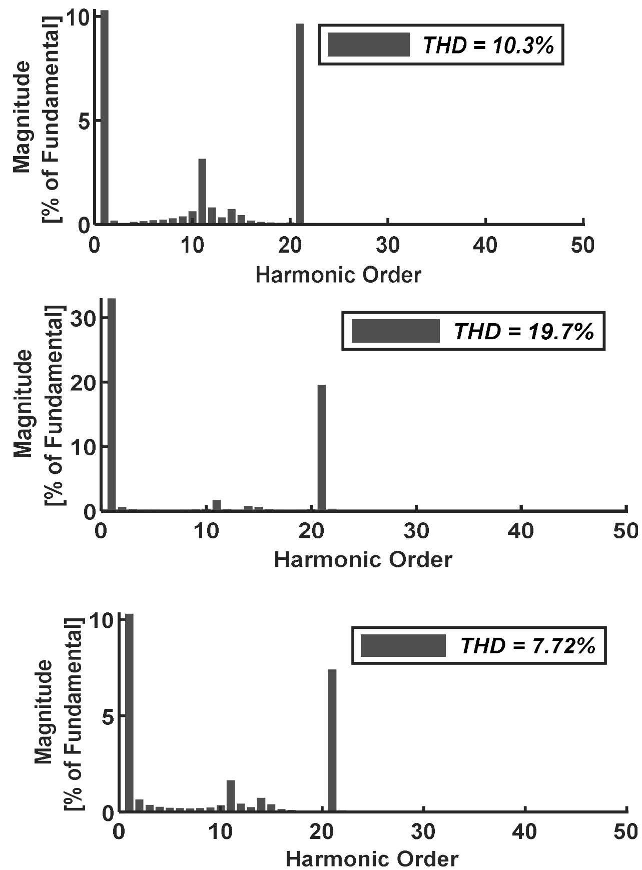
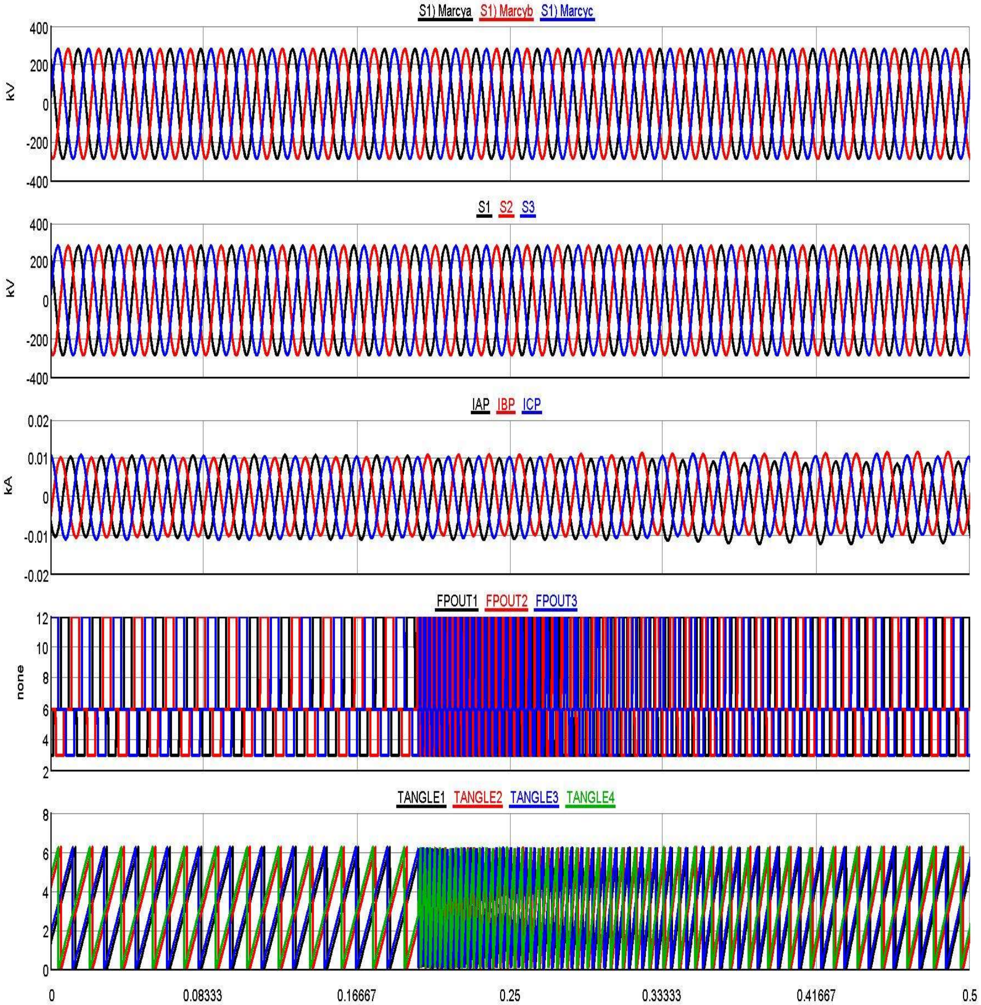
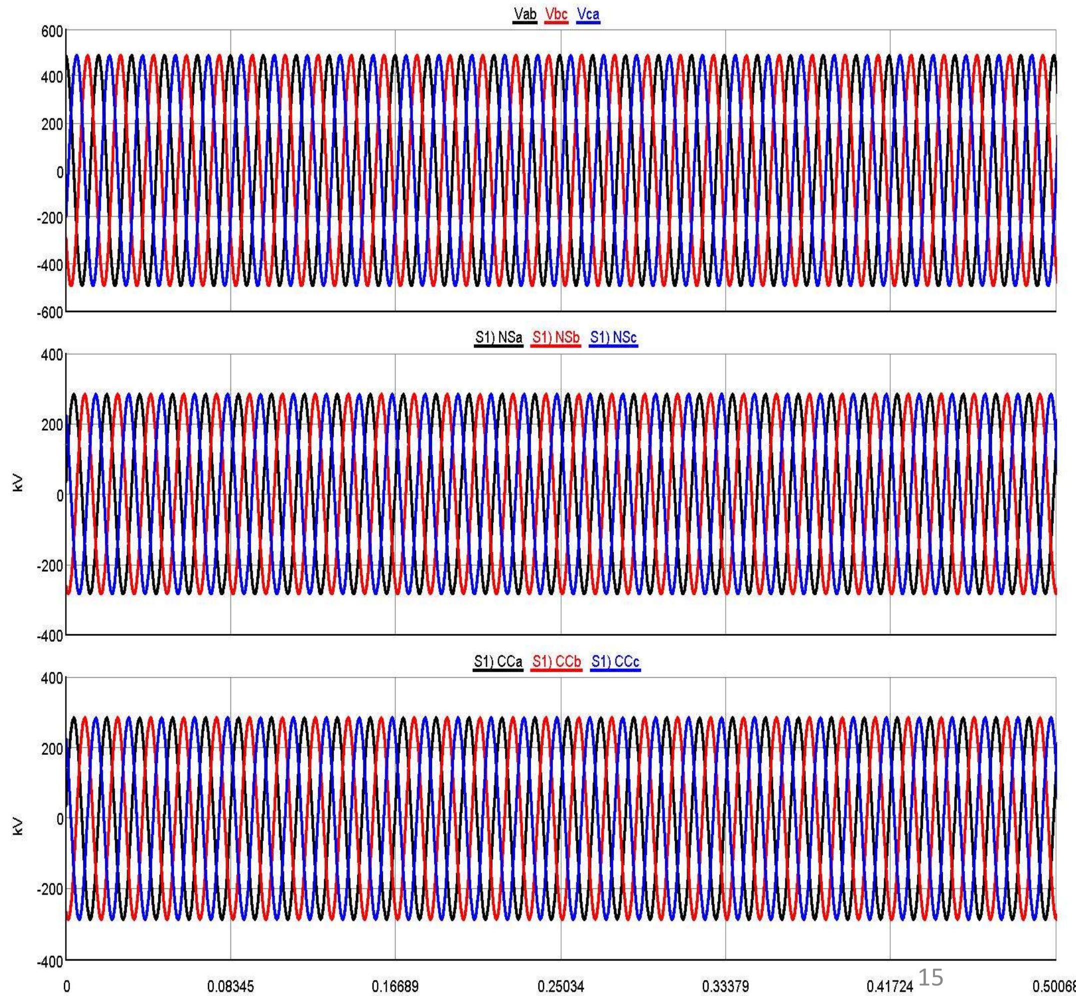


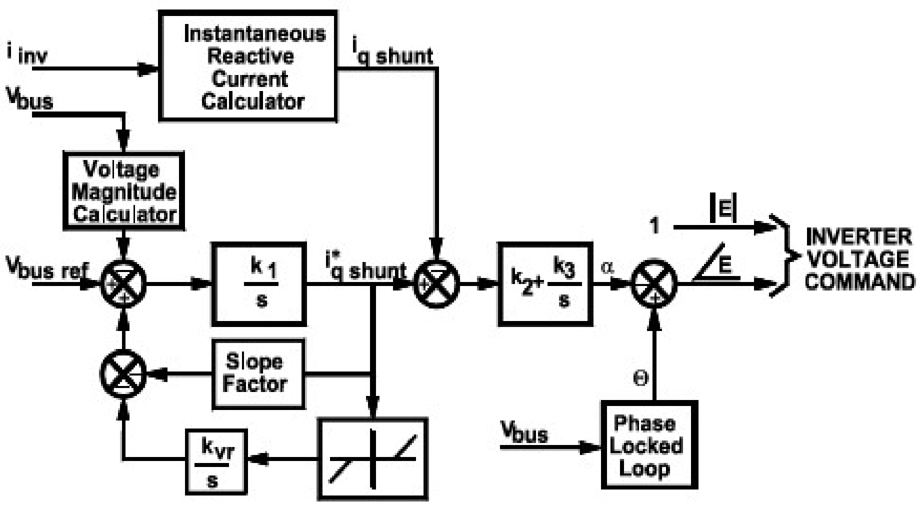

Figure 10: Harmonic Spectrum Analysis of Three-phase Marcy Bus Voltages at Post-fault with NPC STATCOM

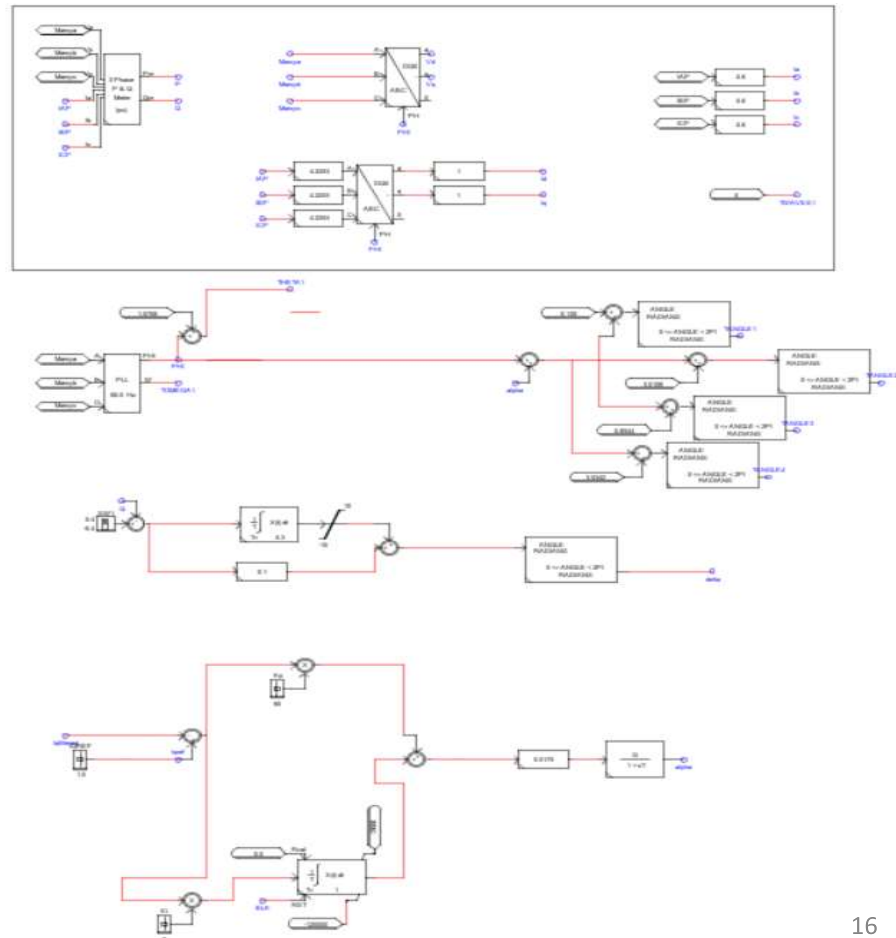
NC STATE UNIVERSITY

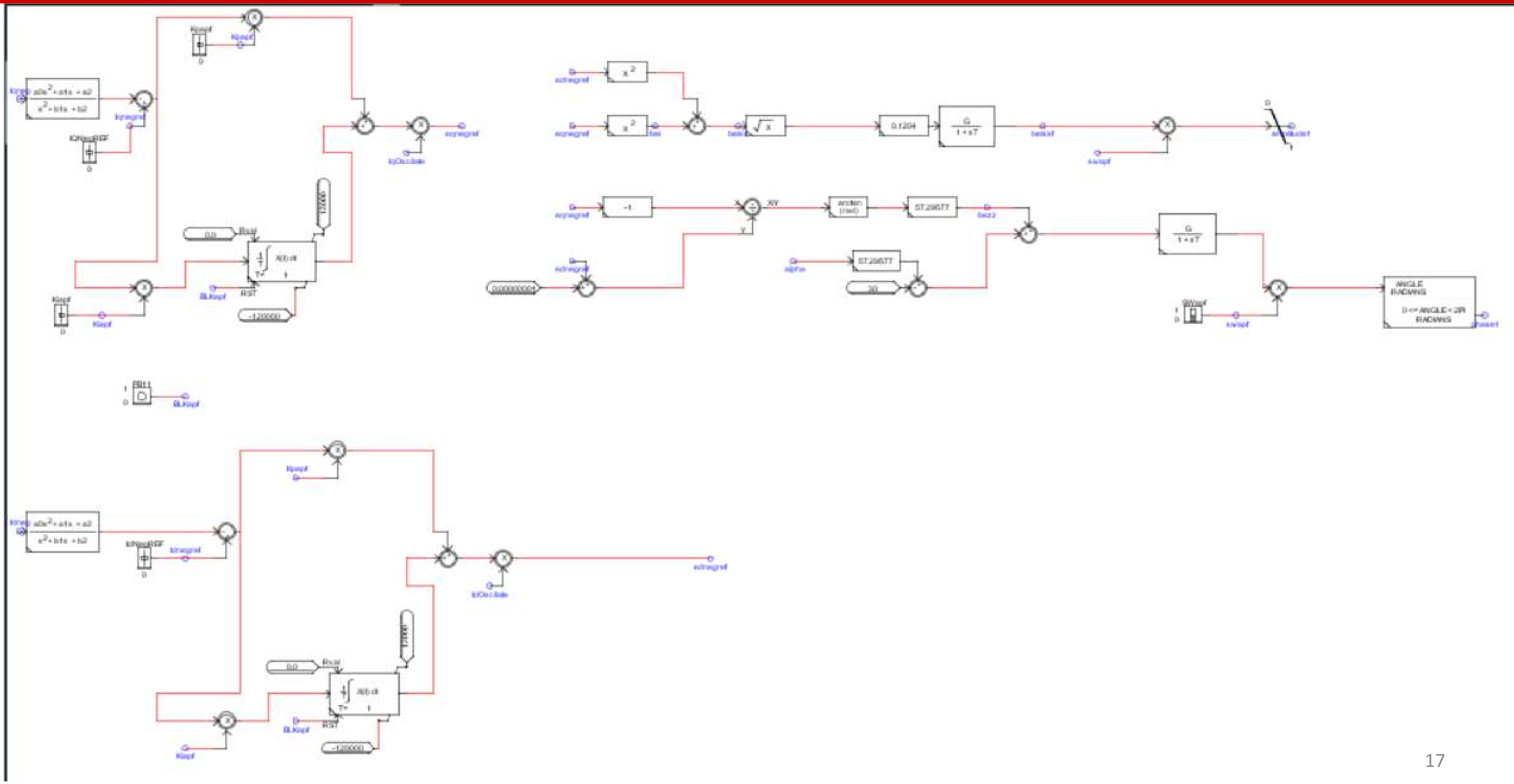


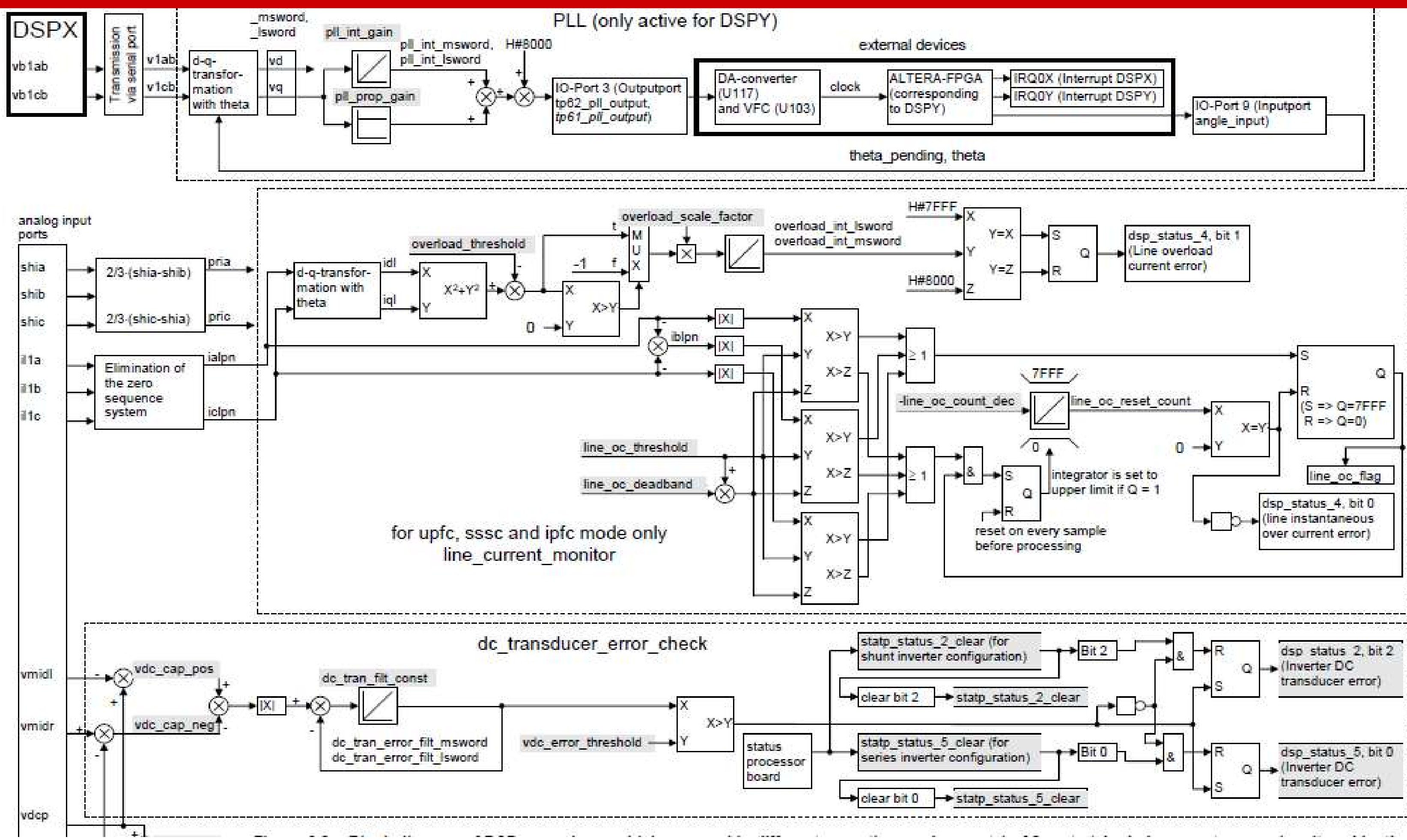
## STATCOM Reactive Current Control





- Source code is written in assembly language.
- The inverter currents, the line currents, and the source voltage angle are transmitted from each inverter to related DSPs to DSPX via serial port.
- DSPX also detects the bus voltages and the line voltages for each inverter via analogue input ports.
- To calculate the fundamental positive sequence system of all the quantities, park transformations is applied then a moving average filter is applied.
- The PLL for the bus voltages is controlled by DSPY.

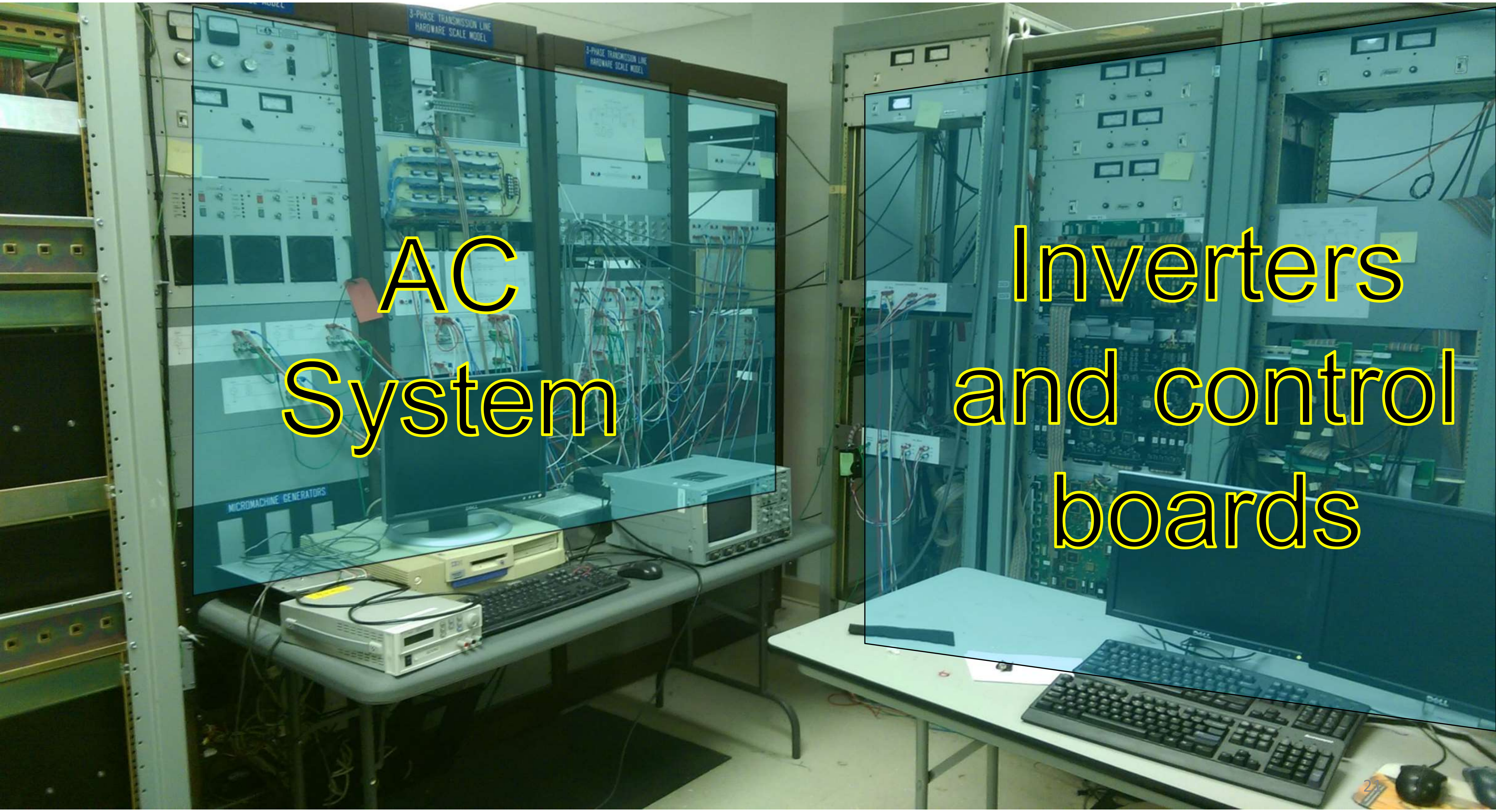


DSPX
vb1ab
vb1cb
Transmission via serial port
v1ab
v1cb
d-q-transfor-mation with theta
vd
vq
_msword, _lsword
pll_int_gain
pll_prop_gain
pll_int_msword, pll_int_lsword
H#8000
PLL (only active for DSPY)
IO-Port 3 (Outputport tp62_pll_output, tp61_pll_output)
external devices
DA-converter (U117) and VFC (U103)
clock
ALTERA-FPGA (corresponding to DSPY)
IRQ0X (Interrupt DSPX)
IRQ0Y (Interrupt DSPY)
IO-Port 9 (Inputport angle_input)
theta_pending, theta
analog input ports
shia
shib
shic
il1a
il1b
il1c
2/3·(shia-shib)
2/3·(shic-shia)
pria
pric
Elimination of the zero sequence system
ialpn
iclpn
d-q-transfor-mation with theta
idl
iql
X²+Y²
overload_threshold
X>Y
overload_scale_factor
overload_int_lsword
overload_int_msword
H#7FFF
H#8000
Y=X
Y=Z
dsp_status_4, bit 1 (Line overload current error)
iblpn
|X|
X>Y
X>Z
≥ 1
7FFF
-line_oc_count_dec
line_oc_reset_count
X=Y
(S => Q=7FFF R => Q=0)
line_oc_threshold
line_oc_deadband
integrator is set to upper limit if Q = 1
reset on every sample before processing
line_oc_flag
dsp_status_4, bit 0 (line instantaneous over current error)
for upfc, sssc and ipfc mode only
line_current_monitor
dc_transducer_error_check
vmidl
vmidr
vdcp
vdc_cap_pos
vdc_cap_neg
dc_tran_filt_const
dc_tran_error_filt_msword
dc_tran_error_filt_lsword
vdc_error_threshold
status processor board
statp_status_2_clear (for shunt inverter configuration)
Bit 2
clear bit 2
statp_status_2_clear
statp_status_5_clear (for series inverter configuration)
Bit 0
clear bit 0
statp_status_5_clear
dsp_status_2, bit 2 (Inverter DC transducer error)
dsp_status_5, bit 0 (Inverter DC transducer error)

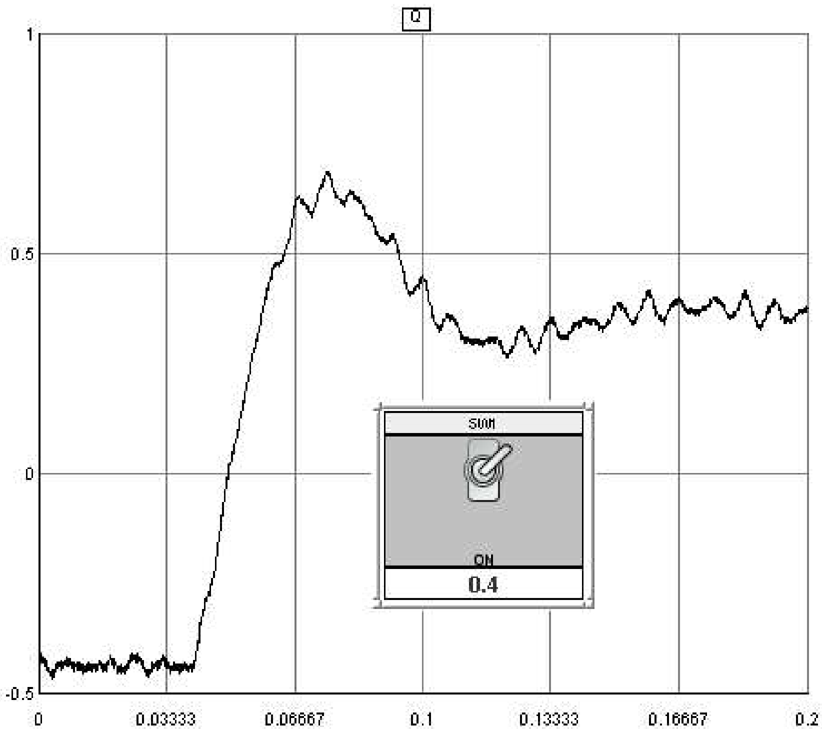
# Transient Network Analyzer (TNA)

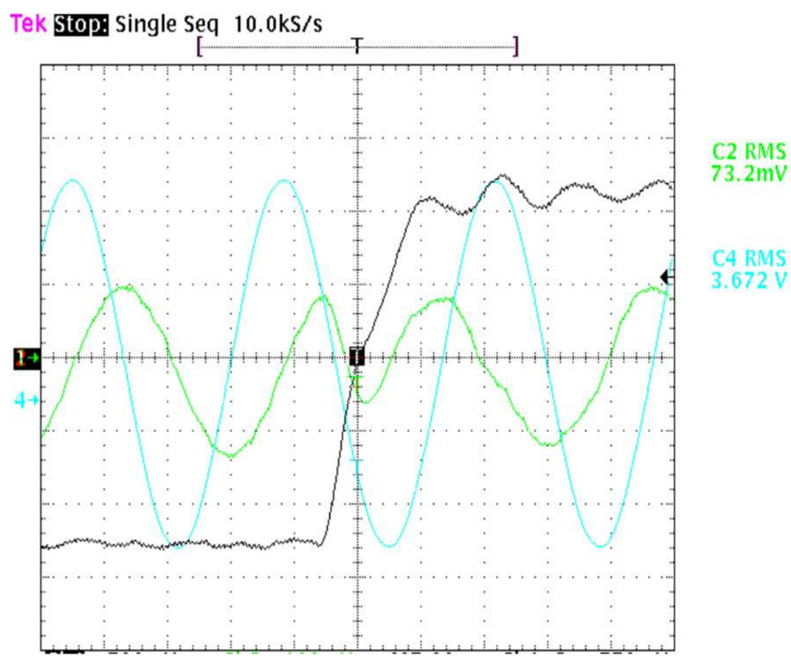
- FREEDM has The Transient Network Analyzer (TNA) which is a scaled-down analog model of the CSC with identical controls and all equipment ratings modified to an equivalent 12VA, 100V system.

- TNA allows injection of low frequency oscillations in source voltage magnitude and angle to allow simulation of transient power system oscillations.


AC System
Inverters and control boards
3-PHASE TRANSMISSION LINE HARDWARE SCALE MODEL
MICROMACHINE GENERATORS

# Comparison between TNA and RTDS

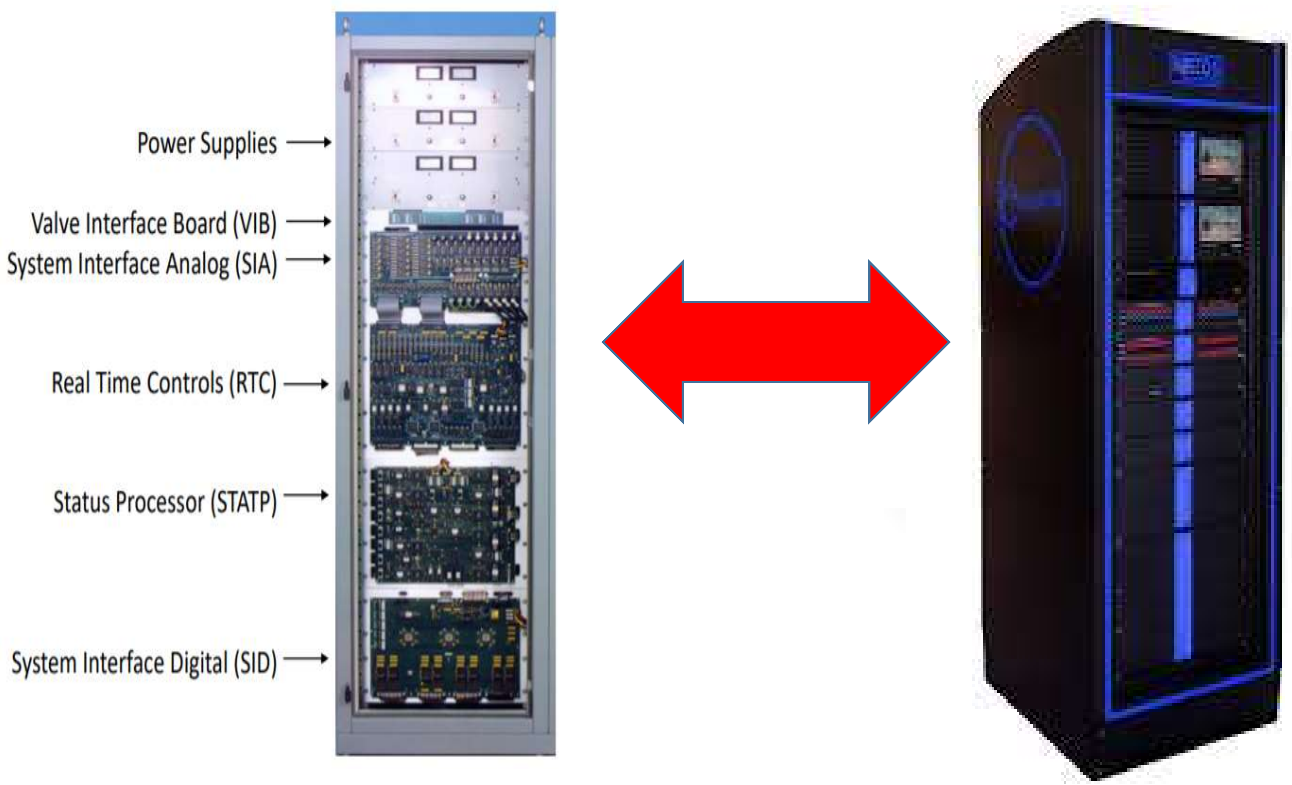


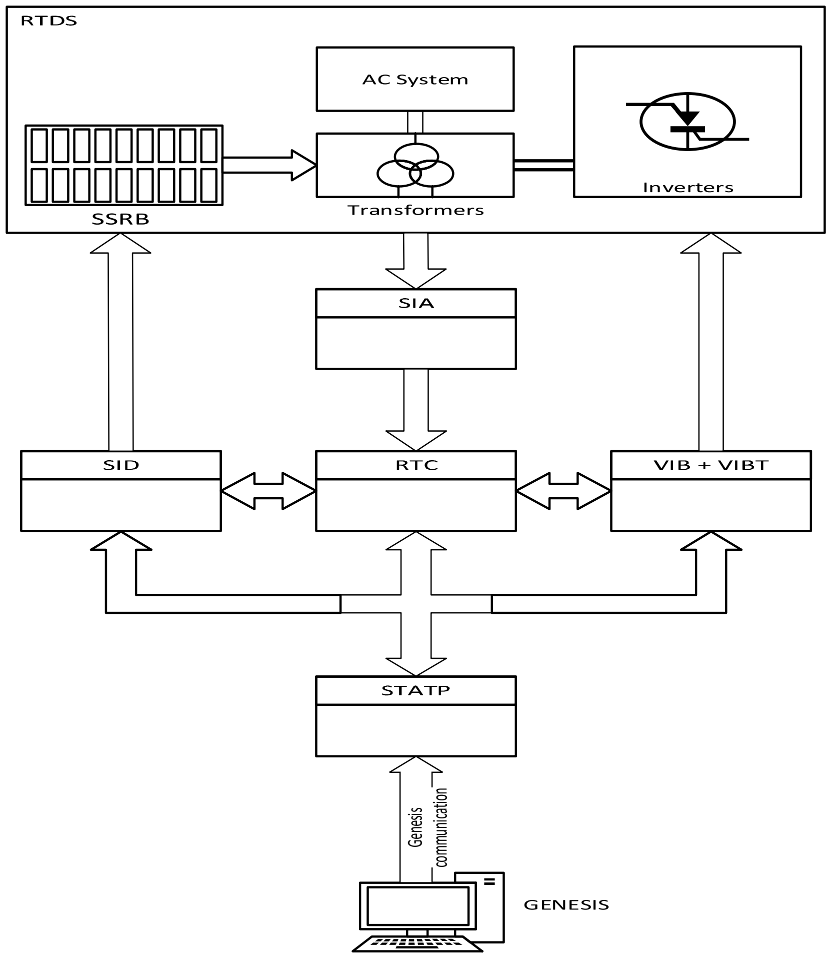



- There are three signal Processors on the Real Time Control Board (RTC).
- DSPX is used for housekeeping on the RTC board while DSPY (Inverter 1) and DSPZ (Inverter 2) are responsible for the inverters.
- Shunt Control is the most complex of the four control modes with an outer (voltage ) loop and an inner (current) loop working in series to generate the control angles.
- The outer control loop derives the set point value of the reactive current controller (i*qshunt) from the bus voltage controller. The reactive current component of the inverter currents (iqshunt) is derived via a transformation into a rotating dq-reference frame. The reference angle for the transformation is the bus voltage angle derived from the phase locked loop.

- The CSC may have one or both of its inverters configured for Shunt Control. Normally the shunt connected inverter operates as a STATCOM.
- It generates reactive power. However, when the shunt connected inverter is part of a UPFC it must also be able to generate real power. Therefore its DC capacitor is connected to the DC capacitor of the UPFC series inverter.
- When the shunt inverter is in STATCOM mode the DC capacitors of the two inverters remain disconnected. The shunt connected inverter always retains (indirect) control of the DC capacitor voltage and uses the variation in its magnitude to control the magnitude of the shunt inverter's output voltage and current.
- A fixed control ratio between the DC voltage and the amplitude of the inverter output voltage space vector is used for shunt inverter operation i.e. the width of the zero step in its output voltage waveform remains fixed

# C-HIL Implementation (In Progress)




RTDS
AC System
SSRB
Transformers
Inverters
SIA
SID
RTC
VIB + VIBT
STATP
Genesis communication
GENESIS

# Thank you!

sisik@ncsu.edu – hnath@ncsu.edu