




HOW TO AVOID RELAY MISOPERATIONS DUE TO WRONG SETTINGS OR FIRMWARE BUGS

J. Holbach May 2019

RTDS User Group Meeting in Denver

QUANTA TECHNOLOGY

Smart Solutions, Practical Results

Overview

- Introduction
- Test Application
- Results
- Test Automation Process
- Conclusion

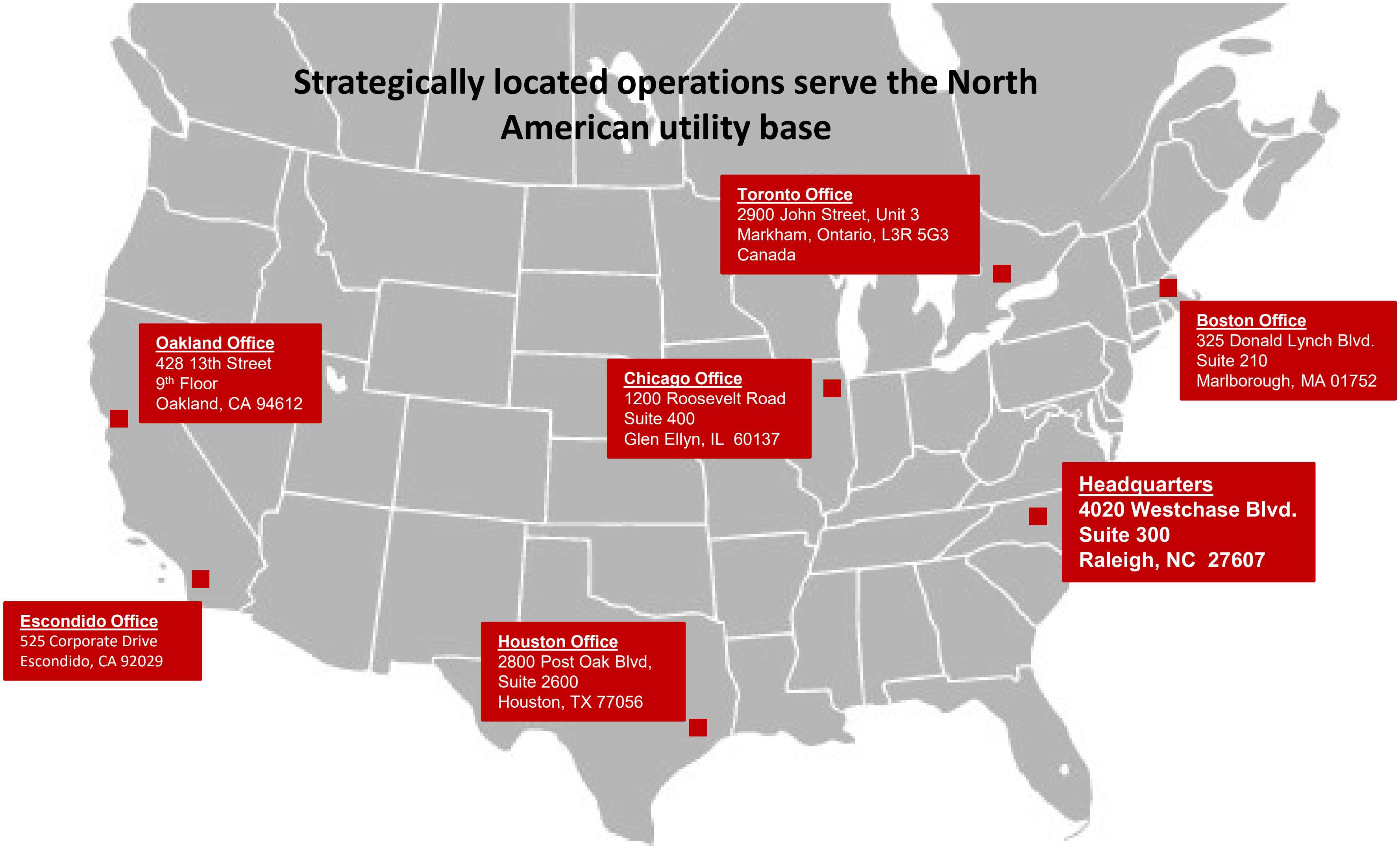
Smart Solutions, Real Results

- **Premium technical & business consulting**
- **Independent arm of Quanta Services**
- **Industry thought leaders: practical experts**
- **Headquarters in Raleigh, NC**
- **U.S. and international regional offices**
- **Extensive T&D Experience**

We are . . .

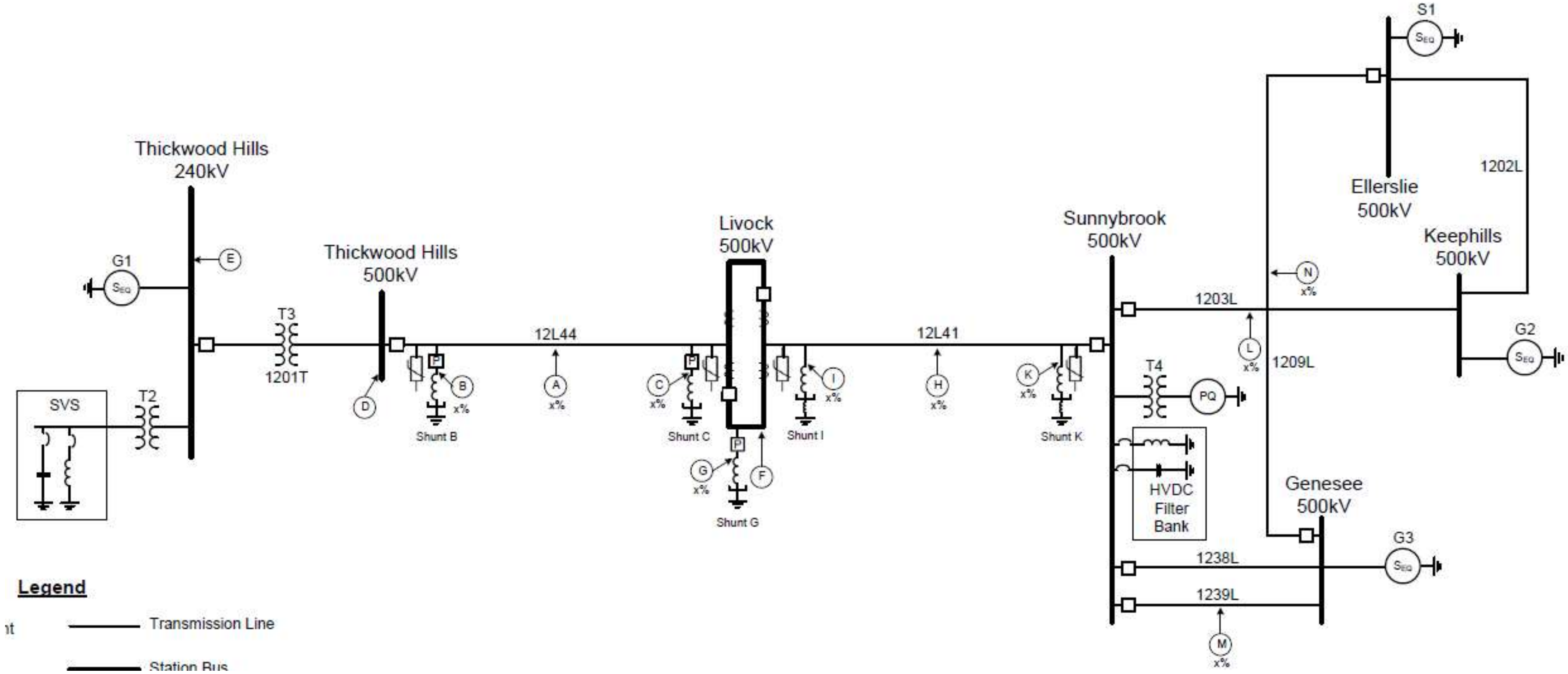
- Seasoned staff including former utility executives and engineers with 25+ years of practical experience serving utility industry
- Talented mid-level and junior staff poised to become industry leaders
- Many patents, books and published articles
- Thought leaders, actively involved in development of industry standards and evolving planning and operation practices
- Advanced Degrees, Professional Licenses & Certifications (PhD, PE, MBA, PMP), IEEE Fellows

Quanta Technology Locations



Alberta PowerLine

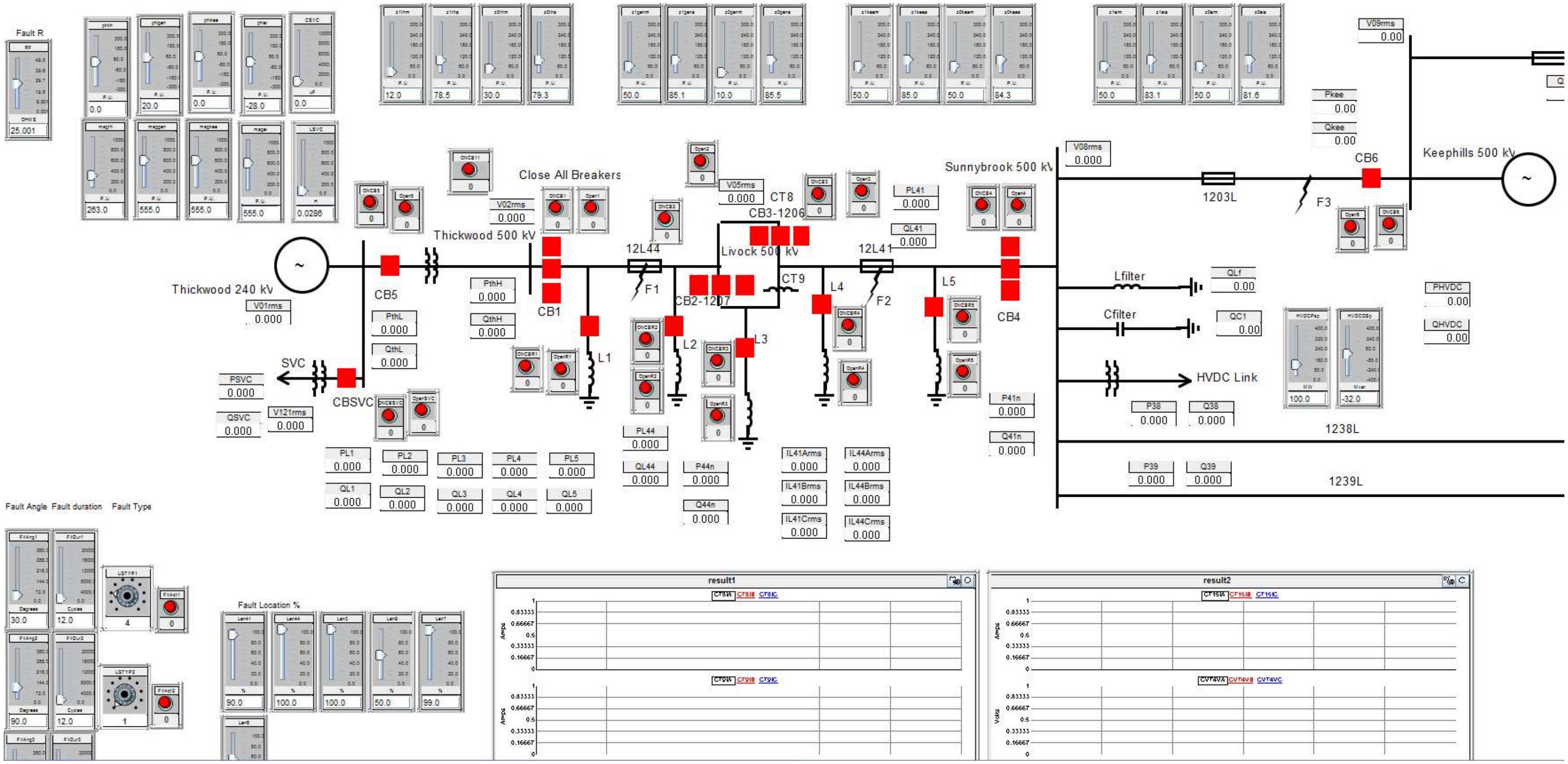
Fort McMurray West 500 kV Transmission Project



Test Application

- Test included test of protection and control devices for two 500kV transmission lines
  - 12L41 is a ~415km shunt compensated transmission line connecting Livock substation to Sunnybrook substation (an AltaLink owned/operated substation)
  - 12L44 is a ~100km shunt compensated transmission line connecting Livock substation to Thickwood Hills substation
  - Shunt reactors are installed at each line terminal
  - 500kV line protection is provided by two primary distance protection systems using Siemens 7SA522 devices for system ‘A’ and SEL-421-5 devices for system ‘B’.
  - The systems utilize high-speed communications assisted permissive over-reaching transfer trip (POTT), direct under-reaching transfer trip (DUTT) and direct transfer trip(DTT) schemes with time graded stepped distance elements for communications independent backup protection
  - Shunt Reactor Protection include the REC670 and SEL-487E devices

RTDS HMI

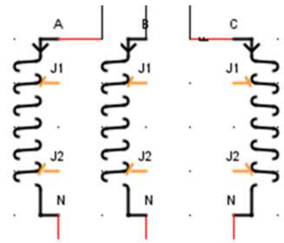


Fault R
Close All Breakers
Thickwood 500 kV
Thickwood 240 kV
CB5
CB1
SVC
CBSVC
12L44
F1
L1
L2
CB2-1207
CT8
CB3-1206
Livock 500 kV
CT9
L3
L4
12L41
F2
L5
Sunnybrook 500 kV
CB4
1203L
F3
CB6
Keephills 500 kV
Lfilter
Cfilter
HVDC Link
1238L
1239L
Fault Angle
Fault duration
Fault Type
Fault Location %
result1
result2

Alberta PowerLine : HIL Test Set-Up

New RTDS Shunt Reactor Model

Non-Linear model of Shunt Reactor

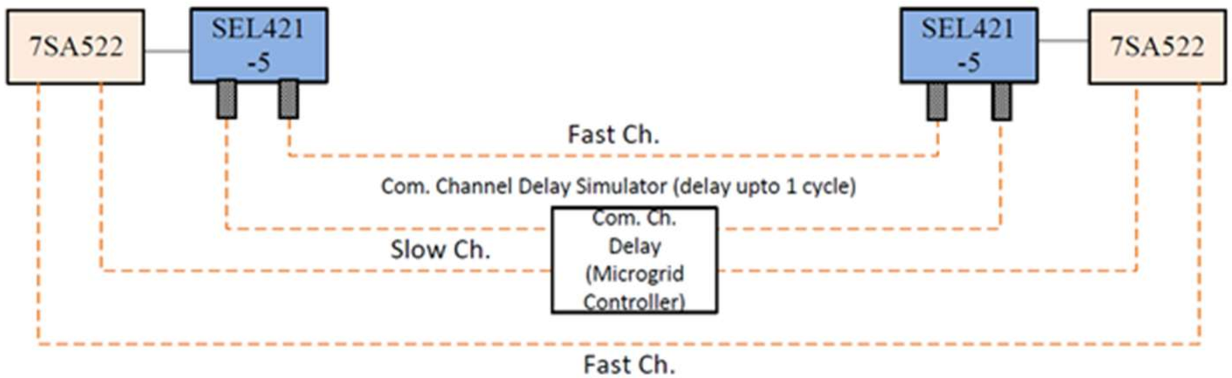


Name	Description	Value	Unit
Name	Component Name	SR1A	
TName	Terminal Label	A	
cnfg	Format of Reactor Electrical Data Input:	MVAR	
VbsIn	Rated RMS Line-to-Neutral Voltage:	303.11	kV
HTZ	Base Frequency:	60.0	Hertz
Rmvar	Rated MVAR of the Reactor:	16.7	MVAR
XSR	Reactor Total Reactance	387.2	Ohm
CuL	Copper Losses:	2e-3	p.u.
Coretyp	Type of the Reactor Magnetic Core	Iron Core	
satur	Specification of Reactor Saturation Curve	Points	
Xl	Reactor Leakage Reactance	0.3	p.u.
MfacAir	Mutual Coupling Coefficient of Sub-Windings (<1.0) for Air-Path Flux	0.0	
FLTprc1	Percentage of the 1st Point of Fault from the Neutral	50	%
FLTprc2	Percentage of the 2nd Point of Fault from the Neutral	30	%
Icon	Show component icons as	Small	

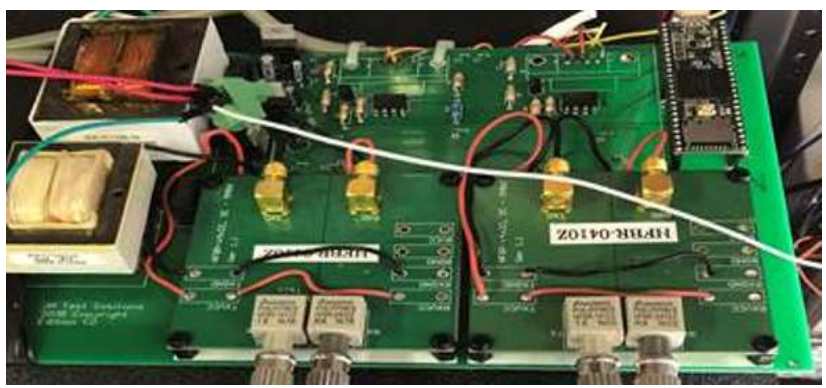
- It contains three sub-windings and two junction nodes in addition to the terminal nodes.
- The model allows users to apply turn-to-turn and turn-to-ground faults for a single-phase shunt reactor.
- The user has the option of specifying reactor core type: air-core or iron-core.

Communication Delay Simulation

- A communication latency of 16 ms had to be simulated
- Logic of relay cannot be changed for test!



- No commercial solution was available-> Quanta Technology developed customized solution for this test



Test Plan-Functional Tests

7.1.1 Basic Internal Faults

- Temporary metallic internal faults
- Fault duration = 200 ms (12 cycles)
- Only fast communication channel is active in Siemens and SEL protection
- Cases #1a, #1b: Heavy load with system normal is simulated
- Faults locations H (note: locations I and K are considered in reactor functional tests).

Table 7-1-1: Internal Faults

Test Case #	Fault Location	Percent	Fault Type	Fault Duration [cycle]	Fault Angle	Fault Resistor	Load
L41_1101	H	0.00	BG	12	0	0.01	Case#1a
L41_1102	H	0.00	AG	12	0	0.01	Case#1b
L41_1103	H	0.00	ABG	12	30	0.01	Case#1b
L41_1104	H	0.00	BC	12	60	0.01	Case#1a
L41_1105	H	0.00	ABC	12	90	0.01	Case#1b
L41_1106	H	10.00	BG	12	0	0.01	Case#1a
L41_1107	H	10.00	CG	12	0	0.01	Case#1b
L41_1108	H	10.00	BCG	12	30	0.01	Case#1b
L41_1109	H	10.00	CA	12	60	0.01	Case#1a
L41_1110	H	10.00	ABC	12	90	0.01	Case#1b
L41_1111	H	30.00	CG	12	0	0.01	Case#1a
L41_1112	H	30.00	AG	12	0	0.01	Case#1b
L41_1113	H	30.00	CAG	12	30	0.01	Case#1b
L41_1114	H	30.00	AB	12	60	0.01	Case#1a
L41_1115	H	30.00	ABC	12	90	0.01	Case#1b
L41_1116	H	50.00	AG	12	0	0.01	Case#1a
L41_1117	H	50.00	CG	12	0	0.01	Case#1b
L41_1118	H	50.00	ABG	12	30	0.01	Case#1b
L41_1119	H	50.00	BC	12	60	0.01	Case#1a
L41_1120	H	50.00	ABG	12	90	0.01	Case#1b
L41_1121	H	70.00	AG	12	0	0.01	Case#1a
L41_1122	H	70.00	BG	12	0	0.01	Case#1b
L41_1123	H	70.00	ABG	12	30	0.01	Case#1b
L41_1124	H	70.00	BC	12	60	0.01	Case#1a
L41_1125	H	70.00	ABC	12	90	0.01	Case#1b
L41_1126	H	90.00	AG	12	0	0.01	Case#1a
L41_1127	H	90.00	BG	12	0	0.01	Case#1b
L41_1128	H	90.00	ABG	12	30	0.01	Case#1b
L41_1129	H	90.00	BC	12	60	0.01	Case#1a
L41_1130	H	90.00	ABC	12	90	0.01	Case#1b
L41_1131	H	100.00	BCG	12	0	0.01	Case#1a
L41_1132	H	100.00	CA	12	30	0.01	Case#1b
L41_1133	H	100.00	ABC	12	60	0.01	Case#1a
L41_1134	H	100.00	CG	12	90	0.01	Case#1b
L41_1135	H	100.00	BG	12	90	0.01	Case#1a

Test Plan-Batch Tests

7.3 12L41 Protection Operating Time Batch Tests

After the functional testing, the final settings will be tested with extensive operating time batch tests simulating internal line faults and external system faults. The batch tests shall be configured to simulate the conditions listed below.

Internal Batch Tests (Per Appendix D of the AESO Functional Specification)

- Three fault locations will be tested: H(0%), H(50%) and H(100%)
- At each fault location all ten fault types are to be applied: AG, BG, CG, AB, BC, CA, ABG, BCG, CAG and ABC
- Ground faults will consider 0Ω fault resistance (per AESO documentation, defined clearing times for ground faults are for solid ground faults)
- For each fault type the following fault inception angles are to be applied: 0, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110 and 120 deg. of phase A
- The above tests will be carried out considering the following load flow/system contingency cases: #1a, #1b, #3, #4 and #5
- Each test will include line energization with a stabilization period (>4s) followed by the fault event. Energization from both terminals is possible, thus, tests will be configured in a way that energization will be simulated from alternating terminals.

External Batch Tests

- Six fault locations will be tested: C(0%), A(50%), A(100%), L(0%), L (100%), M(100%)
- At each fault location all ten fault types are to be applied: AG, BG, CG, AB, BC, CA, ABG, BCG, CAG and ABC
- Ground faults will consider 0Ω fault resistance
- For each fault type the following fault inception angles are to be applied: 0, 30, 60, 90 deg. of phase A
- The above tests will be carried out considering the following load flow/system contingency cases: #1a, #1b, #3, #4 and #5
- Simulated adjacent clearing times to include: high speed clearing (i.e. communications assisted) and delayed clearing (i.e. communications failure or breaker failure).

AESO Timing Requirements

Location	Multi-phase Faults	Single Line To Ground Faults
Line Near-end Clearing Time	3.5 cycles	4.5 cycles
Line Far-end Clearing Time	4.5 cycles	5.5 cycles
Substation Fault Clearing Time	3.5 cycles	4.5 cycles
Breaker Failure Near-end Clearing Time	9.0 cycles	10.0 cycles
Breaker Failure Far-end Clearing Time	10.0 cycles	11.0 cycles

Test Results

- Approx. 3500 cases were tested in 3 weeks
- During functional Test (ca. 200 tests)
  - 2 critical setting problems where found
    - Switch onto fault pick-up level was to sensitive
    - Overreach of zone 1
  - 5 setting improvements where detected and implemented
    - Incorrect logic
    - Timer adjustments
- One critical firmware issue was found during sophisticated batch test of 3500 test (requirement of AESO)
  - Firmware bug caused wrong direction determination for external fault
  - Quanta Technology supported customer and manufacturer during the revision of the firmware
- Communication delay simulation devices was developed particular for this test

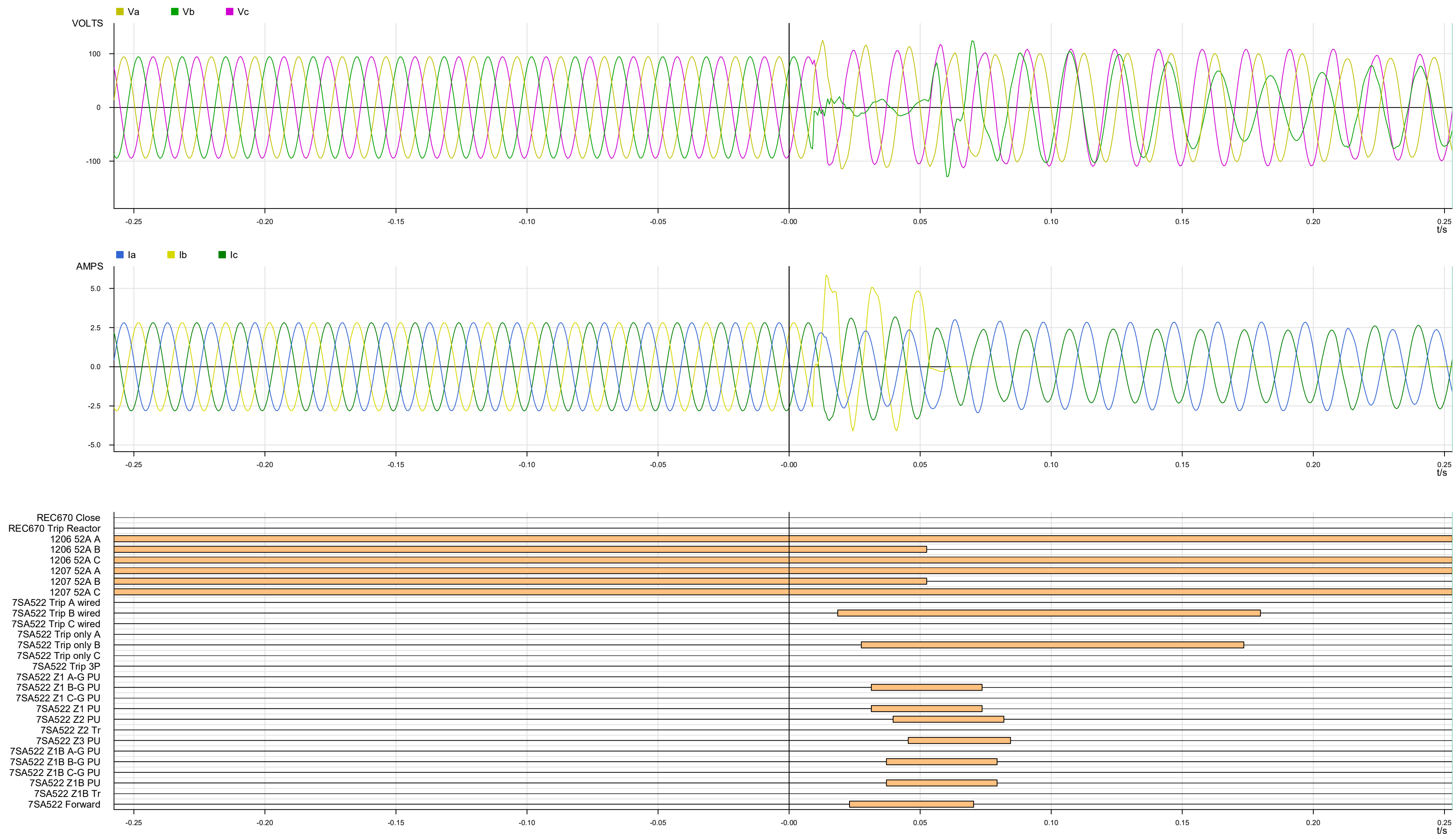
Result Table for 1200 External Faults

	Case	Line	Location	Type	Resitor	Angle	Load					REC670 Close	REC670 Trip Reactor	1206 52A A (RTDS)	1206 52A B (RTDS)	1206 52A C (RTDS)	1207 52A A (RTDS)	1207 52A B (RTDS)	1207 52A C (RTDS)
BatchEx	245	C	0	2	0.001	0	1b 1 0		1	LivockLine1	245	1044.48	Low	High	43.52	High	High	43.52	High
BatchEx	323	A	100	1	0.001	60	1b 1 0		1	LivockLine1	323	1036.16	Low	43.52	High	High	43.52	High	High
BatchEx	324	A	100	1	0.001	90	1b 1 0		1	LivockLine1	324	1035.52	Low	42.88	High	High	42.88	High	High
BatchEx	325	A	100	2	0.001	0	1b 1 0		1	LivockLine1	325	1040	Low	High	42.88	High	High	42.88	High
BatchEx	346	A	100	7	0.001	30	1b 1 0		1	LivockLine1	346	Low	Low	42.88	42.88	42.88	42.88	42.88	42.88
BatchEx	350	A	100	8	0.001	30	1b 1 0		1	LivockLine1	350	Low	Low	42.88	43.52	43.52	42.88	43.52	43.52
BatchEx	1	C	0	1	0.001	0	1a 1 0		0	LivockLinelt1	1	Low	Low	High	High	High	High	High	High
BatchEx	2	C	0	1	0.001	30	1a 1 0		0	LivockLinelt1	2	Low	Low	High	High	High	High	High	High
BatchEx	3	C	0	1	0.001	60	1a 1 0		0	LivockLinelt1	3	Low	Low	High	High	High	High	High	High
BatchEx	4	C	0	1	0.001	90	1a 1 0		0	LivockLinelt1	4	Low	Low	High	High	High	High	High	High
BatchEx	5	C	0	2	0.001	0	1a 1 0		0	LivockLinelt1	5	Low	Low	High	High	High	High	High	High
BatchEx	6	C	0	2	0.001	30	1a 1 0		0	LivockLinelt1	6	Low	Low	High	High	High	High	High	High
BatchEx	7	C	0	2	0.001	60	1a 1 0		0	LivockLinelt1	7	Low	Low	High	High	High	High	High	High
BatchEx	8	C	0	2	0.001	90	1a 1 0		0	LivockLinelt1	8	Low	Low	High	High	High	High	High	High
BatchEx	9	C	0	3	0.001	0	1a 1 0		0	LivockLinelt1	9	Low	Low	High	High	High	High	High	High
BatchEx	10	C	0	3	0.001	30	1a 1 0		0	LivockLinet1	10	Low	Low	High	High	High	High	High	High
BatchEx	11	C	0	3	0.001	60	1a 1 0		0	LivockLinet1	11	Low	Low	High	High	High	High	High	High
BatchEx	12	C	0	3	0.001	90	1a 1 0		0	LivockLinet1	12	Low	Low	High	High	High	High	High	High
BatchEx	13	C	0	4	0.001	0	1a 1 0		0	LivockLinet1	13	Low	Low	High	High	High	High	High	High
BatchEx	14	C	0	4	0.001	30	1a 1 0		0	LivockLinet1	14	Low	Low	High	High	High	High	High	High
BatchEx	15	C	0	4	0.001	60	1a 1 0		0	LivockLinet1	15	Low	Low	High	High	High	High	High	High
BatchEx	16	C	0	4	0.001	90	1a 1 0		0	LivockLinet1	16	Low	Low	High	High	High	High	High	High
BatchEx	17	C	0	5	0.001	0	1a 1 0		0	LivockLinet1	17	Low	Low	High	High	High	High	High	High
BatchEx	18	C	0	5	0.001	30	1a 1 0		0	LivockLinet1	18	Low	Low	High	High	High	High	High	High
BatchEx	19	C	0	5	0.001	60	1a 1 0		0	LivockLinet1	19	Low	Low	High	High	High	High	High	High
BatchEx	20	C	0	5	0.001	90	1a 1 0		0	LivockLinet1	20	Low	Low	High	High	High	High	High	High
BatchEx	21	C	0	6	0.001	0	1a 1 0		0	LivockLinet1	21	Low	Low	High	High	High	High	High	High
BatchEx	22	C	0	6	0.001	30	1a 1 0		0	LivockLinet1	22	Low	Low	High	High	High	High	High	High
BatchEx	23	C	0	6	0.001	60	1a 1 0		0	LivockLinet1	23	Low	Low	High	High	High	High	High	High
BatchEx	24	C	0	6	0.001	90	1a 1 0		0	LivockLinet1	24	Low	Low	High	High	High	High	High	High
BatchEx	25	C	0	7	0.001	0	1a 1 0		0	LivockLinet1	25	Low	Low	High	High	High	High	High	High
BatchEx	26	C	0	7	0.001	30	1a 1 0		0	LivockLinet1	26	Low	Low	High	High	High	High	High	High
BatchEx	27	C	0	7	0.001	60	1a 1 0		0	LivockLinet1	27	Low	Low	High	High	High	High	High	High

......

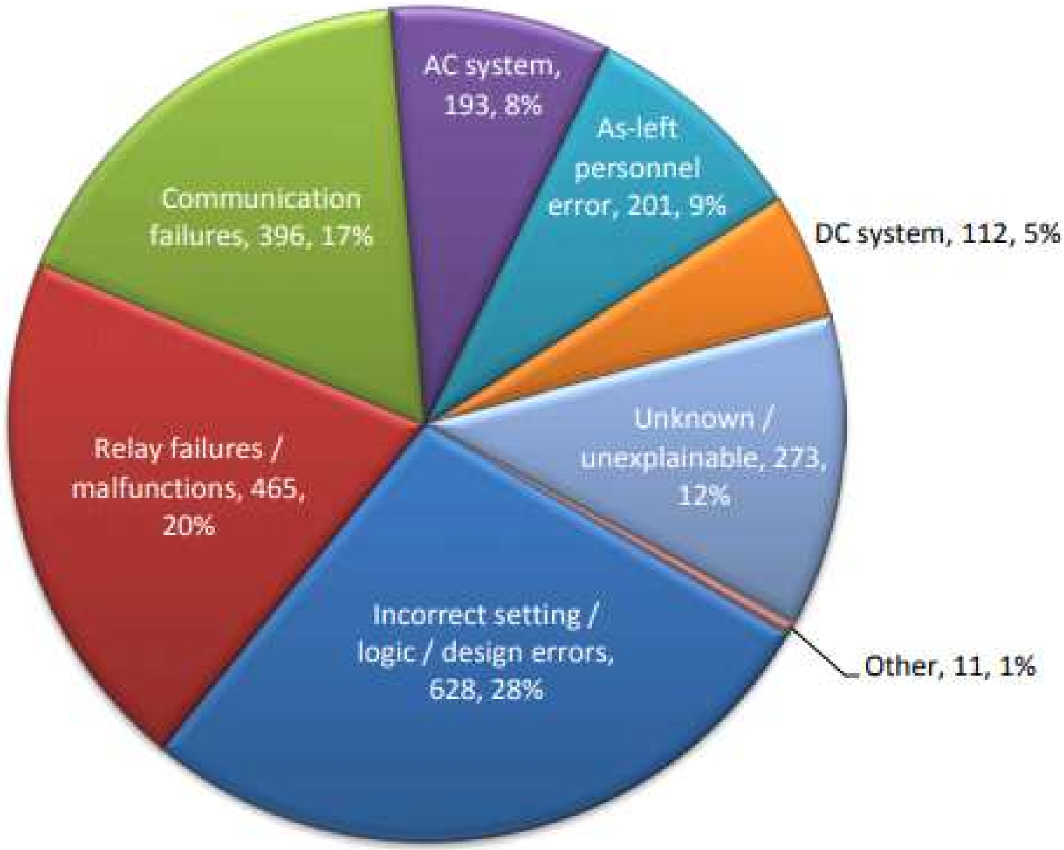
BatchEx	1197	M	100	10	0.001	0	5 1 0		0	LivockLine	1197	Low	Low	High	High	High	High	High	High
BatchEx	1198	M	100	10	0.001	30	5 1 0		0	LivockLine	1198	Low	Low	High	High	High	High	High	High
BatchEx	1199	M	100	10	0.001	60	5 1 0		0	LivockLine	1199	Low	Low	High	High	High	High	High	High
BatchEx	1200	M	100	10	0.001	90	5 1 0		0	LivockLine	1200	Low	Low	High	High	High	High	High	High

Extern Fault 245



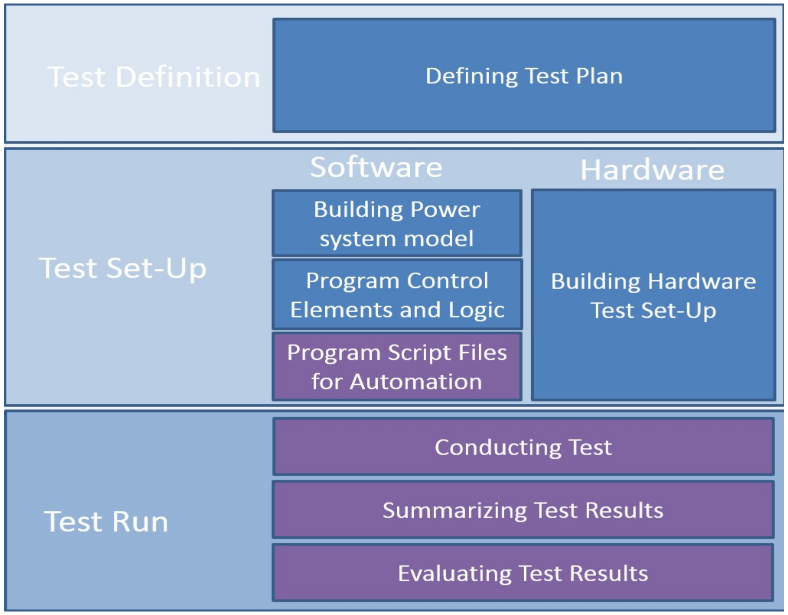
NERC Protection System Misoperations Task Force 2013

Figure 2: NERC-wide Misoperations by Cause Code (Jan 1, 2011 – April 1, 2012)



Advanced Automation & Testing Process

- **Advanced Automation & Testing Process Used by Quanta Technology**
  - Conducting RTDS testing is a budget and resource commitment which should not be underestimated.
  - Quanta Technology utilized a combination of testing automation and process enhancements to reduce the time it takes to conduct RTDS testing, while simultaneously improving the quality of the results.
  - Our goal has been to optimize the process to ensure all necessary tests are conducted as efficiently as possible



Test Plan

Test Plan (tabulated)

Test No.	Fault Position [%]	Fault Location	Type of fault	Rf [ohm]	Angle [Degree]
1001	0.1	F1	AG	0.05	0
1002	0.1	F1	AG	0.05	90
1003	0.1	F1	AB	0.05	150
1004	0.1	F1	AB	0.05	60
1005	0.1	F1	ABG	0.05	0
1006	0.1	F1	ABG	0.05	90
1007	0.1	F1	ABC	0.05	0
1008	0.1	F1	ABCG	0.05	90
1009	30.0	F1	BG	0.05	120
1010	30.0	F1	BG	0.05	30
1011	30.0	F1	BC	0.05	90
1012	30.0	F1	BC	0.05	0

Automation

Script input file

```
001   0.1   F1   1   0.05
002   0.1   F1   1   0.05   90
003   0.1   F1   8   0.05   150
004   0.1   F1   8   0.05   60
005   0.1   F1   4   0.05   0
006   0.1   F1   4   0.05   90
007   0.1   F1   7   0.05   0
008   0.1   F1   7   0.05   90
009   30    F1   2   0.05   120
010   30    F1   2   0.05   30
11    30    F1   9   0.05   90
      30    F1   9   0.05   0
```

Script program file

```
***************************************************/
 Initialization */
/****************************************************/

string fName = "C:\xy_1B.txt";  /* Input File */
fopen(fName,"r");

for ( k=0 ; k<33 ; k++ ) /* Increase K for more test cases,
Maximum is 54  ****/

{
/****** Read from File *****/
     fscanf(fName,"%d",FLTcase);
     fscanf(fName,"%f",FLTpercent);
     fscanf(fName,"%s",FLTLoc);
     fscanf(fName,"%d",FLTtypeNmb);
     fscanf(fName,"%f",FLTresist);
     fscanf(fName,"%f",FLTangle);
SetSlider "Subsystem #2 : CTLs : Inputs : FltDurxxx2"=150; //10
cycles fault duration
SetDial "Subsystem #2 : CTLs : Inputs : LGTYPxxx2" = FLTtypeNmb;
SetSlider "Subsystem #2 : CTLs : Inputs : FltAngxxx2" = FLTangle;
SetSlider "DraftVariables : Lenxx" = FLTpercent;
SetSlider "DraftVariables : RF" = FLTresist;
Start;
SUSPEND 3;
PushButton "Subsystem #2 : CTLs : Inputs : FltActxxx2";
SUSPEND 0.141;
ReleaseButton "Subsystem #2 : CTLs : Inputs : FltActxxx2";
SUSPEND 3;
sprintf(mystring,"C:\x\d_%s",version,FLTcase,version);
ComtradePlotSave "xxx",mystring;
SUSPEND 3.00;
sprintf(mystring,"C:\y\%d_%s",version,FLTcase,version);

ComtradePlotSave "yyy",mystring;
SUSPEND 3.00;

Stop;
}
```

Test Results Summary

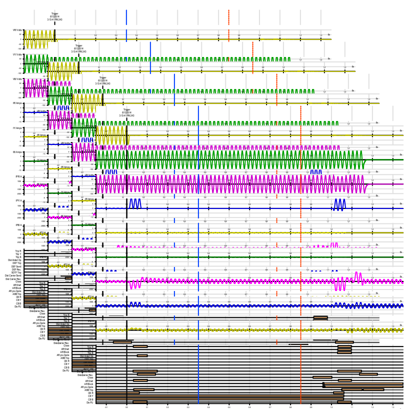
Test No.	Fault Position [%]	Fault Location	Type of fault	Rf [ohm]	Angle [Degree]
1001	0.1	F1	AG	0.05	0
1002	0.1	F1	AG	0.05	90
1003	0.1	F1	AB	0.05	150
1004	0.1	F1	AB	0.05	60
1005	0.1	F1	ABG	0.05	0
1006	0.1	F1	ABG	0.05	90
1007	0.1	F1	ABC	0.05	0
1008	0.1	F1	ABCG	0.05	90
1009	30.0	F1	BG	0.05	120
1010	30.0	F1	BG	0.05	30
1011	30.0	F1	BC	0.05	90
1012	30.0	F1	BC	0.05	0

Automatically Generated Summary of Test Results

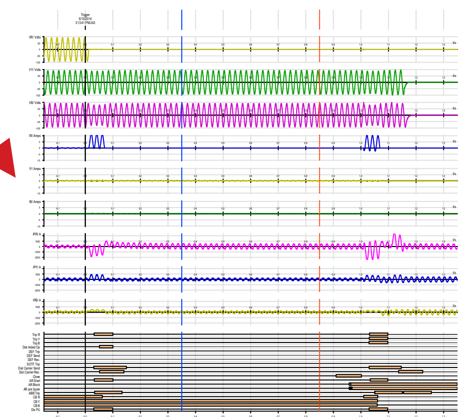
Fault describtion							Raleigh (all times are in ms)				
Test No.	Fault Position [%]	Fault Location	Type of fault	Rf [ohm]	Angle [Degree]		Comtrade File	Trip R	Trip Y	Trip B	Dist Aided Op
1001	0.1	F1	AG	0.05	0		Raleigh_1001_V107	19.2	1017.65	1016.6	38.55
1002	0.1	F1	AG	0.05	90		Raleigh_1002_V107	18.3	1014.8	1013.6	29.55
1003	0.1	F1	AB	0.05	150		Raleigh_1003_V107	18.35	17.7	16.95	27.65
1004	0.1	F1	AB	0.05	60		Raleigh_1004_V107	17.95	17.3	16.3	29.3
1005	0.1	F1	ABG	0.05	0		Raleigh_1005_V107	18.15	17.35	17.25	27.5
1006	0.1	F1	ABG	0.05	90		Raleigh_1006_V107	18.6	17.95	16.9	27.95
1007	0.1	F1	ABC	0.05	0		Raleigh_1007_V107	18.4	17.5	16.6	27.55
1008	0.1	F1	ABCG	0.05	90		Raleigh_1008_V107	18.55	17.8	16.8	27.8
1009	30	F1	BG	0.05	120		Raleigh_1009_V107	1021.25	18.7	1019.6	26.55
1010	30	F1	BG	0.05	30		Raleigh_1010_V107	1045.65	18	1044	28.9
1011	30	F1	BC	0.05	90		Raleigh_1011_V107	20.4	19.6	18.75	29.75
1012	30	F1	BC	0.05	0		Raleigh_1012_V107	20.15	19.5	18.5	26.4
1013	30	F1	BCG	0.05	120		Raleigh_1013_V107	18.6	19.05	17.9	27.9
1014	30	F1	BCG	0.05	30		Raleigh_1014_V107	20.2	19.6	18.65	27.9
1015	30	F1	BCA	0.05	120		Raleigh_1015_V107	20.8	21	20.1	25.05
1016	30	F1	BCAG	0.05	30		Raleigh_1016_V107	20.95	19.95	19.1	28.1
1017	70	F1	CG	0.05	60		Raleigh_1017_V107	1075.2	1074.4	28.35	29.3
1018	70	F1	CG	0.05	150		Raleigh_1018_V107	1037.35	1036.8	23.8	24.7
1019	70	F1	CA	0.05	30		Raleigh_1019_V107	25.8	24.95	25.2	25.1
1020	70	F1	CA	0.05	120		Raleigh_1020_V107	25.7	25.1	24.4	24.05
1021	70	F1	CAG	0.05	60		Raleigh_1021_V107	25.75	25.1	24.1	25.1
1022	70	F1	CAG	0.05	150		Raleigh_1022_V107	29.75	29.2	28.4	29
1023	70	F1	CAB	0.05	60		Raleigh_1023_V107	29.95	29.45	28.3	29.25
1024	70	F1	CABG	0.05	150		Raleigh_1024_V107	26	25.35	24.25	25.3
1025	99	F1	AG	0.05	0		Raleigh_1025_V107	29.4	1104.8	1103.7	28.7
1026	99	F1	AG	0.05	90		Raleigh_1026_V107	25.45	1090.05	1088.8	23.8
1027	99	F1	AB	0.05	150		Raleigh_1027_V107	28.75	27.85	26.85	27.85
1028	99	F1	AB	0.05	60		Raleigh_1028_V107	29.95	29.15	29.2	29.15
1029	99	F1	ABG	0.05	0		Raleigh_1029_V107	25.35	24.6	23.9	23.65
1030	99	F1	ABG	0.05	90		Raleigh_1030_V107	28.15	27.8	26.8	27.8
1031	99	F1	ABC	0.05	0		Raleigh_1031_V107	25.75	24.85	23.9	23.9
1032	99	F1	ABCG	0.05	0		Raleigh_1032_V107	24.55	24.75	23.8	23.65
1033	99	F1	ABCG	0.05	90		Raleigh_1033_V107	25.1	24.55	23.4	23.45

Test No.	DEF Trip	DEF Send	DEF Rec.	SOTF Trip	Dist Carrier Send	Dist Carrier Rec.	Close	AR Start	AR Block	AR pre 3pole	ABB Trip	CB R	CB Y	CB B
1001	-	-	-	-	18.05	38.85	897.1	19.85	944.5	944.85	20.9	49.25	1047.7	1046.65
1002	-	-	-	-	17.1	30	896.05	17.75	944.1	944	25.55	48.35	1044.85	1043.65
1003	-	-	-	-	17.2	26.9	895.65	18.9	942.8	943.6	28.35	48.4	47.75	47
1004	-	-	-	-	16.65	29.65	895.3	18.55	942.6	943.3	21.75	48	47.35	46.35
1005	-	1127.15	-	-	16.95	28	897.3	19.8	942.9	945.2	24.6	48.4	47.4	47.6
1006	-	-	-	-	17.55	28.3	896.8	20.25	944.7	944.95	25.7	48.65	48	46.95
1007	-	-	-	-	17.05	26.05	-	-	51.65	61.7	25.1	48.45	47.55	46.65
1008	-	-	-	-	17.35	28.15	-	-	52.25	61.7	24.05	48.6	47.85	46.85
1009	-	-	-	-	18.05	26.85	897.15	18.8	945.3	944.95	25.85	1051.3	48.75	1049.65
1010	-	-	-	-	17.35	29.4	896.95	20.1	943.35	945.15	24.7	1075.7	48.05	1074.05
1011	-	-	-	-	19.35	30.2	899.25	21.9	944.05	947.25	23.3	50.45	49.65	48.8
1012	-	-	-	-	19.05	26.75	899.55	22.75	949.15	947.65	23.75	50.2	49.55	48.55
1013	-	-	-	-	17.3	28.2	898.05	20.15	943.05	945.5	21.1	48.65	49.1	47.95
1014	-	-	-	-	19.15	27.15	901.35	22.95	946.9	948.65	21.45	50.25	49.65	48.7
1015	-	-	-	-	19.45	25.45	-	-	55.1	64.75	21.6	50.85	51.05	50.15
1016	-	-	-	-	19.65	27.55	-	-	55	65.05	23.35	51	50	49.15
1017	-	-	-	-	24.75	27.5	908	29.65	955.55	955.65	25.45	1105.25	1104.45	58.4
1018	-	-	-	-	24.15	22	903.35	26	949	952.4	25.6	1067.4	1066.85	53.85
1019	-	-	-	-	24.65	23.2	903.4	26.5	947.7	951.1	25.7	55.85	55	55.25
1020	-	-	-	-	23.55	22.3	902.6	25.4	950.25	950.1	22.4	55.75	55.15	54.45
1021	-	-	-	-	23.4	25.3	902.35	25.5	950.8	951.2	25.1	55.8	55.15	54.15
1022	-	-	-	-	23.6	28.35	907.3	29.25	951.6	954.65	21.7	59.8	59.25	58.45
1023	-	-	-	-	23.65	29.55	-	-	61.55	70.85	21.75	60.2	59.5	58.35
1024	-	-	-	-	23.8	25.55	-	-	57.5	67.05	23.45	56.05	55.4	54.3
1025	-	-	-	-	24.1	28.2	906.9	28.95	953.1	955.6	21.1	59.45	1134.85	1133.75
1026	-	-	-	-	23.25	23.95	903.25	25.05	947.75	951.1	23.65	55.5	1120.1	1118.85
1027	-	-	-	-	27.3	27.05	906.35	29.15	953.55	953.85	27.35	58.8	57.9	56.9
1028	-	-	-	-	23.6	29.5	907.3	30.5	952.25	955	25.45	60	59.2	59.25
1029	-	1136.2	-	-	23.2	20.85	902.85	24.95	949.35	950.3	22.65	55.4	54.65	53.95
1030	-	1137.5	-	-	23.25	26.1	905.9	28.05	953.3	953.4	25.55	58.2	57.85	56.85
1031	-	-	-	-	23.4	21.15	-	-	56.6	67.05	19.5	55.8	54.9	53.95
1032	-	-	-	-	23.35	21	-	-	55.8	65.95	21.85	54.6	54.8	53.85
1033	-	-	-	-	22.9	22.7	-	-	56.55	65.85	22.2	55.15	54.6	53.45

Standard RTDS output -> n-COMTRADE files

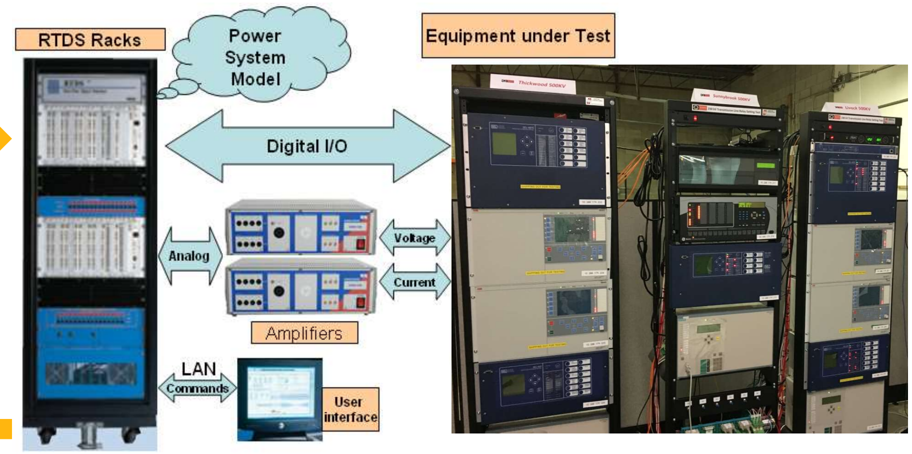


Hyperlink functionality for detailed review



Process Automation

Test Case #	Fault Location	Percent	Fault Type	Fault Duration [cycle]	Fault Angle	Fault Resistor	Load
L44_1201	A	0.00	AG	12	0	5	Case #1a
L44_1202	A	0.00	BG	12	30	5	Case #1b
L44_1203	A	0.00	CG	12	60	5	Case #2a
L44_1204	A	0.00	CG	12	90	5	Case #2b
L44_1205	A	0.00	AG	12	0	5	Case #3
L44_1206	A	0.00	ABG	12	30	5	Case #1a
L44_1207	A	0.00	BC	12	60	5	Case #1b
L44_1208	A	0.00	ABC	12	90	5	Case #2a
L44_1209	A	0.00	CA	12	0	5	Case #2b
L44_1210	A	0.00	CAG	12	30	5	Case #3

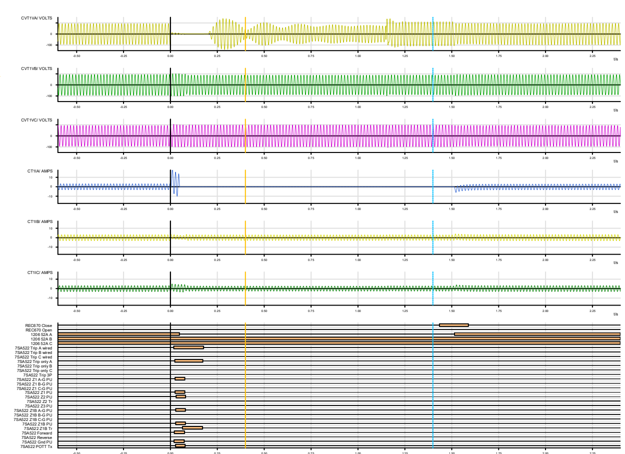


t Description

Test Case #	Fault Location	Percent	Fault Type	Fault Duration [cycle]	Fault Angle	Fault Resistor	Load	Fast Comm Block	Slow Comm Block	
L44_1201	A	0.001	AG	12	0	5	Case #1a	1	0	ThickLine_1201
L44_1202	A	0.001	BG	12	30	5	Case #1b	1	0	ThickLine_1202
L44_1203	A	0.001	CG	12	60	5	Case #2a	1	0	ThickLine_1203
L44_1204	A	0.001	CG	12	90	5	Case #2b	1	0	ThickLine_1204
L44_1205	A	0.001	AG	12	0	5	Case #3	1	0	ThickLine_1205
L44_1206	A	0.001	ABG	12	30	5	Case #1a	1	0	ThickLine_1206
L44_1207	A	0.001	BC	12	60	5	Case #1b	1	0	ThickLine_1207
L44_1208	A	0.001	ABC	12	90	5	Case #2a	1	0	ThickLine_1208
L44_1209	A	0.001	CA	12	0	5	Case #2b	1	0	ThickLine_1209
L44_1210	A	0.001	CAG	12	30	5	Case #3	1	0	ThickLine_1210

Thickwood Line Protection

	REC670 Close	REC670 Open	1206 52A A	1206 52A B	1206 52A C	7SA522 Trip A wired	7SA522 Trip B wired	7SA522 Trip C wired	7SA522 Trip only A	7SA522 Trip only B	7SA522 Trip only C	7SA522 Trip 3P	7SA522 Z1 A-G PU	7SA522 Z1 B-G PU	7SA522 Z1 C-G PU	7SA522 Z1 PU	7SA522 Z2 PU	7SA522 Z2 Tr	7SA522 Z3 PU	7SA522 Z1B A-G PU	7SA522 Z1B B-G PU	7SA522 Z1B C-G PU	7SA522 Z1B PU	7SA522 Z1B Tr
ThickLine_1201	1432	Low	45.6	High	High	15.2	Low	Low	20.8	Low	Low	Low	22.4	Low	Low	22.4	28	Low	Low	25.6	Low	Low	25.6	61.6
ThickLine_1202	1426.4	Low	High	46.4	High	Low	12.8	Low	Low	19.2	Low	Low	Low	20.8	Low	20.8	25.6	Low	Low	Low	24	Low	24	59.2
ThickLine_1203	1428.8	Low	High	High	44.8	Low	Low	14.4	Low	Low	20	Low	Low	Low	21.6	21.6	28	Low	Low	Low	Low	25.6	25.6	64
ThickLine_1204	1420	Low	High	High	44	Low	Low	12.8	Low	Low	18.4	Low	Low	Low	20.8	20.8	26.4	Low	Low	Low	Low	24.8	24.8	57.6
ThickLine_1205	1420.8	Low	44	High	High	14.4	Low	Low	20	Low	Low	Low	21.6	Low	Low	21.6	28.8	Low	Low	25.6	Low	Low	25.6	48
ThickLine_1206	Low	Low	47.2	47.2	47.2	13.6	13.6	13.6	Low	Low	Low	19.2	Low	21.6	Low	21.6	28.8	Low	Low	Low	27.2	Low	27.2	41.6
ThickLine_1207	Low	Low	46.4	46.4	46.4	12.8	12.8	12.8	Low	Low	Low	16.8	Low	Low	Low	18.4	25.6	Low	Low	Low	Low	Low	23.2	47.2
ThickLine_1208	Low	Low	44	44	44	12.8	12.8	12.8	Low	Low	Low	17.6	Low	Low	Low	20	26.4	Low	Low	Low	Low	Low	24.8	40.8
ThickLine_1209	Low	Low	46.4	47.2	47.2	12.8	13.6	13.6	Low	Low	Low	17.6	Low	Low	Low	20	25.6	Low	Low	Low	Low	Low	24.8	43.2
ThickLine_1210	Low	Low	44	44	44	13.6	13.6	13.6	Low	Low	Low	20	21.6	Low	Low	21.6	27.2	Low	Low	25.6	Low	Low	25.6	41.6



Conclusion

- To select appropriate number of test cases is a difficult task
- Time and budget constrains often dictate number of test cases
- Automation enables more effective testing

Thank you!

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