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Practical Application of Co-Simulation Studies

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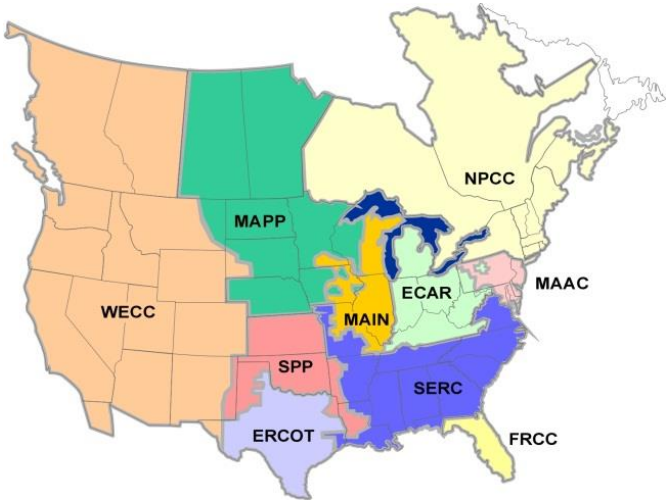
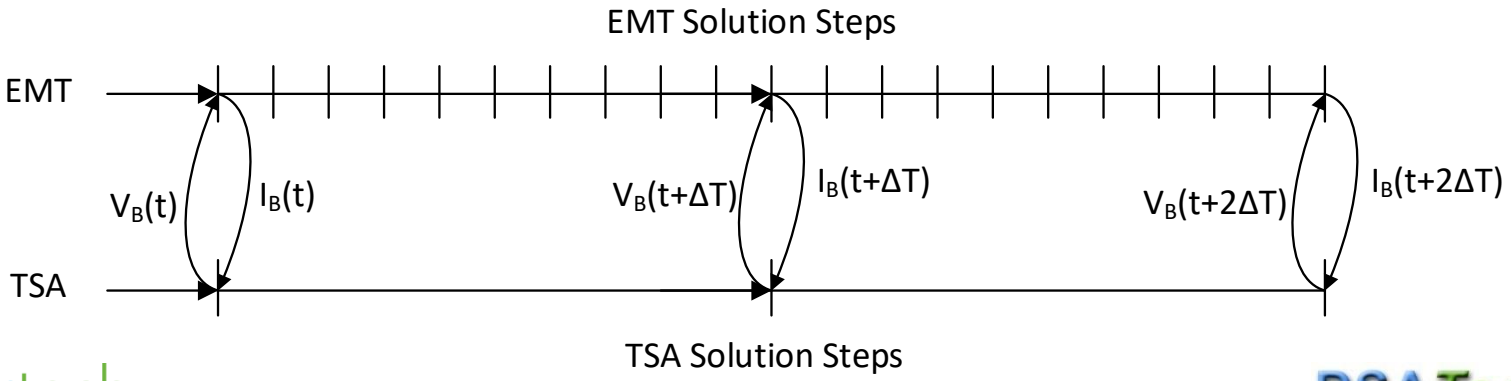
Background

- EMT Simulation Software
  - Three-phase, detailed component model
  - Typically a small region of the system is modelled
- TSA Simulation Software
  - Phasor-Domain, positive sequence models
  - Simulates tens of thousands of buses
  - Planning and operation of bulk power system
- Challenge
  - Gap between application of EMT and TSA
  - How to represent the large external system in EMT simulation?



Background

- Co-Simulation Studies
  - Platform for synchronized simulation using EMT and TSA
  - System partitioned into two or multiple regions, each region simulated by EMT or TSA
  - EMT and TSA run in parallel
  - Injections (responses from the other region) are exchanged at the end of each TSA time-step (typically a few milliseconds)



Background

- Sample Applications of Co-Simulation Studies
  - Hardware-In-Loop (HIL) testing with much larger portion of the system
    - E.g. Testing out-of-step relays, wide area control scheme
  - Impact of low-frequency oscillations on specific devices and vice-versa
    - E.g. HVDC and FACTS devices
  - Access to modeling library of both EMT and TSA simulation packages
    - E.g. Many detailed renewable models available only in EMT packages
  - EMT studies with various system operating conditions
    - It is relatively easier to maintain large number of system snapshots in TSA

TSAT-RTDS Interface (TRI)

- A tool for performing hybrid simulation studies
  - Small region of system modeled in RTDS, rest of system modeled in TSAT
  - Jointly developed by Powertech, KEPCO and Yonsei University
- TRI is developed with special focus on **practical aspects** to
  - Make the tool user-friendly
  - Minimize co-simulation case setup efforts
  - Simplify results analysis steps

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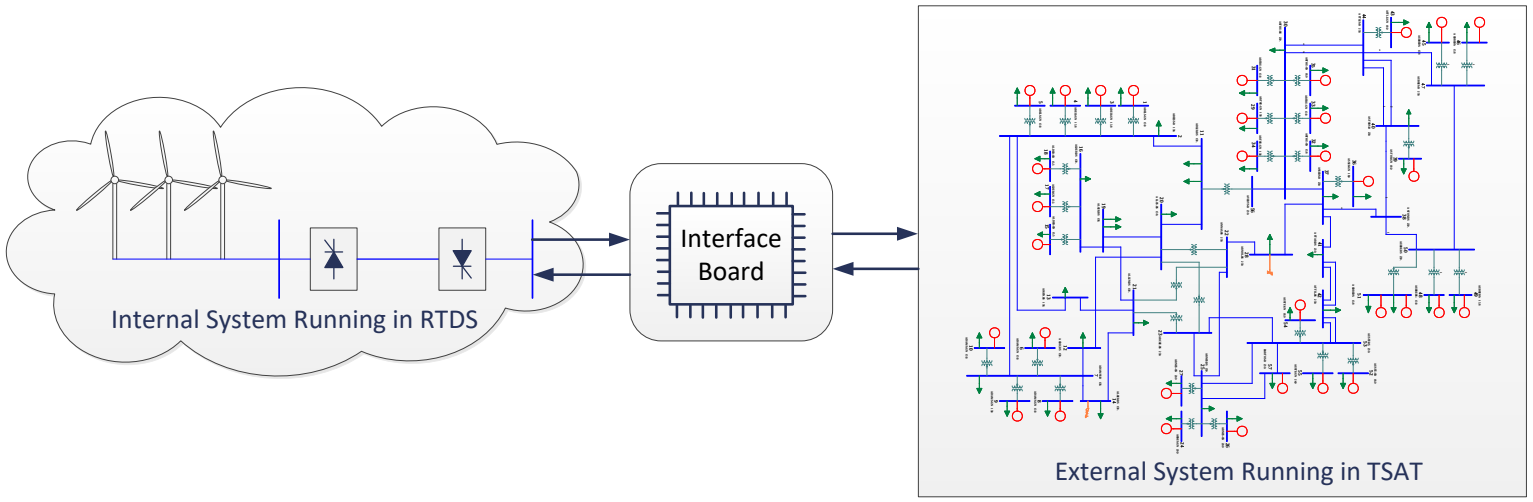
KEPCO

YONSEI UNIVERSITY

DSATools™
Dynamic Security Assessment Software

TSAT-RTDS Interface (TRI)

- System separated into multiple regions
  - Each region is modeled in either TSAT or RTDS
- Synchronized, and real-time simulation
  - 1-second of simulation takes 1 second in both TSAT and RTDS
- Injections exchanged through a FPGA board



Co-Simulation in Practical System

- Powertech has worked with New York Power Authority (NYPA)
- TRI is used in NYPA's AGILe lab
- Co-Simulation cases have been developed
- High-level summary of Co-Simulation case setup is discussed

Co-Simulation Case Setup

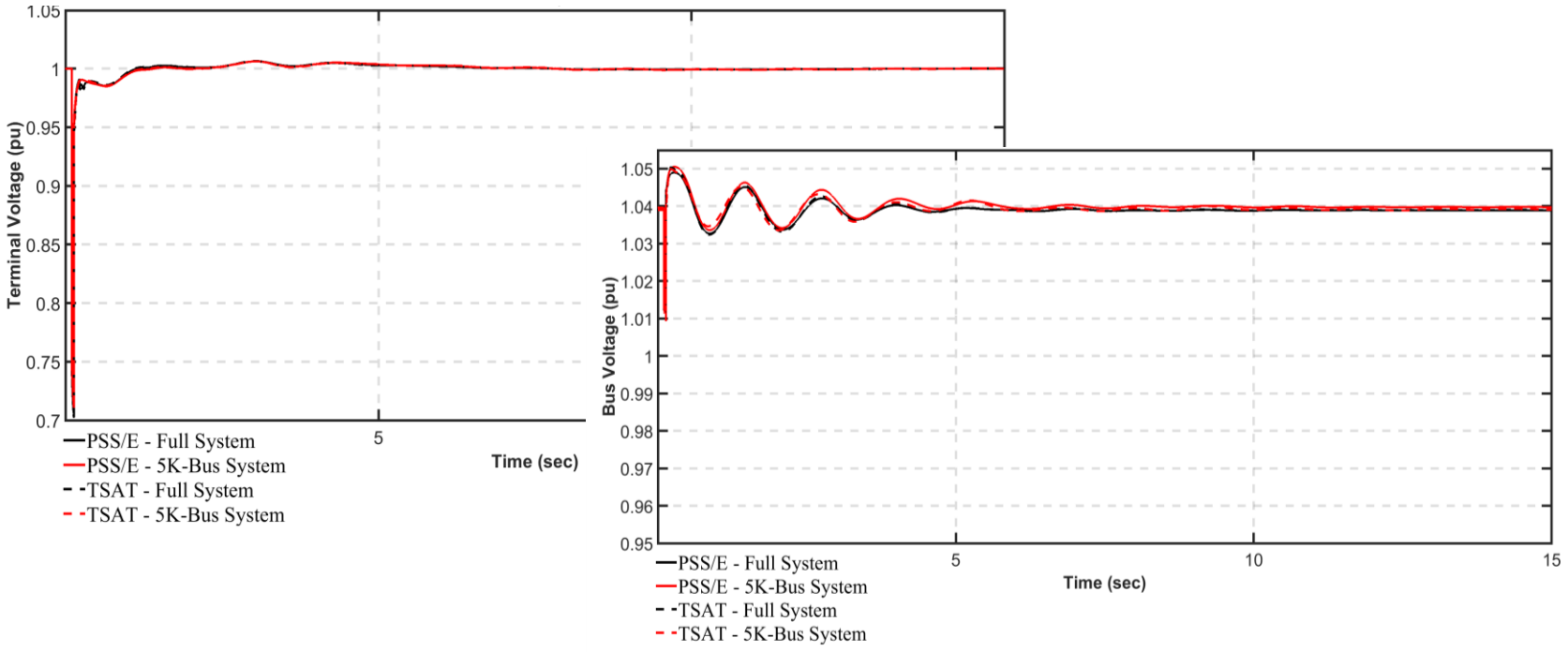
- Hard real-time simulation requirement limits the size of the system model
  - RTDS can normally handle a model with hundreds of buses, depending on hardware size
  - TSAT can simulate a system with ~10,000 buses, with decent hardware (e.g. a PC with Intel® Core™ i7-8700K Processor)
- Eastern Interconnection system planning case has over 80,000 buses
  - Such large system cannot be simulated in real-time using TSAT
- Dynamic reduction was required when preparing the co-simulation cases for NYPA

Co-Simulation Case Setup – Dynamic Reduction

- Objectives
  - Reduce the East Interconnection planning case to less than 10,000 buses
  - Retaining low-frequency oscillation characteristics of the external system
- Approach
  - NYISO system reduction
    - Retain all high voltage network (230kV and up) and most of 138kV network
  - External system reduction
    - Identify low-frequency modes with large participation from NYISO generators
    - Aggregate coherent generator groups using DYNRED software

Co-Simulation Case Setup – Dynamic Reduction

- End results
  - A reduced system with ~5,500 buses was created
- Selected contingencies used for benchmarking

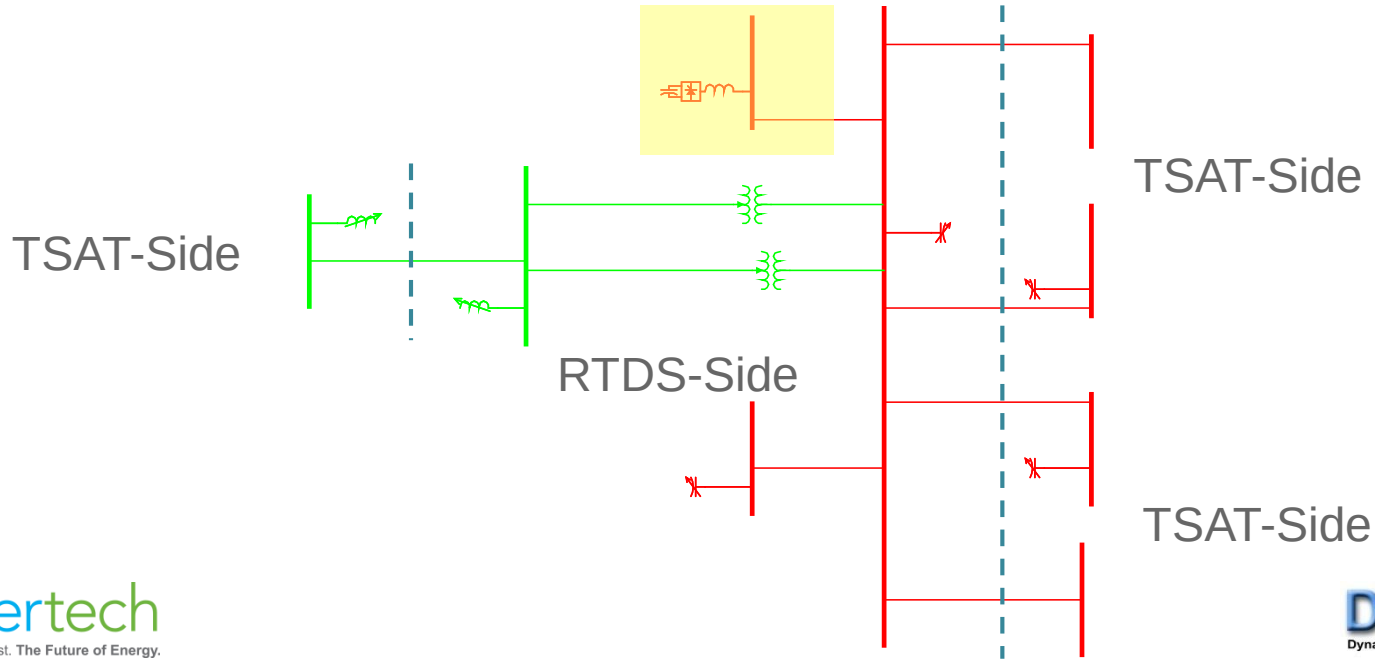


Co-Simulation Case Setup –Boundary Identification

- Next step: Identify the boundaries between RTDS and TSAT
- Multiple co-simulation cases were setup
  - Model a power plant in RTDS (10 boundary ports between RTDS and TSAT)
  - STATCOM case study (2/6 ports)
  - Model a large region of New York state grid in RTDS (6 ports)
- The STATCOM case is discussed here

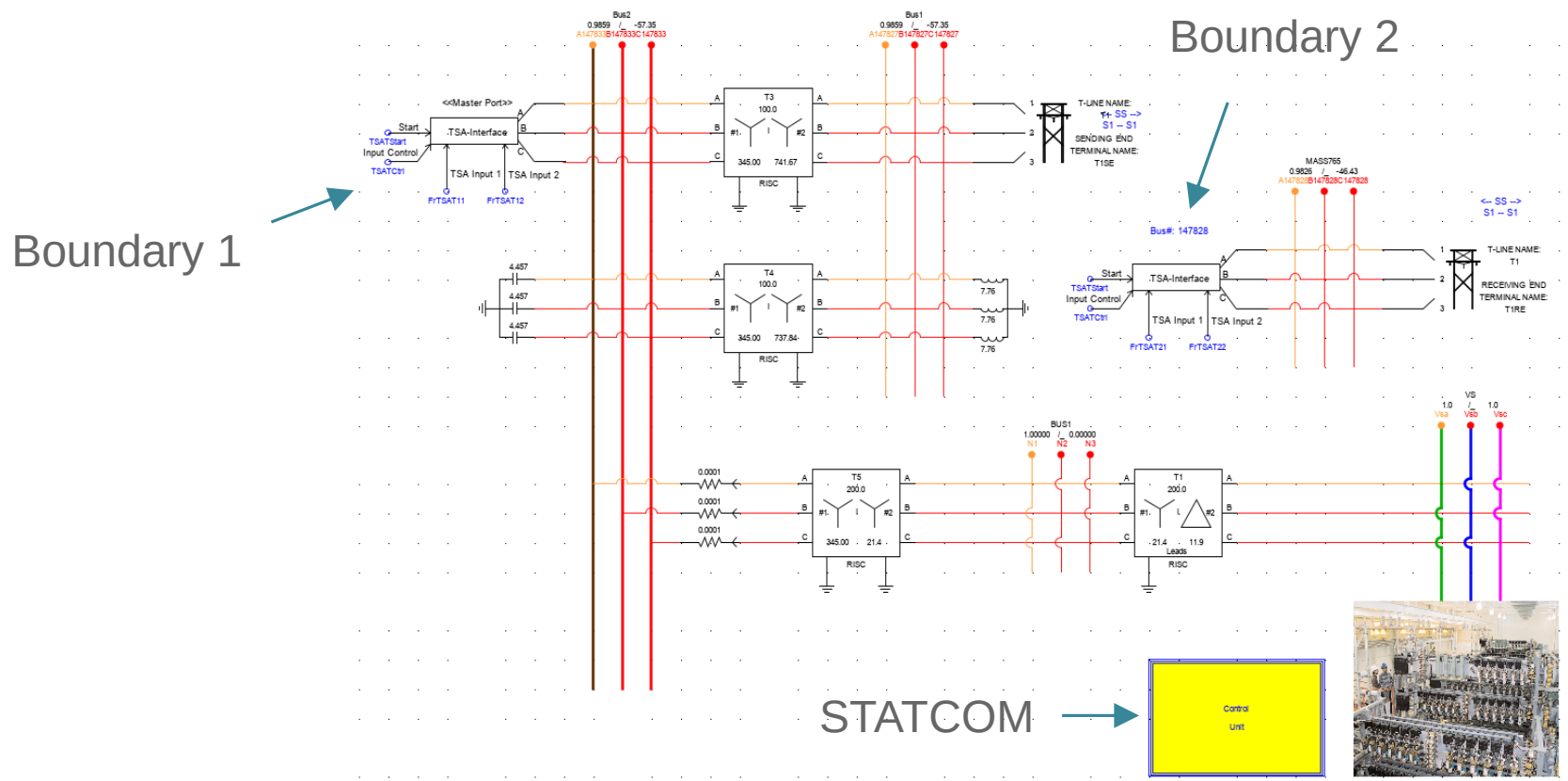
Co-Simulation Case Setup

- A STATCOM in highly meshed region modeled in RTDS
- Rest of system simulated in TSAT
- STATCOM model tested in a small RTDS region first, then tested in a large RTDS region (co-simulation case #3)



Co-Simulation Case Setup

- RTDS case created next



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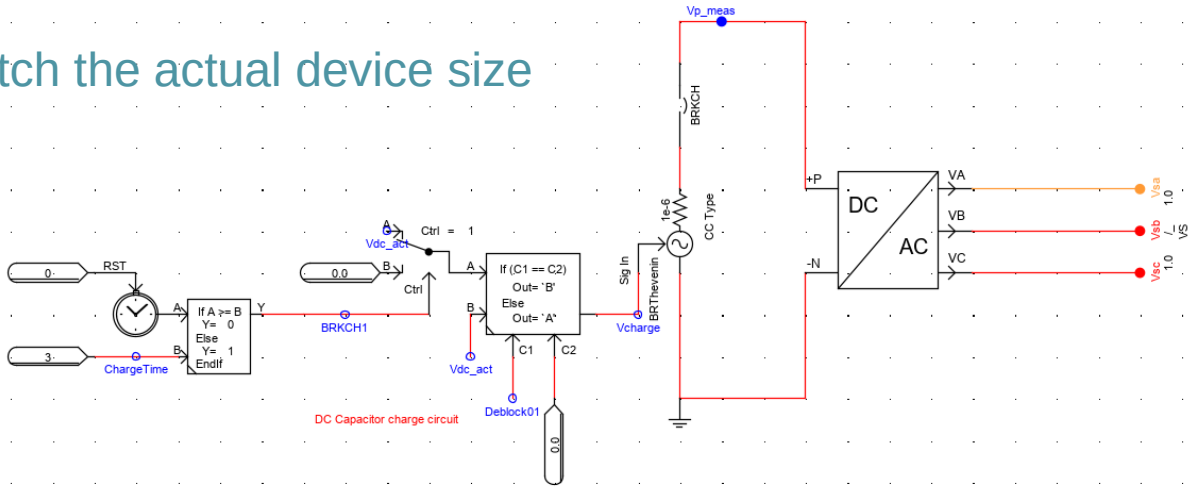
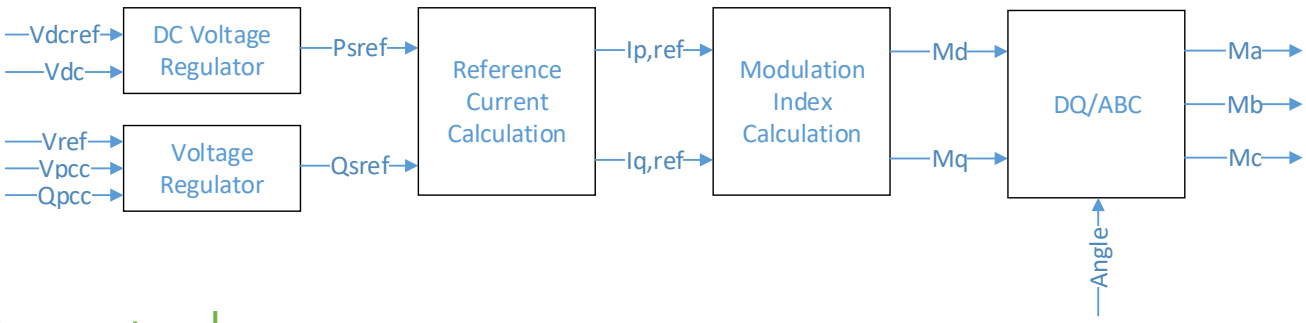
Co-Simulation Case Setup

- STATCOM represented by an Average Value Model (AVM)
  - Modeled provided by RTDS Technologies to NYPA
  - Scaled up to match the actual device size

Power System





Control Structure

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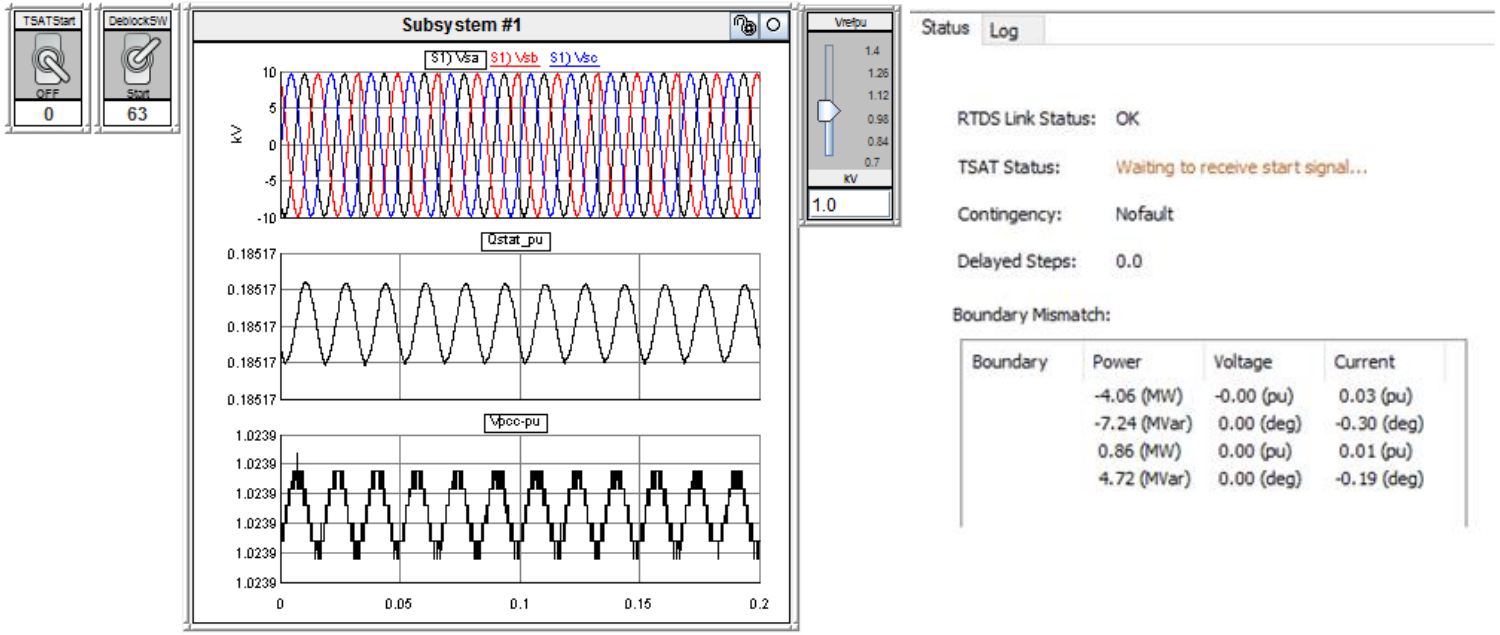
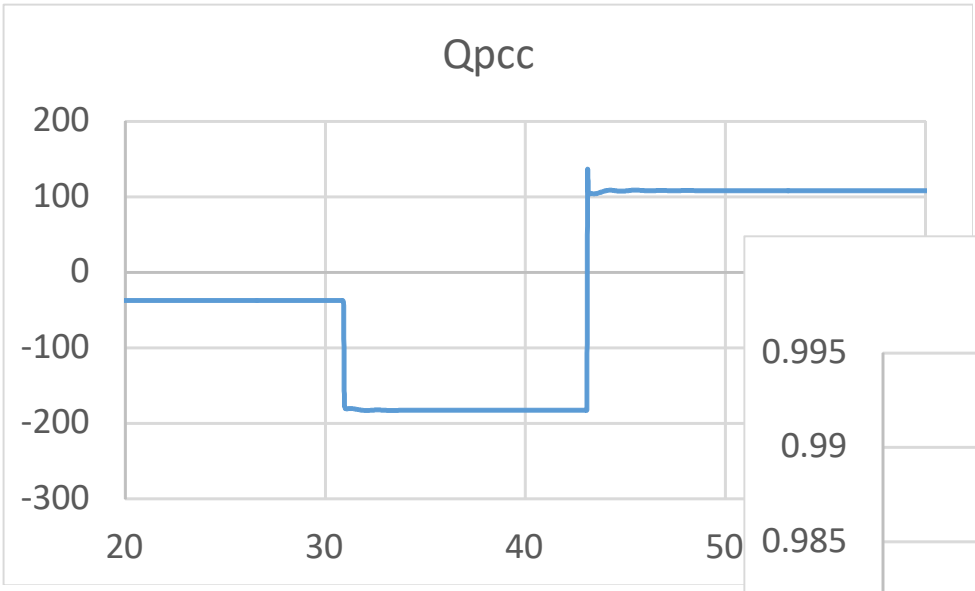
Simulation Results – Verifying RTDS Model

- RTDS case started
- TSAT initialized from powerflow condition, running in Standby mode
- Mismatch between RTDS model and powerflow solution monitored
- Start TSAT simulation once the mismatch is small enough

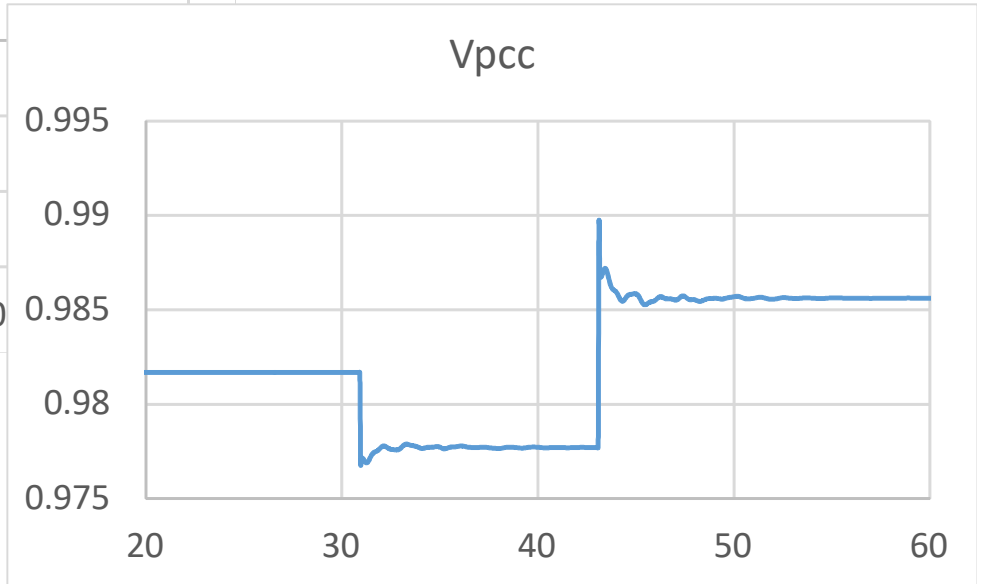


Simulation Results – Verifying RTDS Model

- Test 1 – STATCOM Step Response



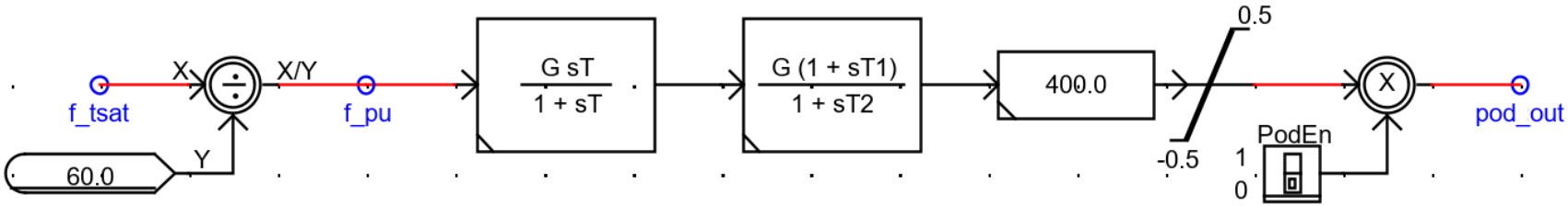
STATCOM Reactive Power (High-Voltage Side)



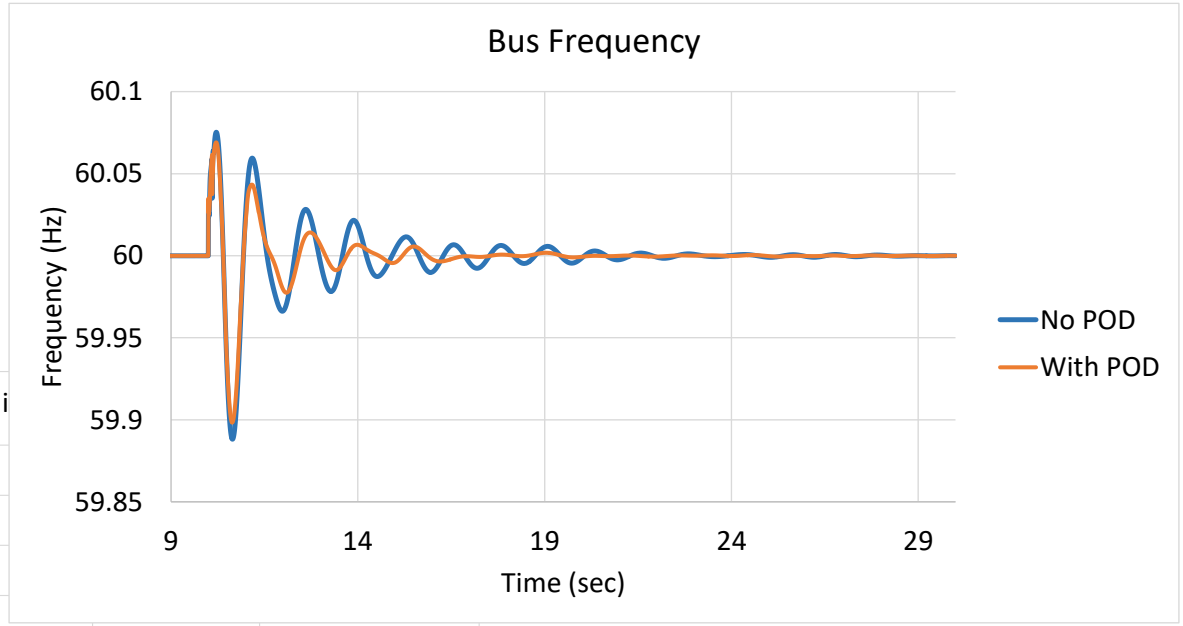
Boundary Bus Voltage (TSAT-Side)

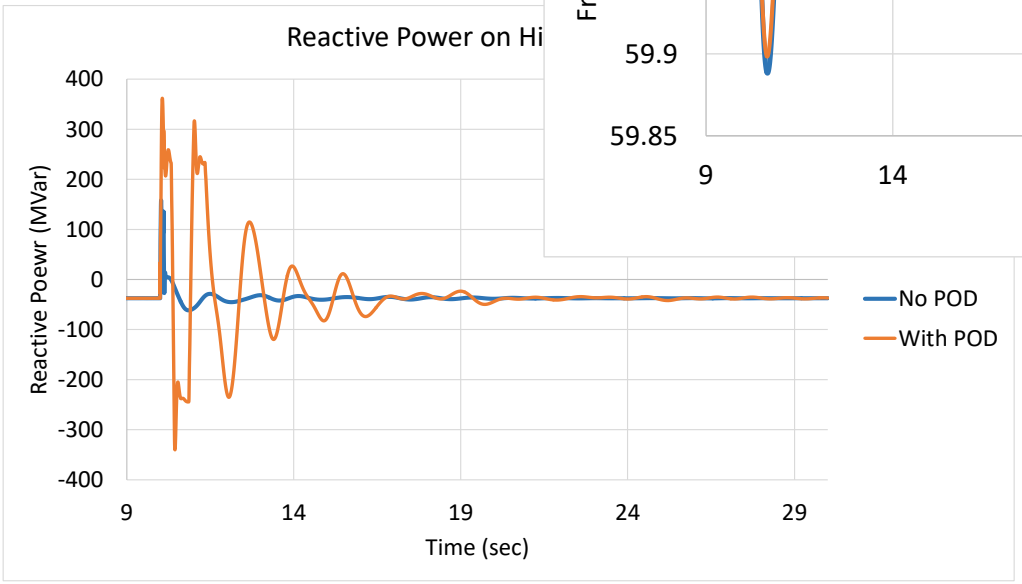
Simulation Results – Adding POD

- Test 2 – Power Oscillation Damper
  - A POD added to the STATCOM controller
  - POD input: frequency measurement of one of buses in the TSAT region
    - Sent to RTDS via available channels on the FPGA card
  - Focus on proving concept instead of tuning POD parameters
    - Better results can be achieved by a full parameter tuning process



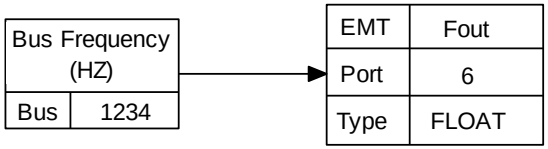
Simulation Results - Adding POD



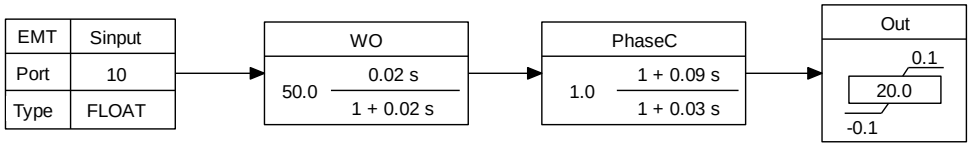


Exchanging Control Signals between RTDS and TSAT

- TSAT sends signals to RTDS



- RTDS sends signals to TSAT



- Similar concept may be used for simulation of other schemes
  - E.g. wide-area protection/control, PMU applications

_rtds_GTFPGA.def

CONFIGURATION | To GTFPGA | From GTFPGA

Name	Description	Value
numVarsFromGTFPGA	Number of Variables recieved from GTFPGA	6
in1	Name of input word #1 from GTFPGA	TSATCtrl
SetTypeFrGTFPGA1	Select Data format from GTFPGA	Int
in2	Name of input word #2 from GTFPGA	FrTSAT11
SetTypeFrGTFPGA2	Select Data format from GTFPGA	Float
in3	Name of input word #3 from GTFPGA	FrTSAT12
SetTypeFrGTFPGA3	Select Data format from GTFPGA	Float
in4	Name of input word #4 from GTFPGA	FrTSAT21
SetTypeFrGTFPGA4	Select Data format from GTFPGA	Float
in5	Name of input word #5 from GTFPGA	FrTSAT22
SetTypeFrGTFPGA5	Select Data format from GTFPGA	Float
in6	Name of input word #6 from GTFPGA	f_tsat
SetTypeFrGTFPGA6	Select Data format from GTFPGA	Float

_rtds_GTFPGA.def

CONFIGURATION | To GTFPGA | From GTFPGA

Name	Description	Value
numVarsToGTFPGA	Number of Variables sent from RTDS to GTFPGA	12
out1	Name of output word #1 to GTFPGA	RTDSCtrl
SetTypeToGTFPGA1	Select Data format to GTFPGA	Int
out2	Name of output word #2 to GTFPGA	ToTSAT11
SetTypeToGTFPGA2	Select Data format to GTFPGA	Float
out3	Name of output word #3 to GTFPGA	ToTSAT12
SetTypeToGTFPGA3	Select Data format to GTFPGA	Float
out4	Name of output word #4 to GTFPGA	ToTSAT21
SetTypeToGTFPGA4	Select Data format to GTFPGA	Float
out5	Name of output word #5 to GTFPGA	ToTSAT22
SetTypeToGTFPGA5	Select Data format to GTFPGA	Float
out6	Name of output word #6 to GTFPGA	ToTSAT31
SetTypeToGTFPGA6	Select Data format to GTFPGA	Float
out7	Name of output word #7 to GTFPGA	ToTSAT32
SetTypeToGTFPGA7	Select Data format to GTFPGA	Float
out8	Name of output word #8 to GTFPGA	ToTSAT41
SetTypeToGTFPGA8	Select Data format to GTFPGA	Float
out9	Name of output word #9 to GTFPGA	ToTSAT42
SetTypeToGTFPGA9	Select Data format to GTFPGA	Float
out10	Name of output word #10 to GTFPGA	fgen1
SetTypeToGTFPGA10	Select Data format to GTFPGA	Float
out11	Name of output word #11 to GTFPGA	fgen2
SetTypeToGTFPGA11	Select Data format to GTFPGA	Float
out12	Name of output word #12 to GTFPGA	fgen3
SetTypeToGTFPGA12	Select Data format to GTFPGA	Float

Conclusion and Future Plan

- Real-time Co-Simulation performed using industry leading EMT and TSA packages
- Co-simulation case setup process simplified
- Utilize the strengths of both RTDS and TSAT

- Next steps
  - Use same concept to break TSAT region into multiple sub-systems. Allow TSAT to simulate super-large system (e.g. the East Interconnection system) in real-time.
  - Further simplify the case setup process