High-bandwidth, low-latency fibre-optic RTDS interface platform for modular, high-power amplifiers

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Introduction

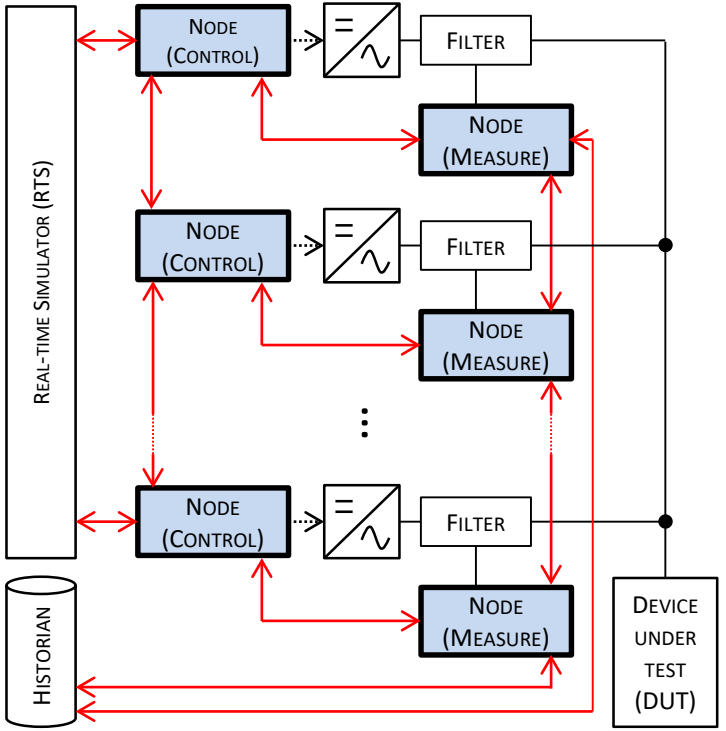
- Power hardware-in-the-loop (PHIL)
- Fibre-optic RTDS interface platform
- Resampled pulse width modulation (PWM)
- Balancing in paralleled interleaved converters
- Conclusions

Power hardware-in-the-loop (PHIL)

- Methodology for characterisation or validation of real power hardware tested against a simulated system
  - Attractive where construction of a physical analogue is infeasible
- Design of the interfacing system (power amplifier) is challenging as the required power-bandwidth increases
  - Move to amplifier comprising multiple, sub-rated converter modules
- As scale of the system increases, performance of the control and data acquisition system becomes a limiting factor

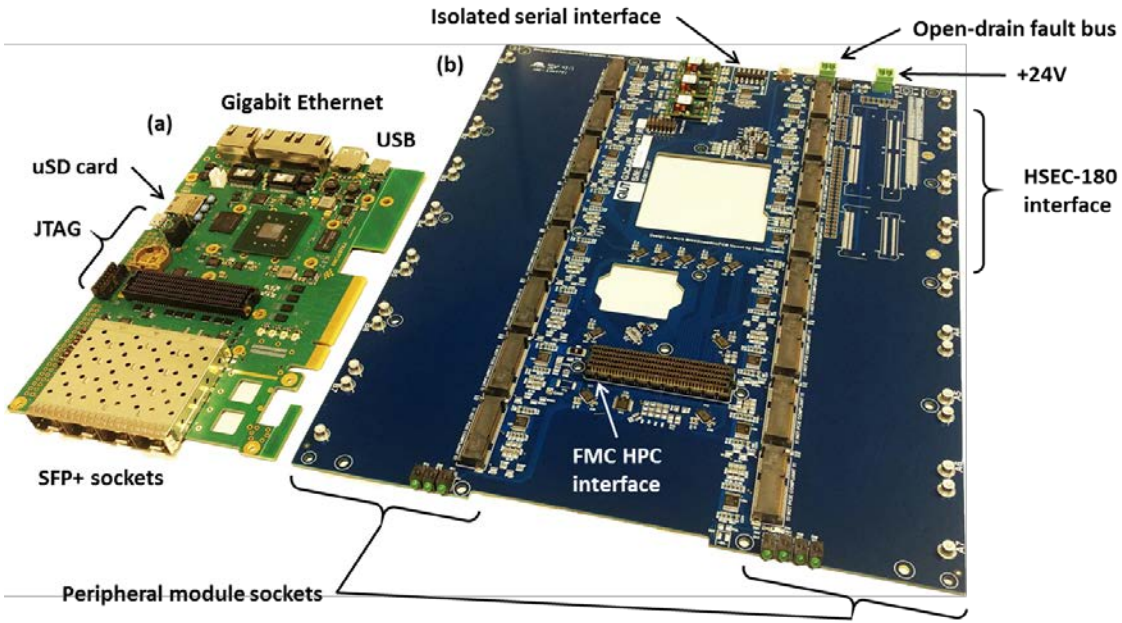
Control and data acquisition topology for high-power, high-bandwidth amplifiers

- Computational nodes connected via full-duplex, multi-gigabit fibre optic links
  - Four transceivers per node permit, ring, star and hybrid topologies
- Nodes may be configured for control and/or measurement functions
  - Peripheral modules define application-specific inputs and outputs (e.g. voltages, currents)
- Real time simulator also interfaced digitally via fibre optic links
  - Measurement samples and control references



FIBRE-OPTIC RTDS INTERFACE PLATFORM

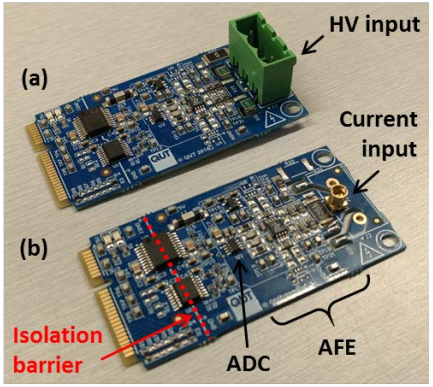
Base board and controller

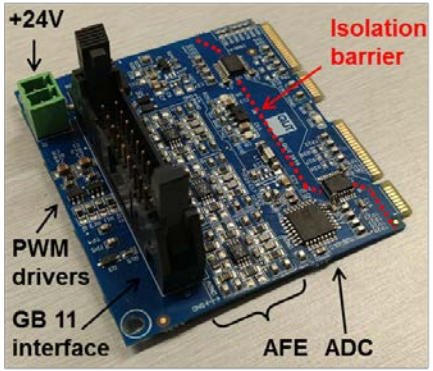


- FPGA System-on-Chip
  - Programmable logic + dual-core ARM
- 4x SFP+ ports (up to 6.6 Gbps)
- Memory, USB, micro SD, Ethernet etc.
- FMC interface to base board
- 16x peripheral module sockets
  - 4 dedicated GPIO, 2 shared GPIO
  - Common I^2C bus
  - 7-bit detect and ID interface
- 44 I/O parallel interface
  - Compatible with HSEC180 TI ControlCARD boards
- 6U Eurocard form factor

Peripheral modules (1st generation)

- G3ADC – Single channel ADC, 1MSPS 12-bit
  - HV input, ± 1000V
  - LV input, ± 10V
  - Current input ± 400mA, to suit LEM closed loop hall-effect sensors
  - Provision for 2nd order multiple feedback lowpass filter (antialiasing)
  - 2.5 kV isolation
- G3DAC – 4 channel DAC, 250 kHz update rate, ~20 kHz bandwidth
- G3GDI – Half-bridge SEMIKUBE gate driver interface
  - 2x 24 V PWM signals
  - Open drain 24 V bidirectional fault bus
  - ADC of three ±10 V signals (typically bus voltage, phase current and temperature); 500 kSPS when uniformly sampled
  - Power via 24 V Eurostyle header

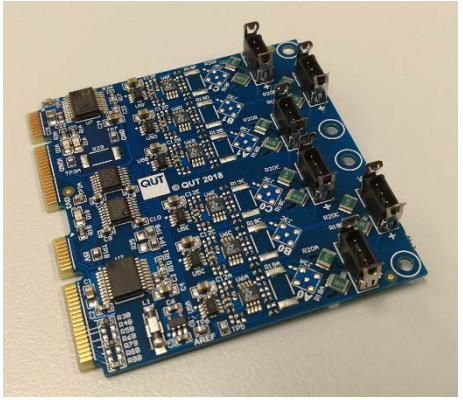


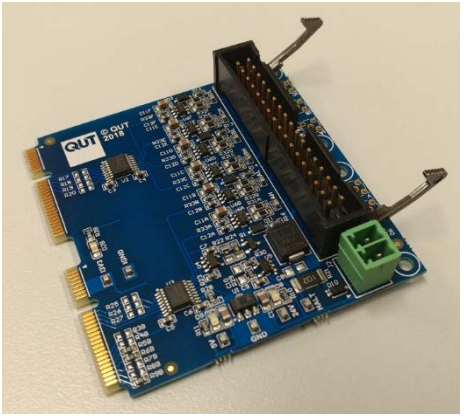


Peripheral modules (2nd generation)

- G3HADC – Hex ADC module
  - 6x simultaneous sampled fully differential inputs
  - 1 MSPS, 12-bit
  - HV, LV and current input variants

- G3TGDI – Three-phase gate drive interface
  - To suit three-phase SEMIKUBE stacks (GD11)
  - 6x 24 V PWM signals, open drain fault bus
  - Analogue signals broken out to MMCX



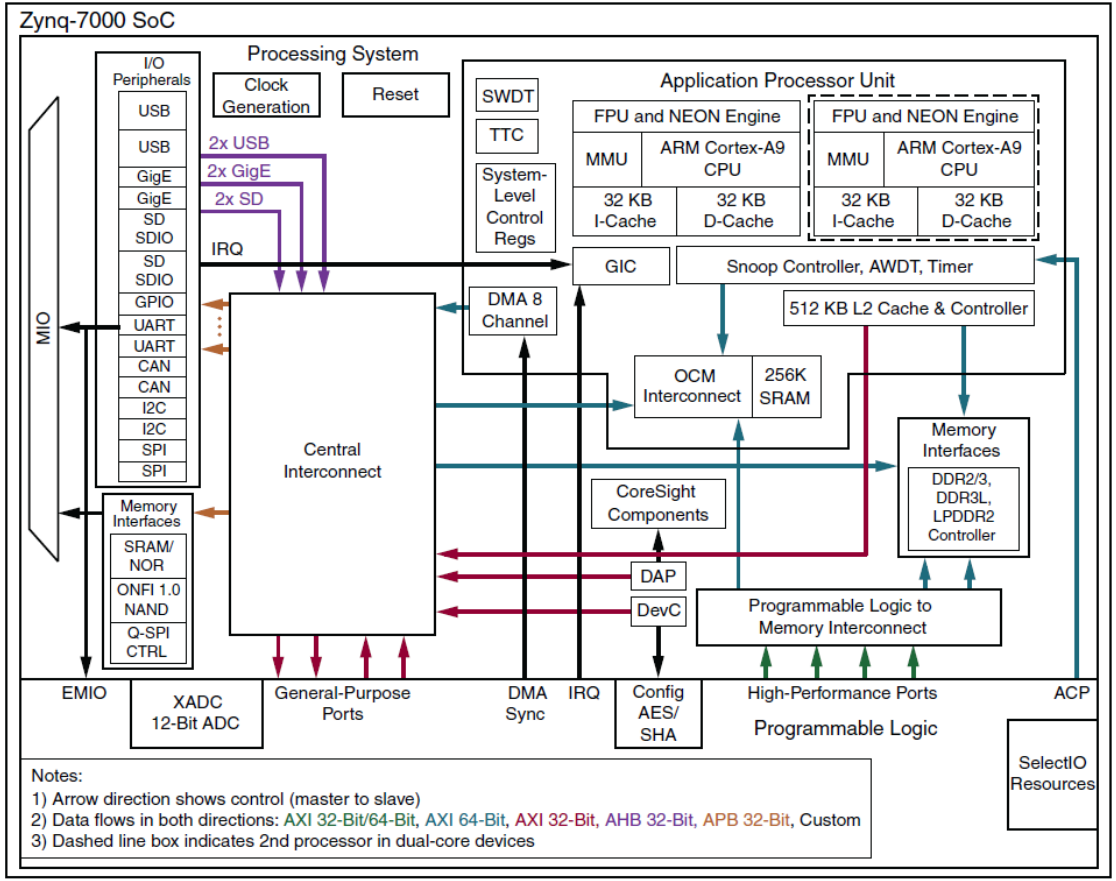


Programmable Logic (PL)

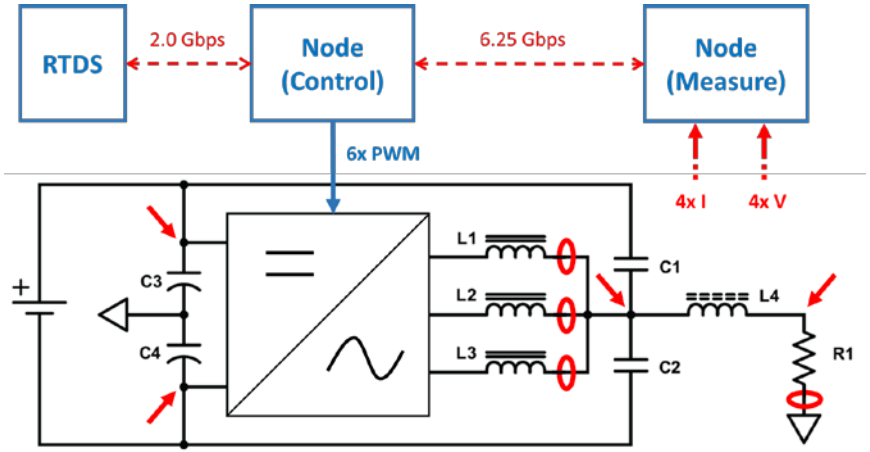
- 200 MHz system clock (5 ns resolution)
- Sampling of ADCs at 1 MHz
- MAF with arbitrary window lengths
- Aurora high-speed serial links
  - 2.0 Gbps to RTDS
  - 6.25 Gbps between nodes
- DMA of sampled values into PS OCM @ 1 MHz
- PACPWM modules

Processor System (PS)

- CPUs @ 667 MHz
- 1 GB DDR3L SDRAM
- Linux OS on CPU0
  - Configuration, supervision, debugging etc.
- Baremetal app on CPU1
  - Real-time control applications
  - Expected control rates up to 1 MHz

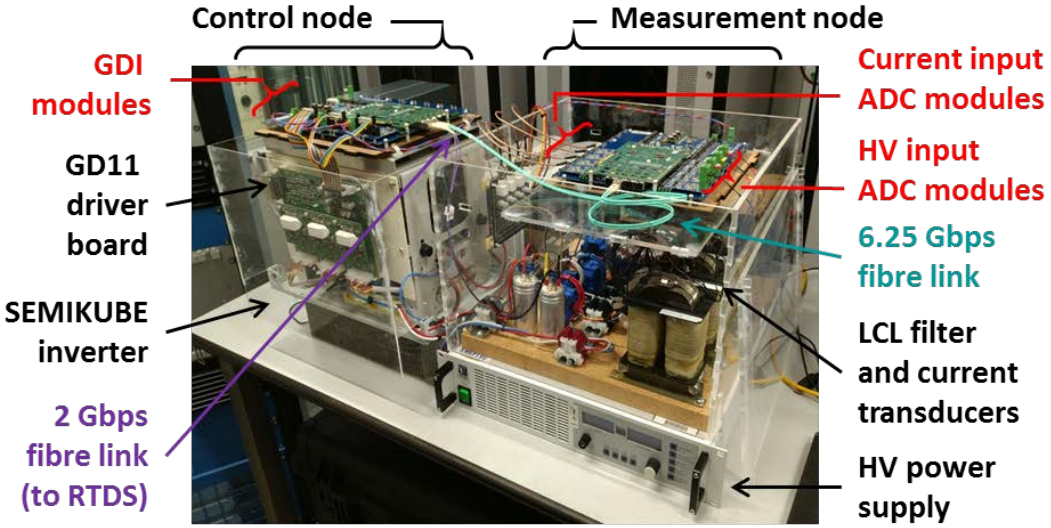


Experimental validation



M. A. H. Broadmeadow, G. R. Walker and G. F. Ledwich, "Modular and scalable control and data acquisition system for power hardware in the loop (PHIL) amplifiers," in *The Journal of Engineering*, vol. 2019, no. 17, pp. 3655-3659, 2019. doi: 10.1049/joe.2018.8035

Experimental prototype



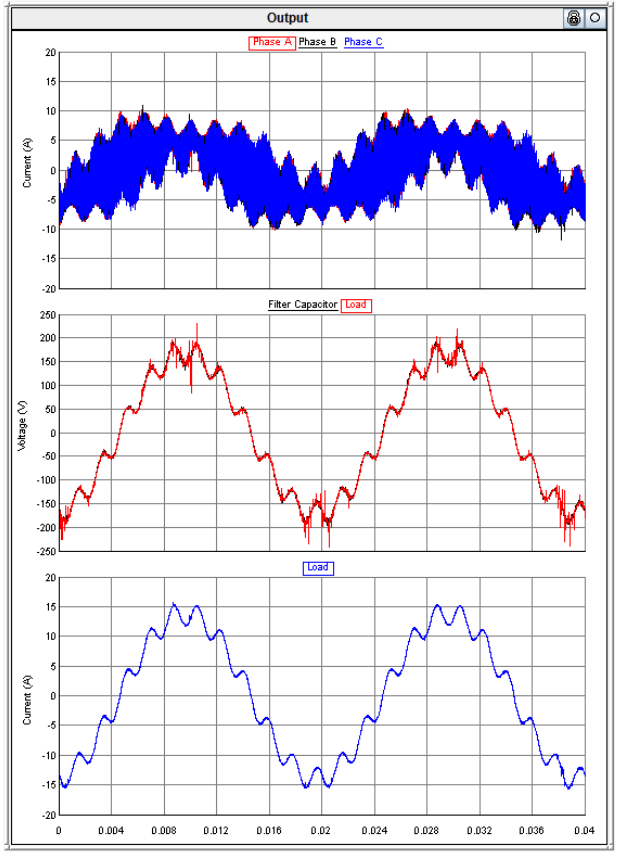
- LEM LF210-S closed loop hall-effect current sensors with 4x turns
- 1 m OM3 fibre optic cable between control and measurement nodes (AFBR-57J9AMZ transceivers)
- 5 m OM3 fibre optic cable between control node and RTDS (FTLF8519P3BNL transceivers)
- Three-phase SEMIKUBE IGBT inverter module

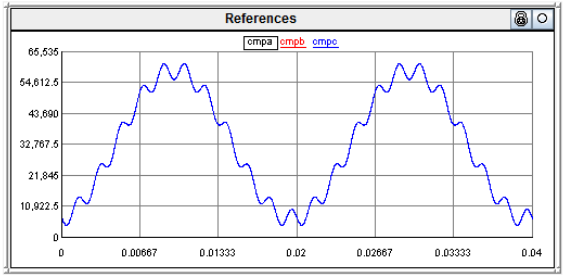
Communications and control

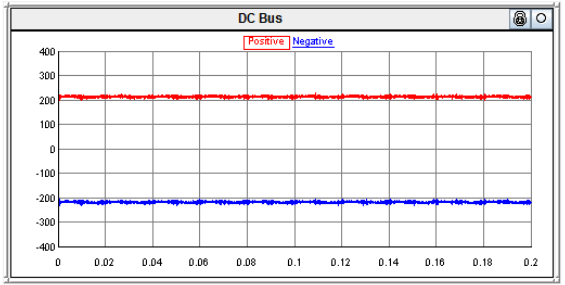
- 4x voltages & 4x currents sampled at measurement node (16-bit)
  - 8 sample MAF applied to signals
- Total of 29x 32-bit words transmitted to RTDS (sign-extended)
  - Including gate driver feedback signals, temperatures, status signals
- 3x 16-bit modulating, plus control register signal sent to control node
  - 80% modulation depth 50 Hz, plus 10% 550 Hz (11^{th} harmonic), open loop
- Aurora 8b10b framing protocol for fibre optic links
  - 6.25 Gbps line rate between control and measurement nodes
  - 2.0 Gbps line rate between control node and RTDS
- 10 kHz asymmetric PWM, arbitrary resample rate with ZOH and lockout
  - PACPWM with 32-bit accumulator and 16-bit compare
- Implemented entirely in PL portion of FPGA SoC
- Large time-step model on RTDS with 6 us timestep

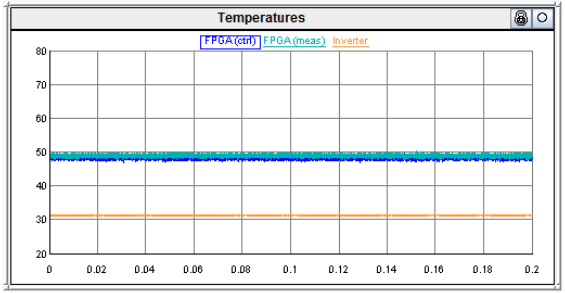
CTRL: OK
MEAS: OK
GDI: OK

Bus 0.5 V



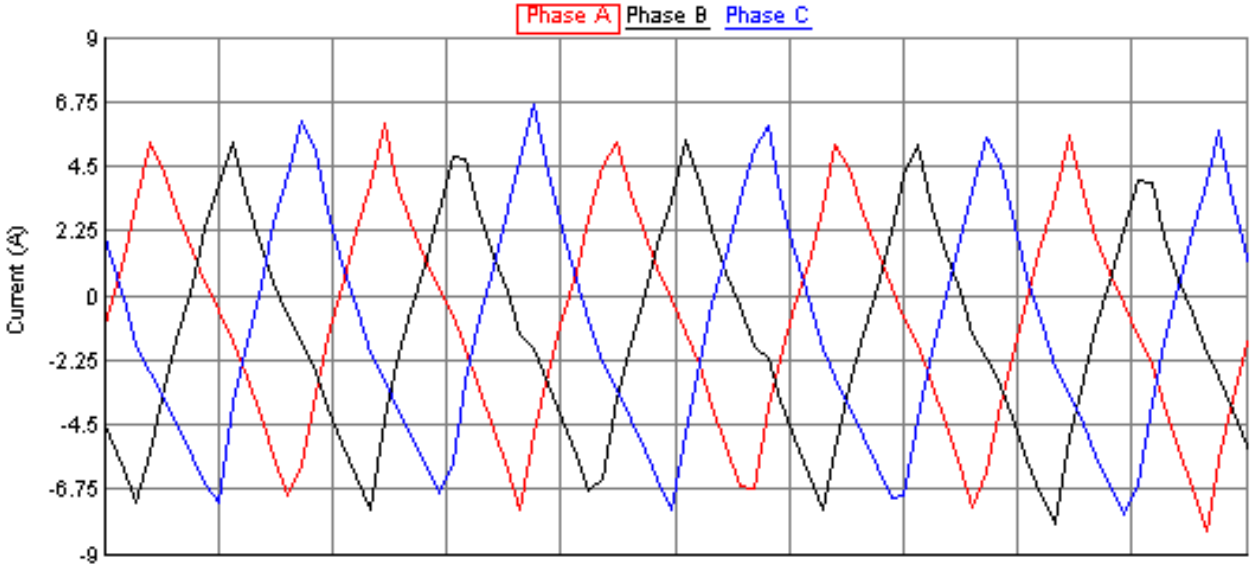






Experimental prototype operating at 120 V_{rms} 10 A_{rms} (1.2 kW)

Results: Ripple current fidelity



10 kHz ripple current as seen at RTDS. 1 MHz sample rate with 6:1 decimation

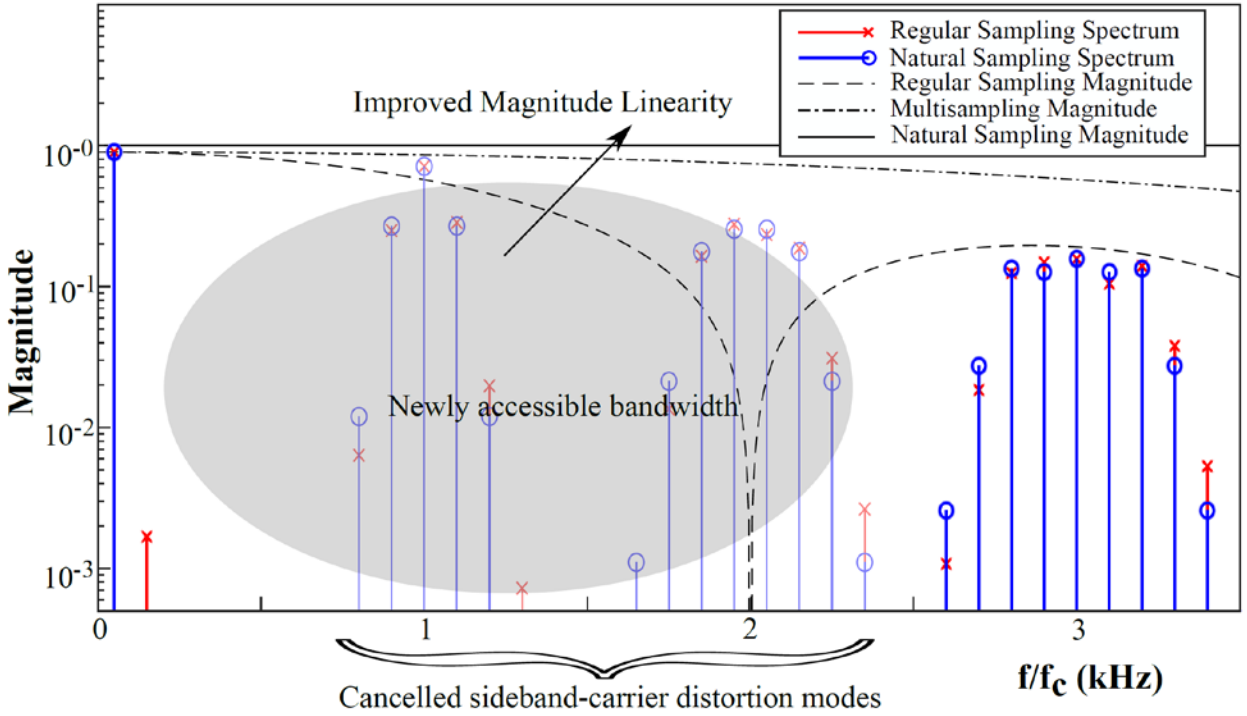
Results: Latency

- Conversion time (~1 µs) largely irreducible due to ADCs used
- Propagation delay to control node larger than expected
  - Non-optimum timing between sampling and communications sub-systems
  - Could be reduced by 1 µs
- Variability in propagation delay to/from RTDS attributable to timestep (6 µs) and lack of synchronisation

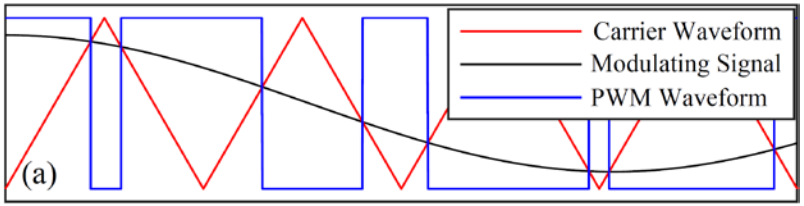
	Propagation delay (µs)		
	Min.	Typ.	Max.
Sampling instant to measurement node	–	1.02	–
Measurement node to Control node	1.14	1.18	1.23
Measurement node to control node via RTDS	9.44	–	15.72

Resampled Pulse Width Modulation (PWM)

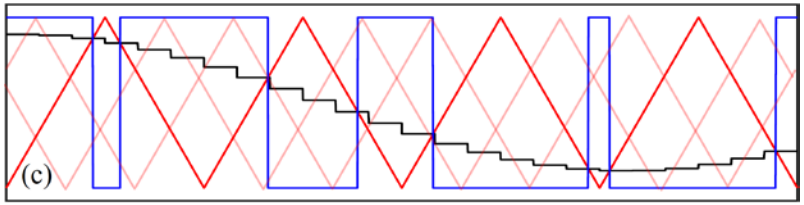
Bandwidth extension in multilevel converters



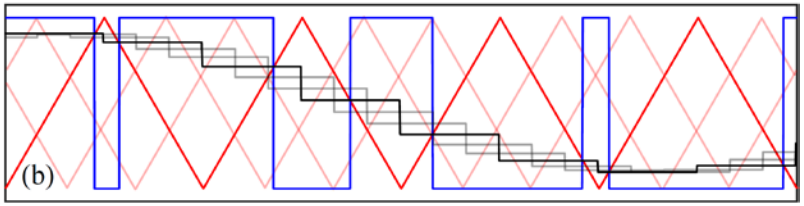
Resampled Pulse Width Modulation (PWM)



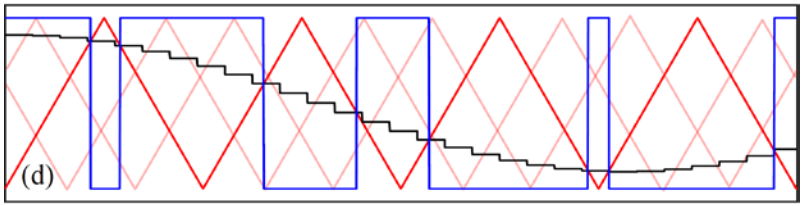
Natural Sampled



Multisampled



Regular Sampled

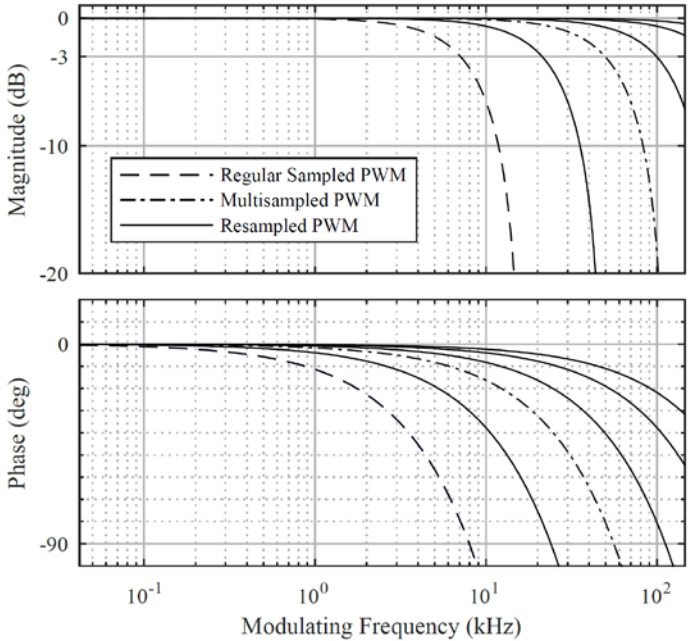


Resampled

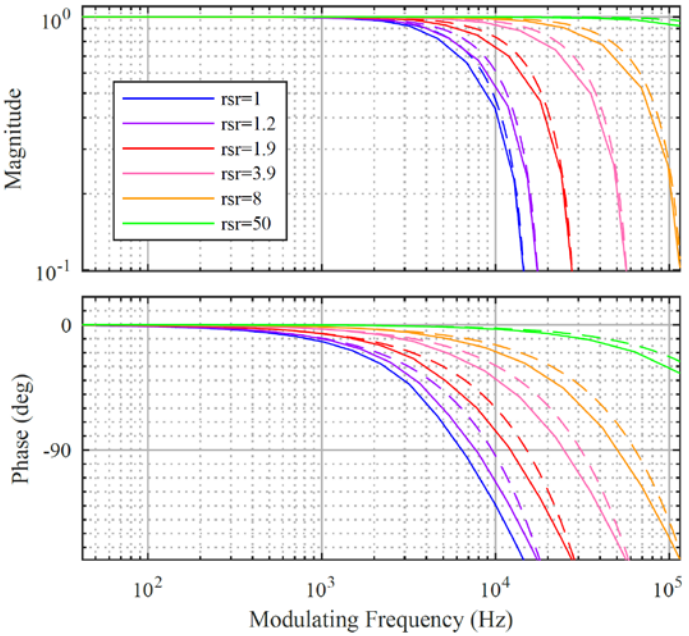
Frequency response

$$rsr = \frac{f_s}{2f_c}$$

Simulated (n_c = 7, rsr = 3, 14, 50)



Experimental (n_c = 7)

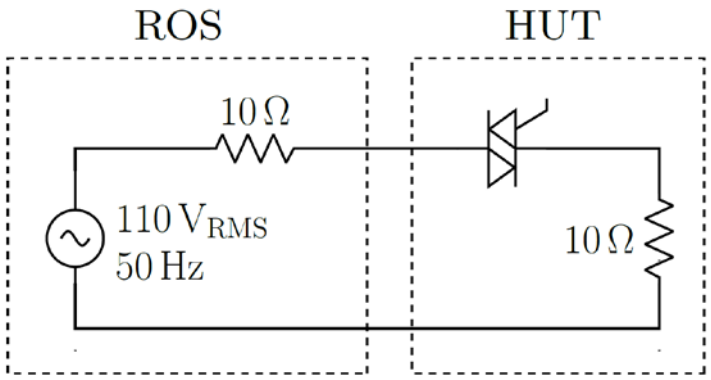


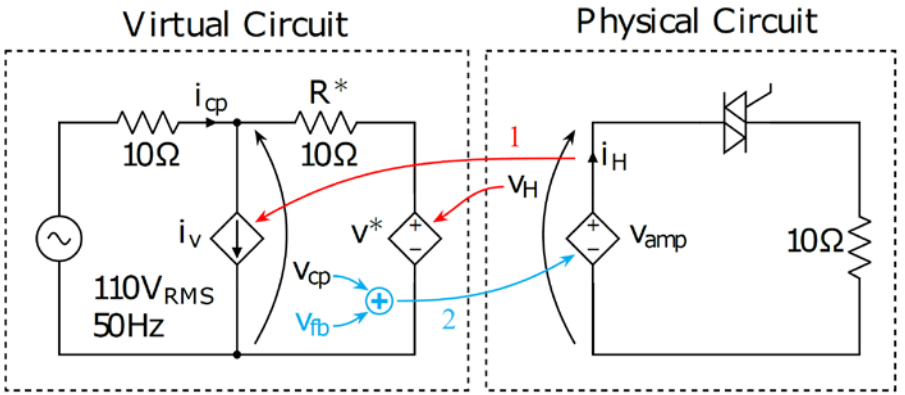
Validation of PHIL benefits

- Application to PHIL experiment with non-linear load
- Three-leg, interleaved amplifier
- Implemented using regular sampled, multisampled and resampled PWM (10.4 kHz)
- Varied RTDS timestep between 5 µs and 45 µs

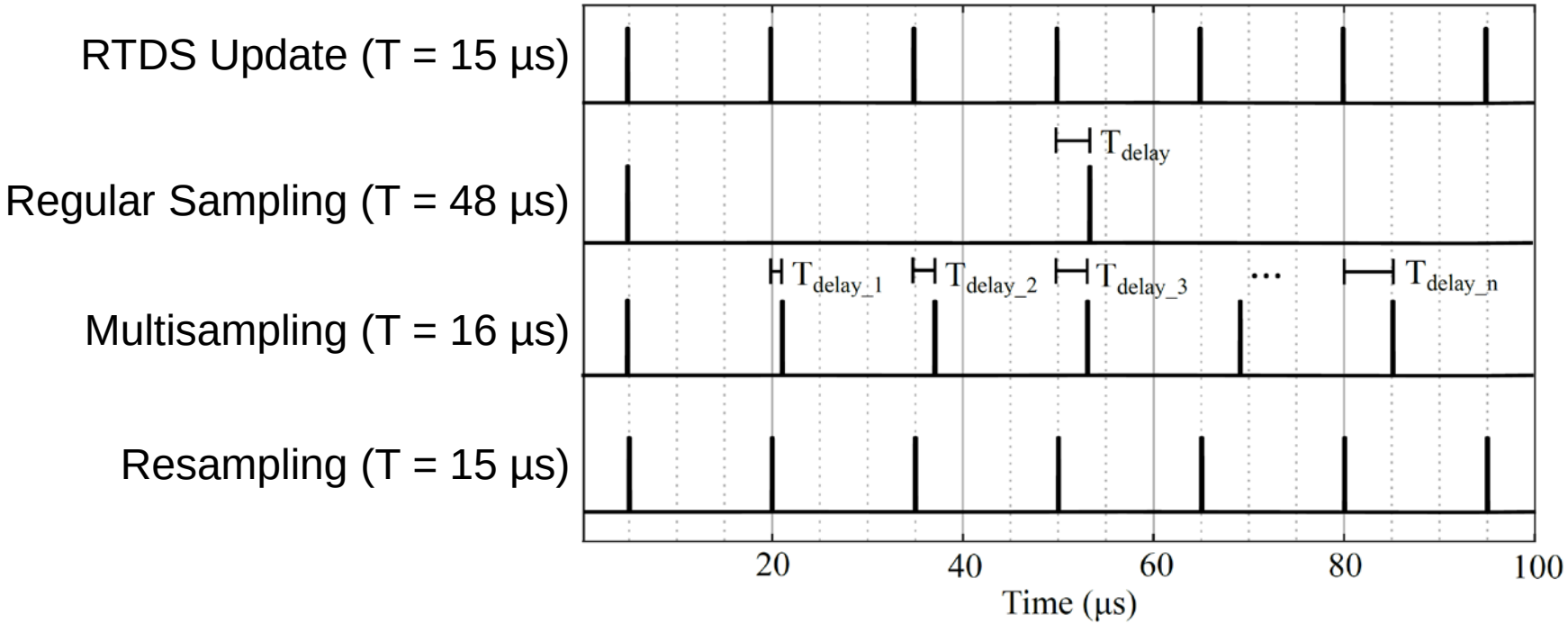
$$u(k) = v_{cp}(k) + v_{\mathrm{fb}}(k)$$

$$v_{\mathrm{fb}}(k) = -k_1 i_{C_f}(k) + k_2 \left(v_{cp}(k) - v_H(k)\right)$$



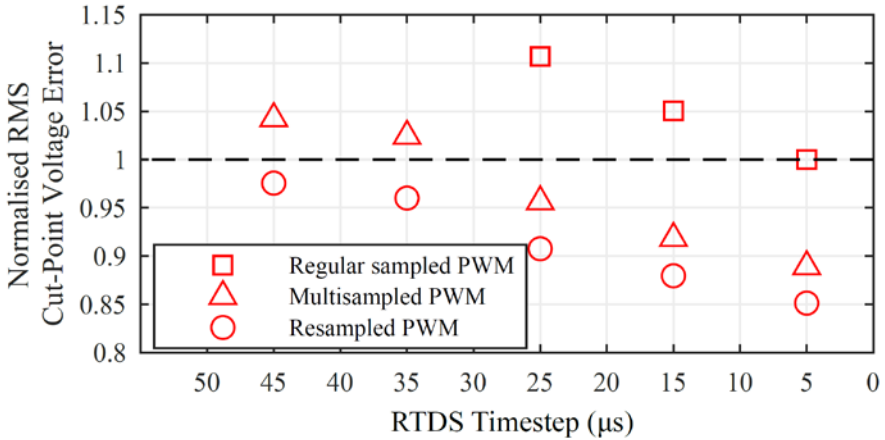


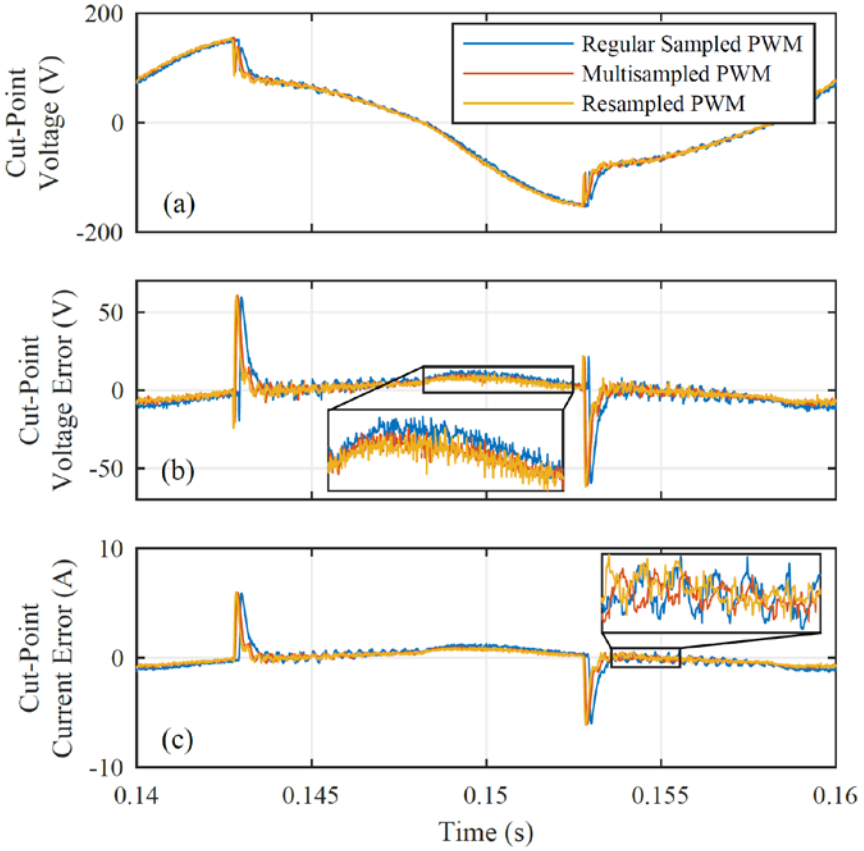
Delay benefits in RTDS applications



Results

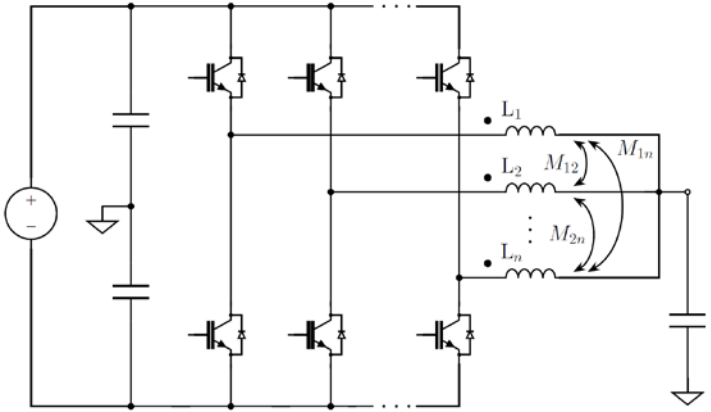
- Resampled PWM outperforms other methods in all cases
- Resampled PWM outperforms regular sampling even at slower control rates

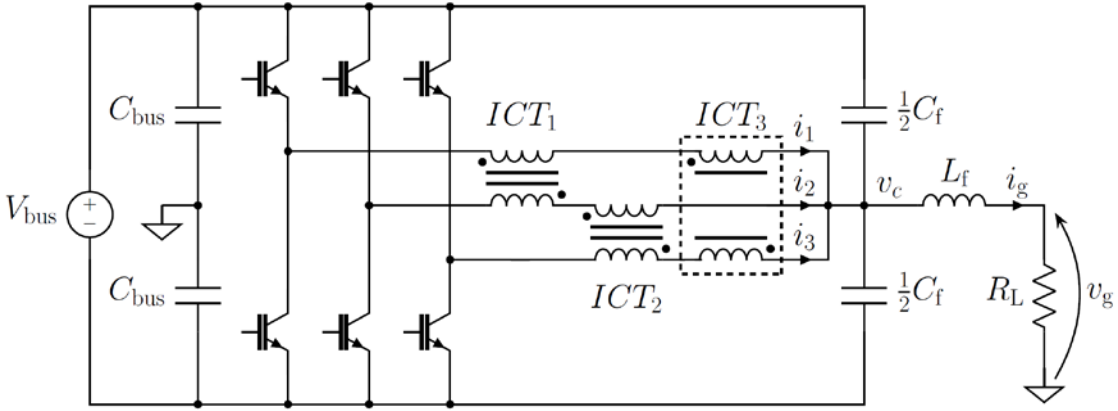




Balancing in Paralleled Interleaved Converters

Parallel interleaved converters





- Increased output current (power) and improved bandwidth
- Coupled output inductors can reduce magneit requirements
- Active control is required to maintain current balance across phase-legs

Decoupled current balancing and refence tracking

- The system model can be transformed into decoupled tracking and balancing states
- We can consequently design a control law based on state feedback which is completely decoupled

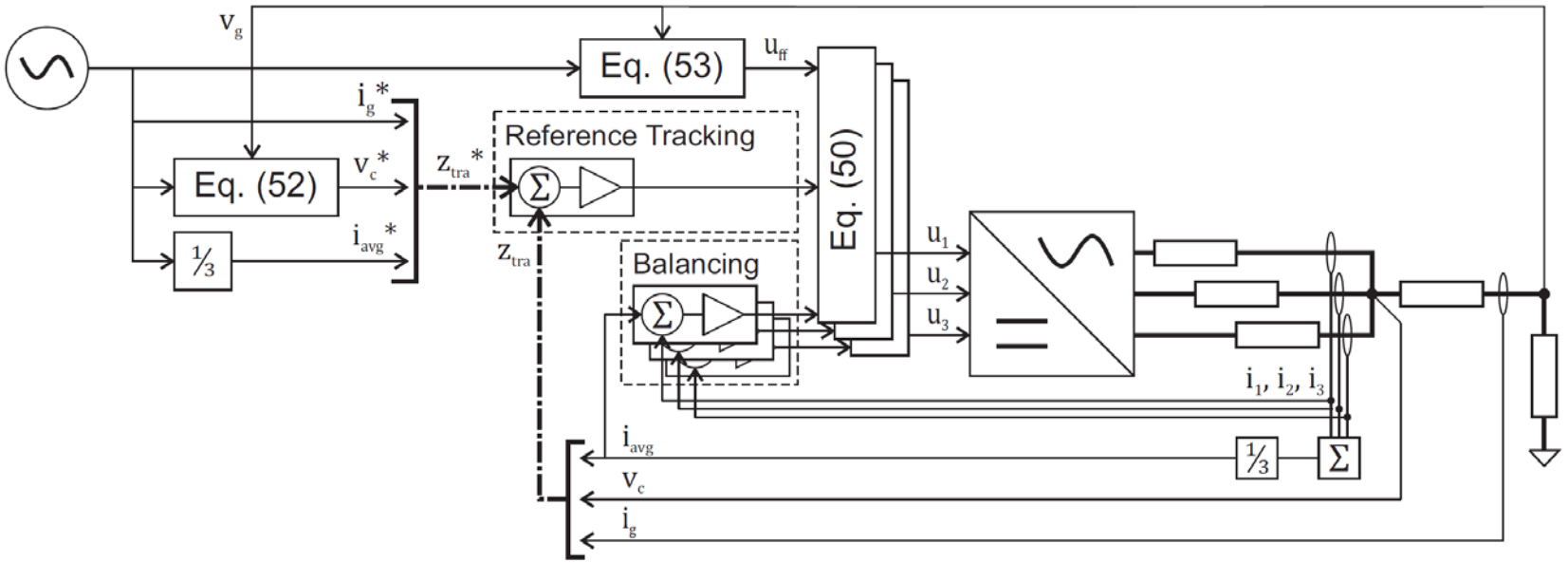
$$\begin{bmatrix} \dot{z}_{\text{tra}} \\ \dot{z}_{\text{bal}} \end{bmatrix} = \left[\begin{array}{c|c} \mathcal{A}_{11} & \\ \hline & \mathcal{A}_{22} \end{array}\right] \begin{bmatrix} z_{\text{tra}} \\ z_{\text{bal}} \end{bmatrix} + \left[\begin{array}{c|c} \tilde{\mathcal{B}}_{11} & \\ \hline & \tilde{\mathcal{B}}_{22} \end{array}\right] \begin{bmatrix} r_{\text{tra}} \\ r_{\text{bal}} \end{bmatrix}$$

$$z = \left[\begin{array}{ccc|ccc} i_{\text{g}} & v_{\text{c}} & i_{\text{avg}} & i_{\text{avg}}-i_1 & i_{\text{avg}}-i_2 & \dots & i_{\text{avg}}-i_n \end{array}\right]^{\mathsf{T}}$$

$$u_n = u_{\text{ff}} - \boldsymbol{K}_{\text{tra}} \left(\boldsymbol{z}_{\text{tra}} - \boldsymbol{z}^*_{\text{tra}}\right) - \mathcal{K}_{\text{bal}} \left(i_n - i_{\text{avg}}\right)$$

D. P. Jovanović, M. A. H. Broadmeadow, R. R. Taylor, G. R. Walker and G. F. Ledwich, "Decoupling of Current Balancing and Reference Tracking Control in Parallel Interleaved Converters," in *IEEE Transactions on Power Electronics (in press)*. doi: 10.1109/TPEL.2019.2936858

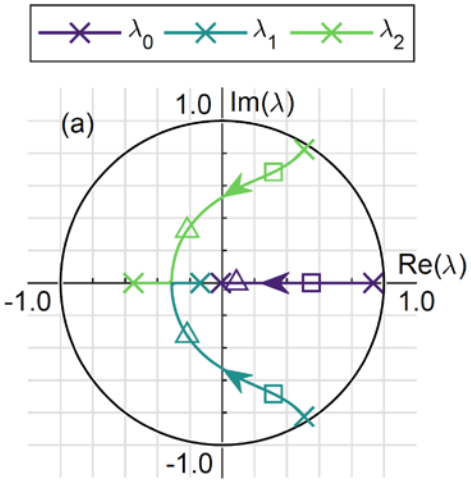
Example decoupled control block design

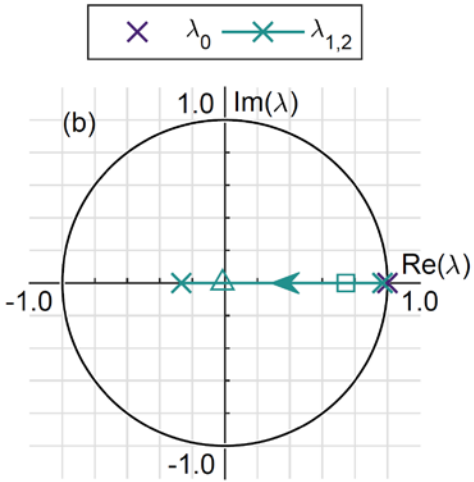


$$u_n = u_{\mathrm{ff}} - \boldsymbol{K}_{\mathrm{tra}}\left(\boldsymbol{z}_{\mathrm{tra}} - \boldsymbol{z}^*_{\mathrm{tra}}\right) - \mathcal{K}_{\mathrm{bal}}\left(i_n - i_{\mathrm{avg}}\right)$$

Decoupled design

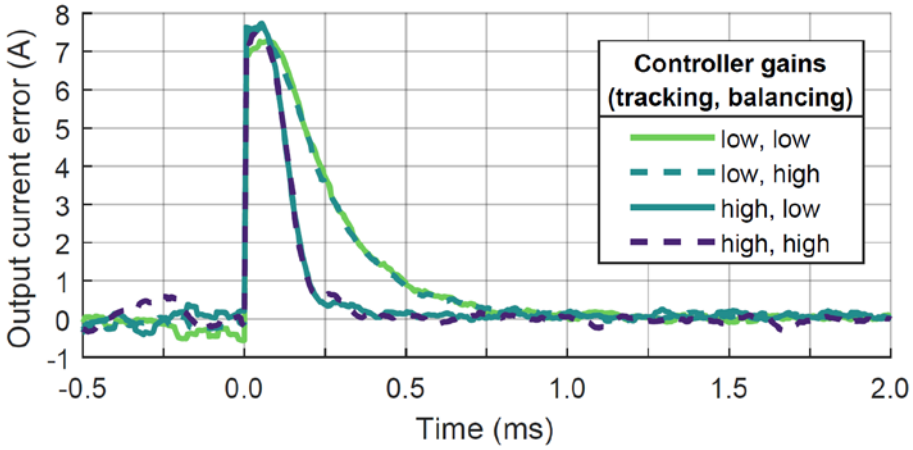
- Control designs can be conducted independently for the reference tracking and balancing systems
- “Relaxed” and “aggressive” design points were selected for both subsystems



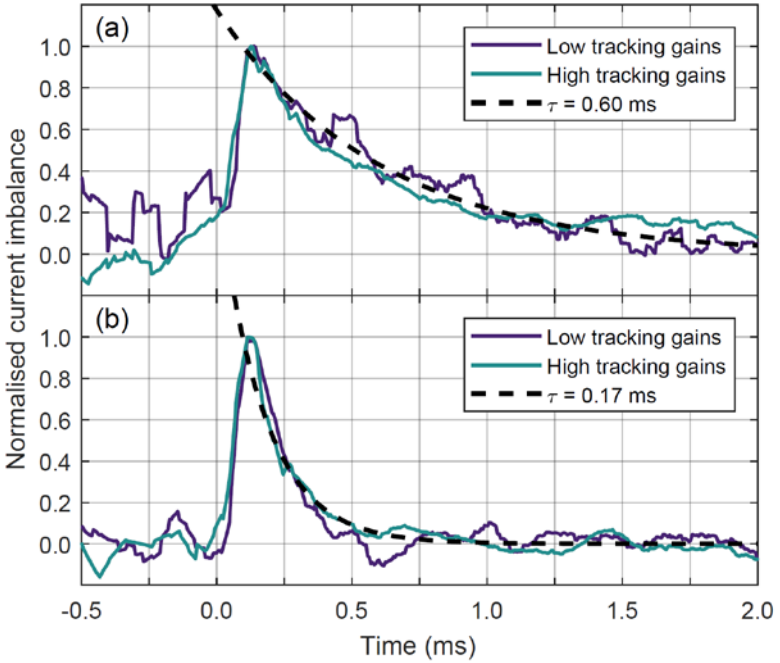


	ρ_{tra}	$\boldsymbol{K}_{\text{tra}}$			ρ_{bal}	$\mathcal{K}_{\text{bal}}$
□	7.40E^{-4}	[4.70	0.230	5.44]	2.74E^{-5}	5.49
△	1.09E^{-2}	[18.8	1.76	11.2]	1.45E^{-4}	21.9

Validation of decoupled operation

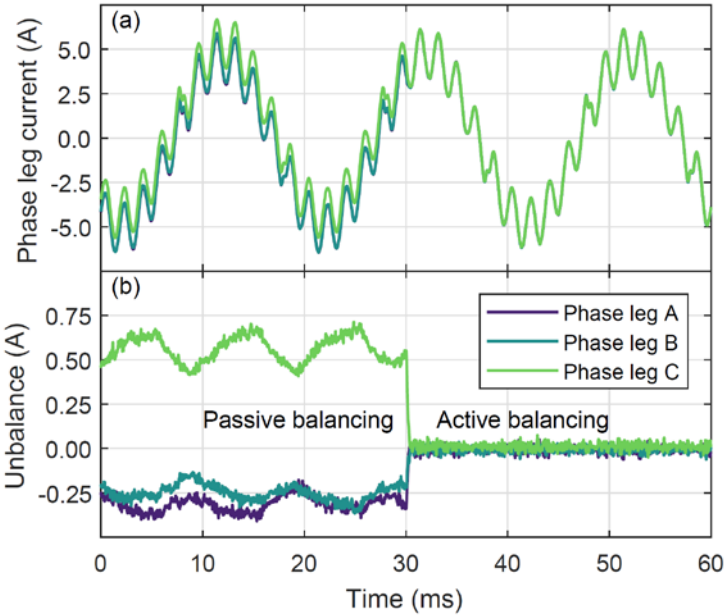


Tracking performance independent of balancing design

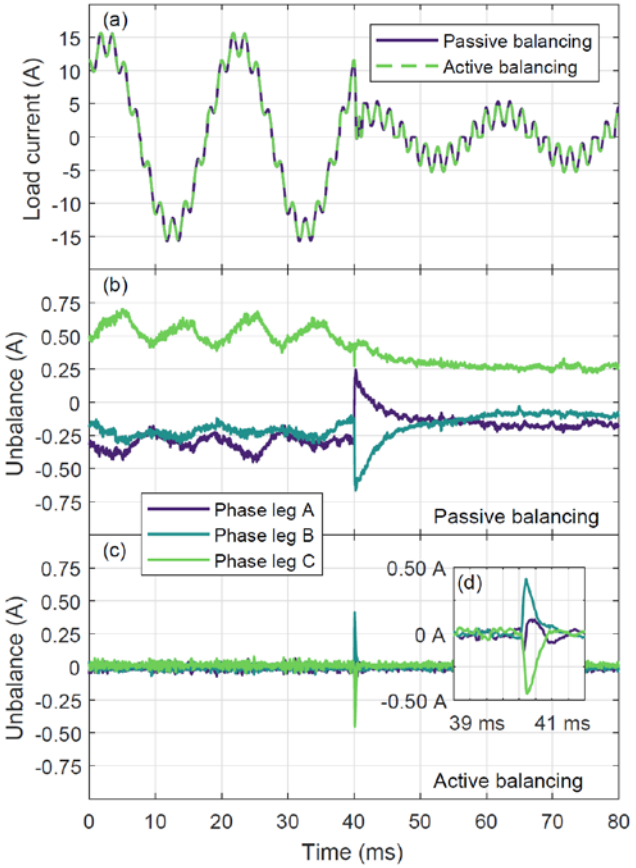


Balancing performance independent of tracking design

Balancing performance



0.1% DC offset introduced in phase leg C



Conclusion

- Modular platform for low-latency, high-bandwidth control of high-power amplifiers
- Resampled PWM provides significant benefits for multilevel converter modulation; particularly in the context of asynchronous real-time simulations
- Active balancing in parallel interleaved converters can be decoupled from, and designed independent of tracking