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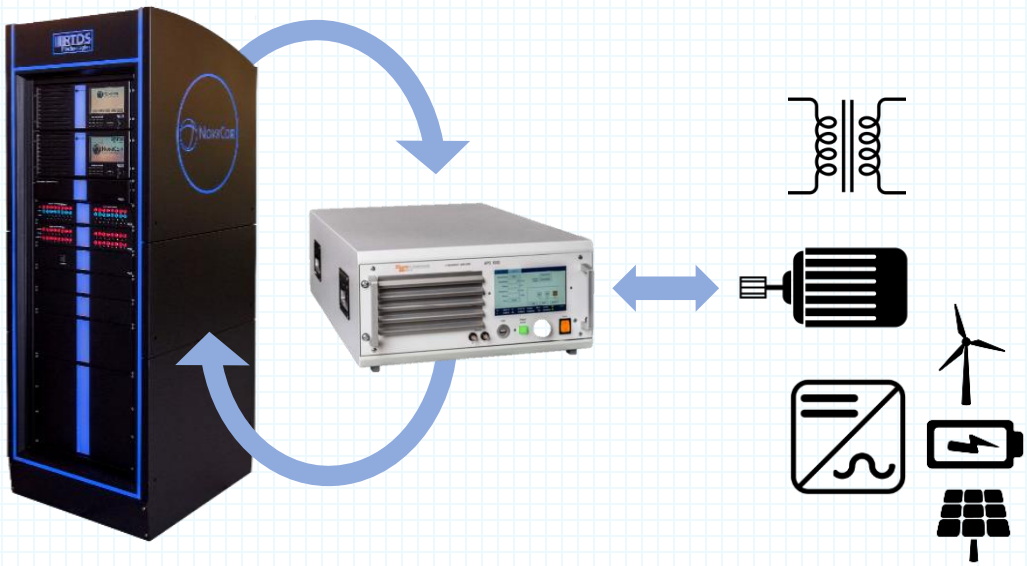
Power Hardware In the Loop Simulation (PHIL)



RTDS Technologies

Contents

1 Introduction to Hardware in the Loop (HIL) Simulations

Real-Time Digital Simulators such as RTDS™ allow external devices to be interfaced to the power system being simulated. By interfacing the physical devices to the simulation, the user is able to characterize the devices' behaviour and impact on the system. Various contingency scenarios can be run in a controlled environment to evaluate the performance of the device under test (DUT) before it is connected to the actual physical system. Simulation cases can be run to check that the device settings are appropriate and the devices' behaviour under extreme or unusual operating conditions can be verified. Having the physical equipment interfaced to the simulator also permits operators of the equipment to become familiar with its use. Hardware-in-the-Loop (HIL) simulations offer a cost-effective and safe method to test physical devices under real-time operating conditions.

HIL simulations are normally closed loop where the device under test receives signals from the simulation and provides signals back to the simulation. HIL simulations are divided into two types: **Control** HIL (CHIL) and **Power** HIL (PHIL).

In CHIL, physical control or protection relay devices are interfaced with the RTDS™ and exchange digital and/or analog signals as shown in Figure 1-1. In most CHIL applications, the signals can be exchanged at low voltage levels (±10V) allowing for a straight forward interface with the RTDS™ by using digital-analog (D/A) and analog-digital (A/D) converters. Some CHIL applications may require amplifiers to provide higher voltages and/or currents than those provided by the D/A converters of the RTDS. In such applications, the loading of the amplifiers does not affect the stability and accuracy of the interface, as the amplifier acts only as a power source i.e. 2- quadrant operation.

Recent advancements in CHIL now allows for the use of communication protocol based interfaces rather than the exchange of voltages using physical wiring. CHIL is well established with numerous applications documented in technical literature.

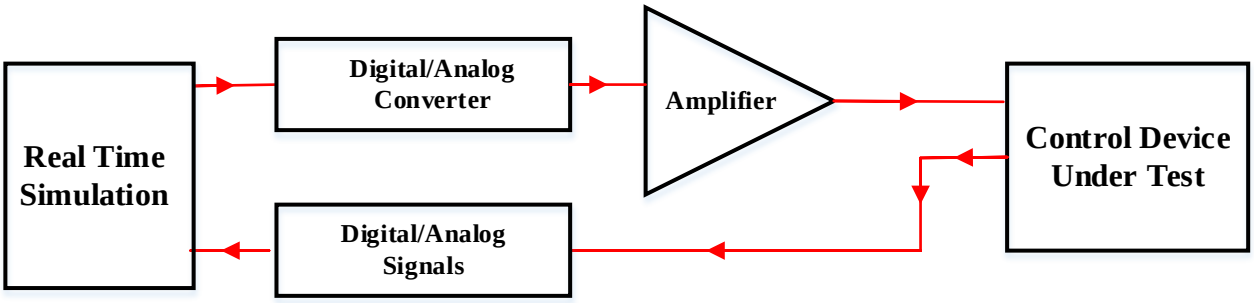


Figure 1-1 Control Hardware In the Loop (CHIL) simulations

In PHIL, power devices that are part of the power system network such as motors, inverters, generators and transformers etc. are interfaced with the simulation.

One of the first applications of PHIL was to interface the RTDS with an analogue simulator [1] [2]. In that case, part of the network was modeled within the RTDS and another part of the network was modeled using analogue components. At each interface point, an amplifier is required to provide the signals computed within the RTDS to the analogue simulator and transducers were required to measure the signals in the analogue simulator and provide those back to the RTDS. Since the amplifiers used for the interface may need to inject real and reactive power into the analogue system or extract real and reactive power from the analogue system the amplifiers must be 4-quadrant type amplifiers.

More recently, there has been interest to use PHIL to test and characterize renewables such as photovoltaics and their inverters.

Since PHIL requires a close integration with the simulation of the network, it is important that those attempting such simulations understand the nature of the interface, as well as, the capabilities and limitations of PHIL. More in-depth details and examples of PHIL are provided in the sections that follow.

2 Power Hardware In the Loop Simulations

PHIL simulations involve interfacing the RTDS with power devices such as motors, inverters, generators and/or transformers. The RTDS and the external device exchange power over the PHIL interface. Digital to analog (D/A) converters included as part of the RTDS provide analog signals at electronic levels with a voltage range of +/-10 volts and current drive in the mA range. Such voltage and current levels are well below the operating voltage/current range of the power device under test. As such, amplifiers are required in PHIL simulations to scale the signals sent from the RTDS to those required by the DUT. Figure 2-1 shows the general setup for PHIL.

In PHIL, the external device is part of the power system network and as such, timing and quality of the signals exchanged between the device and simulator plays an important part in the stability and accuracy of the interface. D/A converters, amplifiers and transducers introduce delay and noise and impact the stability and accuracy of PHIL simulations and must be carefully considered for any PHIL simulation. The following sections outline the key factors to be considered for PHIL simulations.

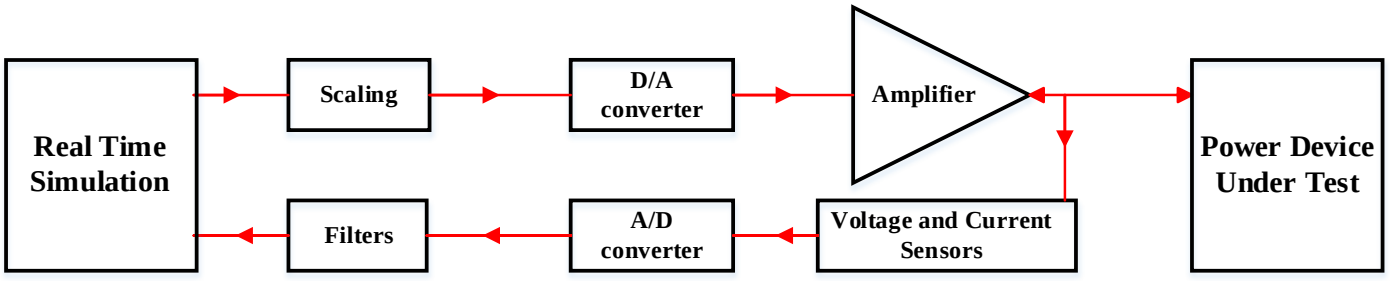


Figure 2-1 Power Hardware In the Loop (PHIL) simulations

Digital simulators such as the RTDS use the Electromagnetic Transients algorithm first introduced by Dommel [3]. The Dommel algorithm uses a nodal analysis based approach and applies numerical techniques to convert the differential equations representing the power system network to algebraic equations. Application of the numerical technique introduces a simulation time-step whereby a new *state* of the system is computed every simulation time-step. Each simulation time-step includes the solution of the network's node voltages and component branch currents. In the digital simulation the network's node voltages are computed using –

$$[V_{1\ldots n}] = [G_{nxn}]^{-1}[I_{1\ldots n}]$$

Generally, it is not possible to split the inverse conductance matrix into multiple smaller matrices. If part of the network is interfaced to the RTDS using PHIL, it effectively removes the elements of the conductance matrix that represents the network modeled externally. Depending upon the techniques used to implement the PHIL, such an interface may result in numerical instability.

Interfacing to an external device that is part of the network requires the exchange of voltages and currents between the digital simulator and the device under test. There are various methods to implement the PHIL interface. Some methods apply node voltages computed by the digital simulator to the external system and measure current as the feedback quantity and others apply computed current and measure voltage. The various methods are described in more detail below.

Consider the method where the voltage computed within the simulator is applied to the device under test. In that case, the node voltages computed in the digital simulator are sent to the amplifier and the amplifier reproduces the voltage based on its gain and applies it to the external device. The current that results due to the application of the voltage to the external device is measured and sent back to the simulator. There are time delays associated with both the forward and backward path of the interface and those time delays may lead to numerical instability. As such, it is important to minimize the delays and understand under what conditions the interface is stable.

Since the current through an inductor cannot change instantaneously and the voltage across a capacitor cannot change instantaneously, it is advantageous to arrange the PHIL interface such that voltages are applied to inductances and the current flowing through the inductance is used as the feedback signal, or alternatively currents are applied to capacitors and the capacitor voltage is used as the feedback signal.

2.1 Interface Methodology

The interface methodology determines which signals are exchanged between the RTDS and the external equipment and when those signals are exchanged during the simulation time-step. Note that interfaces that use currents as the signals applied to the external equipment require amplifiers capable of operating in current mode. Interface algorithms for PHIL simulations include [4]:

2.1.1 Ideal Transformer Method (ITM)

The ITM method is the most commonly used IA due to its high accuracy, low computation requirements and ease of implementation. The ITM works on voltage/current amplification and current/voltage feedback.

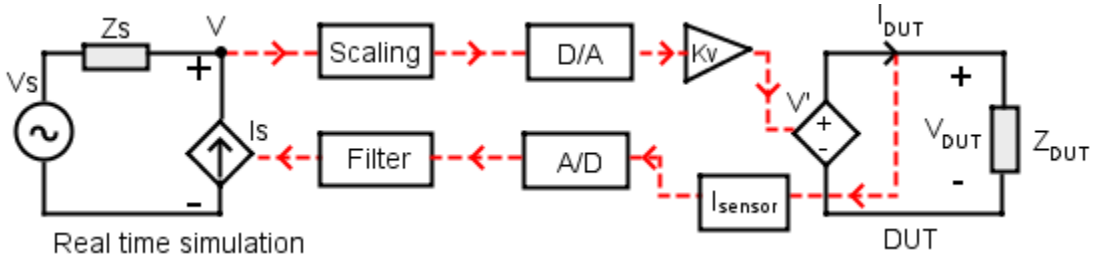


Figure 2-2 Voltage Type: Ideal Transformer Method

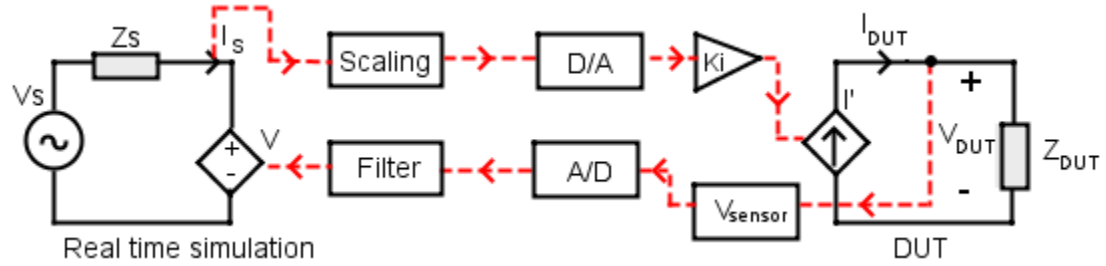


Figure 2-3 Current Type: Ideal Transformer Method

The open loop transfer function of the ITM is given by:

$$Go_{ITM\_voltage} = e^{-s\Delta T_d}\frac{Z_s}{Z_{DUT}}\ T_{amp}(s)T_{filt}(s) \tag{2.1}$$

$$Go_{ITM\_current} = e^{-s\Delta T_d}\frac{Z_{DUT}}{Z_S}T_{amp}(s)T_{filt}(s) \tag{2.2}$$

Where:

- ΔT_d is the total time delay in the PHIL interface.
- Z_s is the equivalent impedance of the network in the RTS.
- Z_{DUT} is the impedance of the device under test.
- T_{amp} is the transfer function of the amplifier
- T_{filt} is the transfer function of the filter
- K_v/K_i is the gain of the voltage/current amplifier

From the open loop transfer function, the stability of the voltage and current type ITM is largely determined by the magnitude of the impedance ratio and the total time delay as shown by the Nyquist contour in Figure 2-4. To avoid instability using the ITM interface, the impedance ratio should satisfy the following criteria:

Voltage ITM: $\left|\frac{Z_S}{Z_{DUT}}\right| \leq 1$ (2.3)

Current ITM: $\left|\frac{Z_{DUT}}{Z_S}\right| \leq 1$ (2.4)

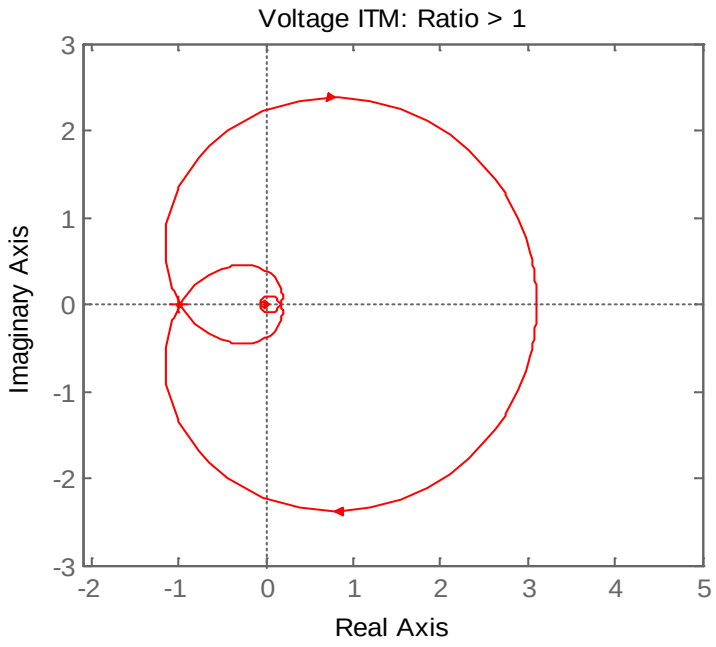


Figure 2-4 Nyquist Contour for Voltage Type ITM

The analysis above presumes a pure time delay, given by the factor $e^{-s\Delta T_d}$ in equations 2.1 and 2.2. The methodology applied in the RTDS sends the voltage (or current) to the amplifier as soon as possible after the voltage (or current) is computed and initiates the current (or voltage) read just before it is required in the computations within the Dommel algorithm used in the simulator's network solution. Thus, the delay is not purely one simulation time-step, but rather is based on the communication delays, amplifier response characteristics and transducer characteristics (including filters). This is discussed in greater detail later in section 3.3.2 below.

2.1.2 Transmission Line Method (TLM)

The TLM uses a linking inductor or capacitor to interface the RTS with the DUT.

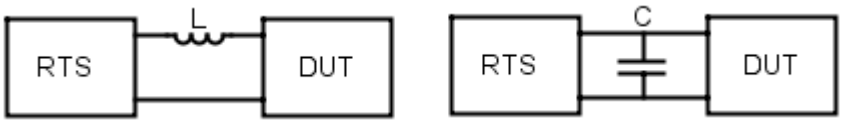


Figure 2-5 Linking component separating RTS and DUT

The inductor or capacitor is taken as a Bergeron transmission line and modeled as an equivalent Norton circuit or Thevenin circuit. The equations of the TLM method are given by:

$$Z_{lk} = \frac{L}{\Delta T_d} \quad or \quad Z_{lk} = \frac{\Delta T_d}{C} \tag{2.5}$$

$$V_1 = V_{DUT}(t - \Delta T_d) + Z_{lk} I_{DUT}(t - \Delta T_d) \tag{2.6}$$

$$V_2 = V(t - \Delta T_d) + Z_{lk} I_s(t - \Delta T_d) \tag{2.7}$$

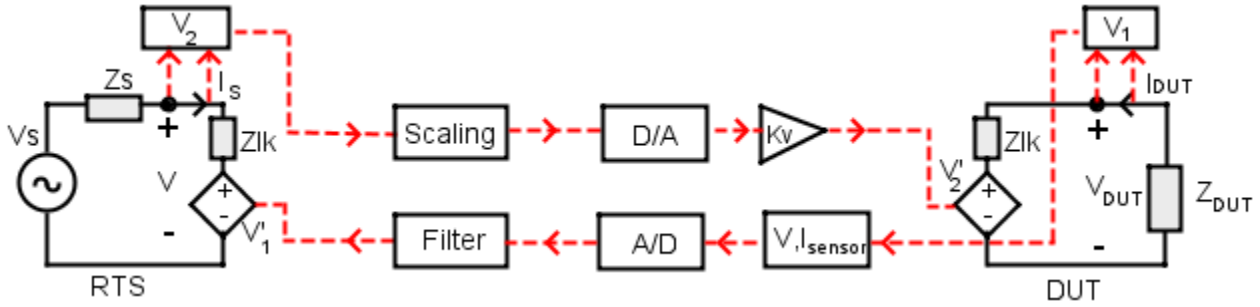


Figure 2-6 Transmission Line Method (TLM) - Thevenin Equivalent

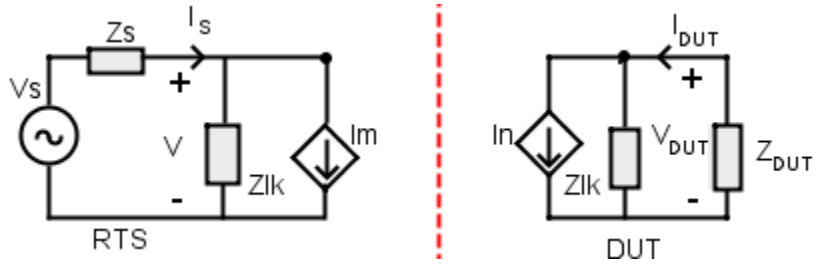


Figure 2-7 Transmission Line Method (TLM) - Norton Equivalent

Where:

ΔT_d is the travel time of the transmission line which becomes the total time delay in the PHIL simulation.

The open loop transfer function of the TLM is given by:

$$Go_{TLM} = \frac{1 - \beta e^{-2s\Delta T_d}}{1 + \beta e^{-2s\Delta T_d}} \frac{Z_s}{Z_{lk}} T_{amp}(s) T_{filt}(s) \tag{2.8}$$

$$\beta = \frac{Z_s - Z_{lk}}{Z_s + Z_{lk}} \tag{2.9}$$

For stability of the TLM, the time delays introduced by the D/A, A/D, amplifier, sensors and filters should be taken into consideration when selecting the minimum length of the interface transmission line.

$$\tau = \Delta T_d = length(km) * \sqrt{L\left(\frac{H}{km}\right) * C\left(\frac{F}{km}\right)} \quad (2.10)$$

$$length\ (km) = \tau\ (s) * speed\ of\ light\ \left(\frac{km}{s}\right) \quad (2.11)$$

$$\tau > T_{D/A} + T_{A/D} + T_{amp} + T_{filt} + T_{sensors} + \Delta T_{time\_step} \quad (2.12)$$

The TLM is highly stable due to the use of trapezoidal integration but its limitations include [4]:

- Reduced accuracy due to power loss in the linking impedance. The power loss in Z_{lk} must be taken into account when sizing the power amplifier.
- Assuming a fixed total time delay introduces errors in the PHIL results as the total time delay varies with the test conditions and the frequency of the PHIL simulation.
- The wiring of the linking impedance introduces more complexity in the PHIL implementation. The linking impedance must be properly sized and changed whenever the circuit configuration changes reducing the flexibility of the TLM.

2.1.3 Partial Circuit Duplication (PCD)

The partial circuit duplication method includes a linking impedance Zab in the simulated system and also on the hardware side. Large values of the linking impedance improves the stability of the interface but introduces inaccuracies due to increased power losses. The open loop transfer function of the PCD method is given by [4]:

$$Go_{PCD} = \frac{Z_s Z_{DUT}}{(Z_s + Z_{ab})(Z_{DUT} + Z_{ab})} e^{-s\Delta T_d}\ T_{amp}(s) T_{filt}(s) \quad (2.13)$$

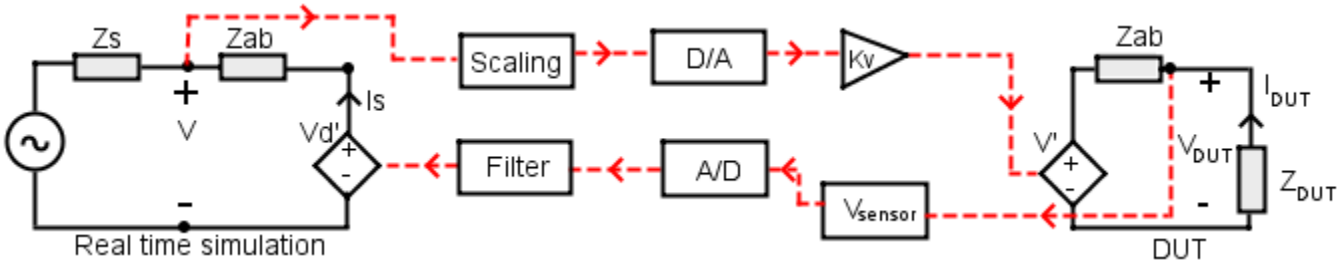


Figure 2-8 Partial Circuit Duplication (PCD)

2.1.4 Damping Impedance Method (DIM)

The damping impedance method has a linking impedance Z_{ab} similar to the PCD and includes a damping impedance Z_{damp}. The DIM has very high stability when the value of Z_{damp} is equal to Z_{DUT}. The open loop transfer function of the DIM method is given by [4]:

$$Go_{DIM} = e^{-s\Delta T_d} \frac{Z_s(Z_{DUT} - Z_{damp})}{(Z_s + Z_{damp} + Z_{ab})(Z_{DUT} + Z_{ab})} \; T_{amp}(s)T_{filt}(s) \tag{2.14}$$

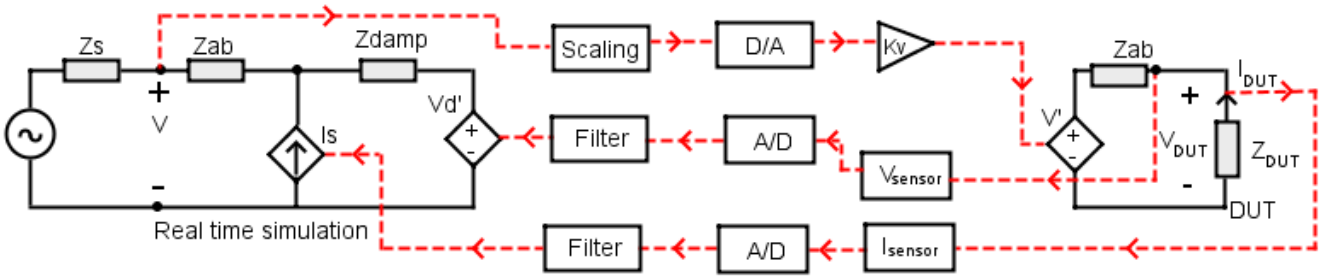


Figure 2-9 Damping Impedance Method (DIM)

2.2 Simulation Time Step

Time delays in the PHIL interface depends on the following –

i) Time required to send the computed voltage (or current) to the amplifier

ii) Time required by the amplifier to produce the scaled voltage at its output terminals

iii) Time required to send to transducer read request

iv) Time required for the transducer to measure the interfaced signal

v) Time required for the measured signal to be sent into the RTDS

vi) The simulation time-step

Items i) – v) above are determined by the physical equipment comprising the interface. The simulation time-step can be set for the simulation case and is determined by the nature of the system being simulated.

The small time step feature can be used to reduce the time-step related delays in the PHIL simulation as the time step is usually between 1.4µsecs - 3µsecs; however stricter node limitations and limited model availability restrict the size of the simulated network that can be achieved in the small time step.

2.3 Amplifier

For closed loop PHIL simulations, the amplifier must be able to operate in all four quadrants of the power plane (i.e. they must be able to sink and source real and reactive power).

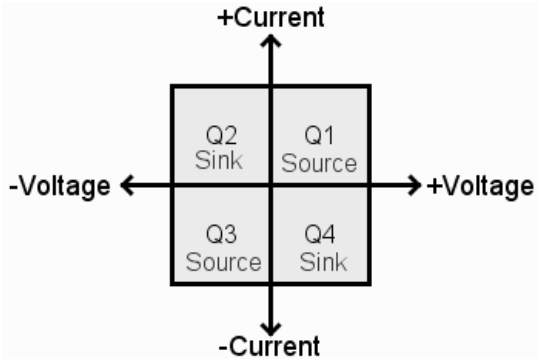


Figure 2-10 Four quadrant amplifier operation for PHIL simulations

Commonly used amplifiers are controlled voltage or controlled current amplifiers. Amplifiers capable of operating as both controlled voltage and controlled current can provide extended capability at a reduced cost.

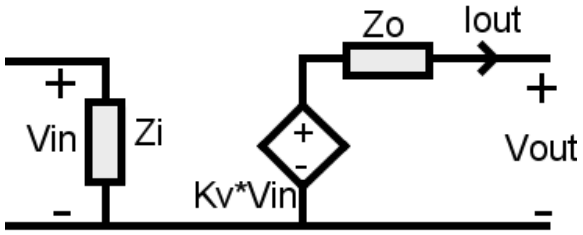


Figure 2-11 Controlled Voltage Amplifier

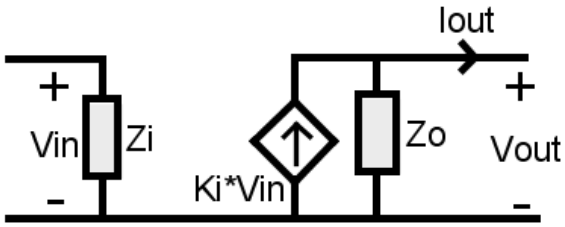


Figure 2-12 Controlled Current Amplifier

Where:

- Zi Input impedance of the amplifier
- Zo Output impedance of the amplifier
- Kv, Ki is the amplifier gain (voltage/current)

Depending on the application, amplifiers can be configured to operate in either AC or DC mode. In DC mode, the input signal is directly coupled to the amplifier input. In AC mode, a capacitive filter is switched between the amplifier input and input signal terminals to suppress the DC components of the input signal. AC operation is used to avoid DC saturation when testing transformers or motor devices. Amplifiers with AC or DC operation option provide extended capability for various PHIL applications. Table 1 lists a comparison of amplifiers used for PHIL simulations.

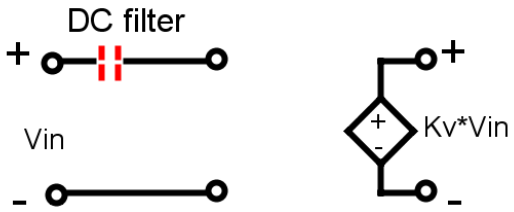


Figure 2-13 Capacitive filter used in AC mode

Table 1 Amplifiers for PHIL Simulation

Amplifier operation	Definition	Complexity	Types and Manufacturer	Dynamic Response	Cost	Flexibility and Application Range
Linear	Change in output proportional to change in input	Low	Voltage or Current	High bandwidth and fast response time (<6µs)	High	Low flexibility (can operate only as voltage or current amplifier). Difficult to build in MW range due to high power losses.
Non-Linear	Change in output NOT proportional to change in input	High (Additional control circuitry required)	Switched mode	Reduced bandwidth and slow response time (>50µs) (due to additional control circuitry)	Low	High Flexibility (can operate as voltage and/or current). Commonly used in the MW range.

The following characteristics must also be carefully considered to select the amplifier for the PHIL application:

- Power ratings of the device under test
- Amplifier interface connections
- Source and sink power ratings of the amplifier
- Amplifier response times
- Amplifier slew rate

- Amplifier harmonic distortion and frequency resolution
- Amplifier input and output voltage/current range
- Amplifier input and output impedances
- Amplifier protection (overload, heating, short circuit operation)

The bandwidth of the amplifier represents the frequency range over which the amplifier is able to effectively amplify the input signal. The selected amplifier should have sufficient bandwidth to amplify the input signal at the frequencies of interest with minimum harmonic distortion. The bandwidth is usually specified from DC to the large signal response (-3dB bandwidth).

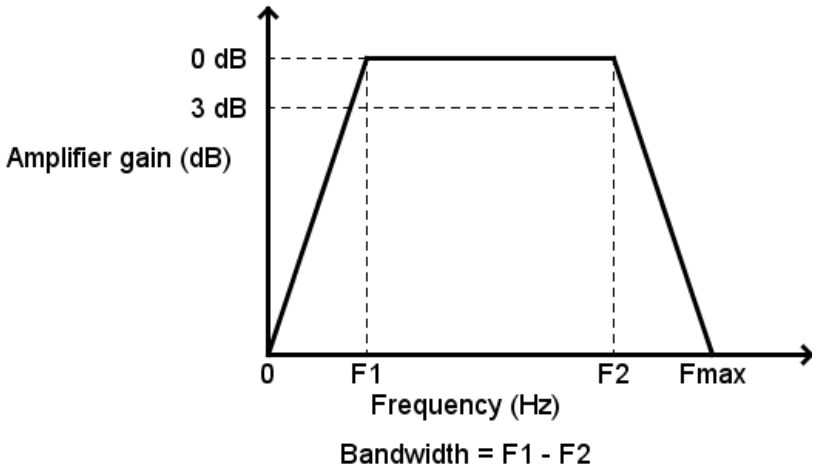


Figure 2-14 Amplifier bandwidth

The amplifier response times and frequency behaviour can be characterized from its step response as shown in Figure 2-15.

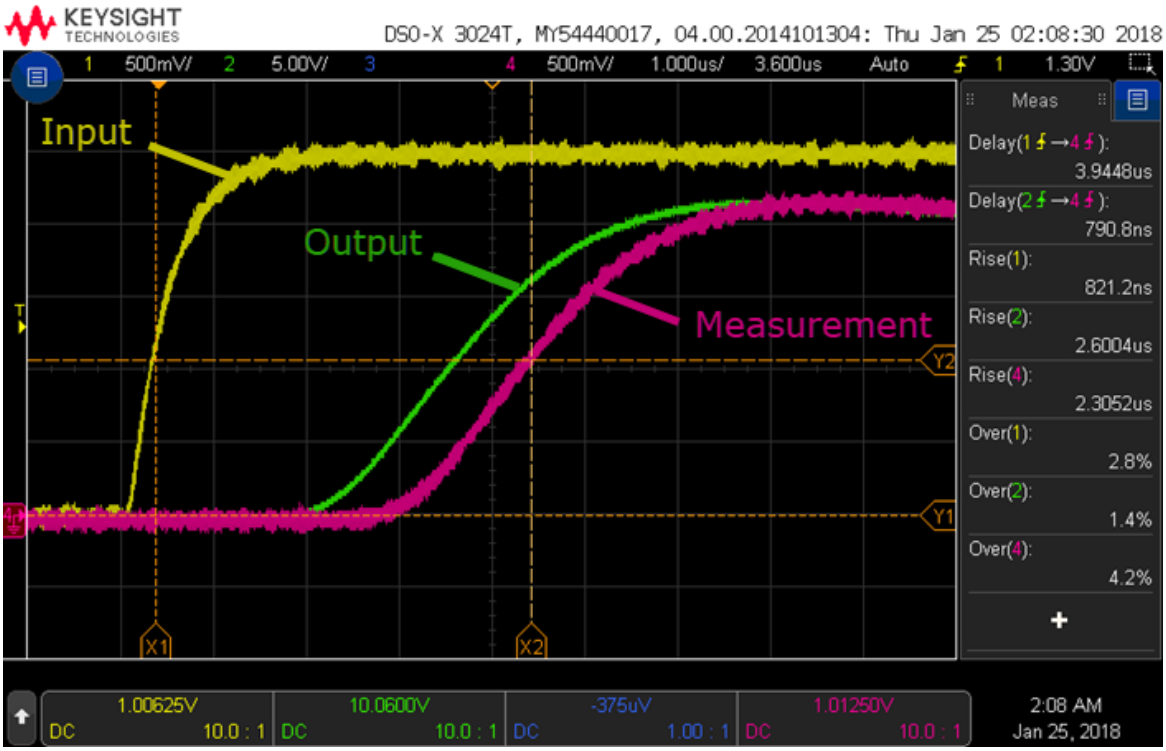


Figure 2-15 Amplifier step response

2.4 Noise reduction/filtering

Filters implemented in hardware/software are required in PHIL simulations to reduce the impact of noise on the PHIL simulation. The voltage and current measurement sensors, physical wiring and electromagnetic coupling between the interfaces devices introduces noise in the PHIL simulation which impacts the accuracy and stability of the simulation. The errors introduced by noise can be increasingly amplified in the interface until the hardware limits on the interface devices are exceeded. Filters, however, introduce frequency dependent magnitude attenuation and additional delays to the PHIL simulation. The amount of time delay and signal attenuation introduced by the filter is determined by the selected filter design and filter cut-off frequency. The filter parameters should be selected to offer an acceptable trade-off between improved stability and accuracy of the PHIL simulation.

The measured analogue signal fed back to the digital simulator via an A/D converter requires an anti-aliasing filter before the A/D's sampler.

3 Characterizing the PHIL interface

Since the loading of the amplifier affects the stability of the PHIL interface, it is recommended to characterize the interface to obtain the required gains, amplifier behaviour, noise errors of the measurement sensors and the time delays. The amplifier used in the discussions below is the APS 1000 amplifier made by Spitzenberger & Spies.

3.1 Amplifier Gain

The APS 1000, 4-quadrant power amplifier can be operated in either Constant Voltage (CV) or Constant Current (CC) mode.

The _rtds_AuroraSPS.def component available in the RSCAD/Draft component library is used to establish the Aurora link between the RTDS and the APS1000. The component automatically calculates the appropriate scaling factors so that a 1:1000 relationship exists for all signals exchanged between the RTDS and the APS1000.

Note that the 1:1000 scaling relationship is used to convert the default units of kV and kA in the RTDS to the units of V and A used in the APS1000.

For example, a signal sent from the RTDS simulation to the APS1000 with a floating point value of 0.01 (interpreted in the RTDS as either kV or kA) would command 10.0V or 10.0A depending on operating mode of APS1000. (i.e. either CV or CC mode) Similarly, a measured voltage of 10.0V from the amplifier would result in a signal value of 0.01 within the RTDS simulation.

3.2 Interface noise

To investigate the noise associated with the interface, a 0.1kV-RMS sine wave generated within the RTDS simulation acts as the control value for the output voltage of APS1000 and is sent to the APS1000 using an Aurora Link. In response to receiving the control value for the output voltage, the APS1000 then waits for a user defined measurement delay after which it returns it's the resulting voltage and current measurement values via the Aurora Link. Details regarding how exactly these

measurements are made are specific to operation of the APS1000. The complete interface noise test setup is shown in Figure 3-1.

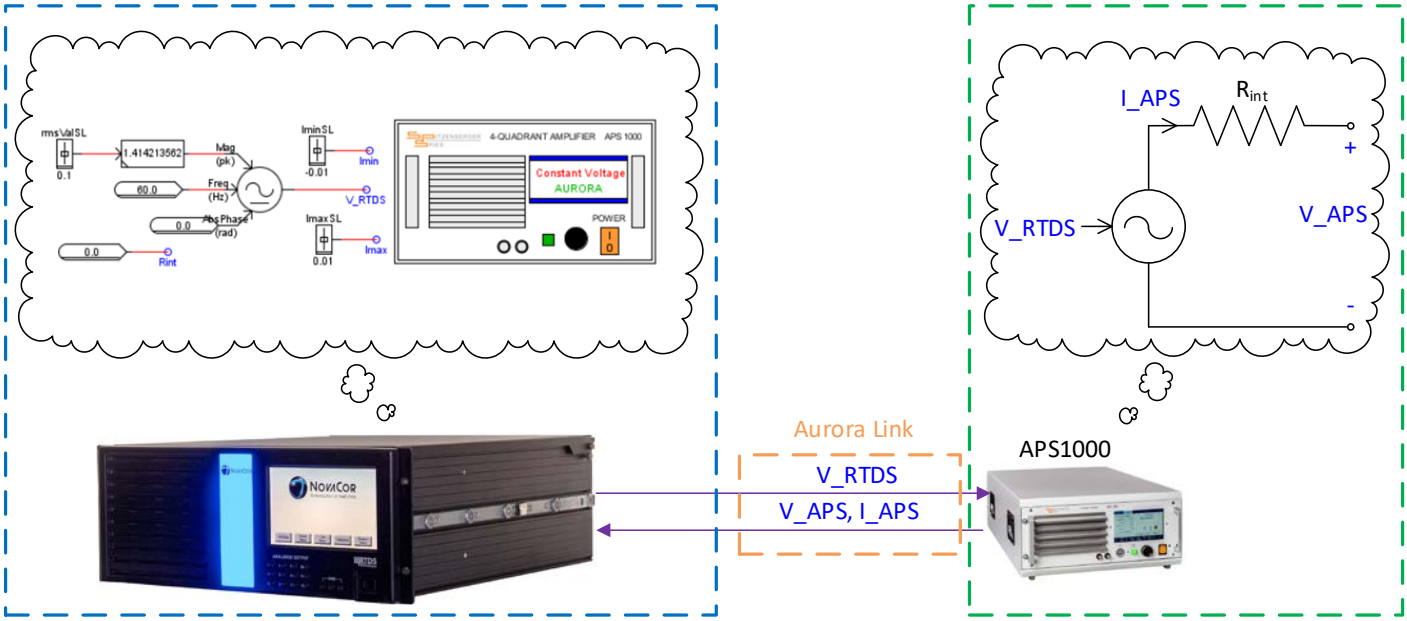


Figure 3-1 Interface noise test setup

The RSCAD/Draft canvas for this test case is shown below in Figure 3-2.

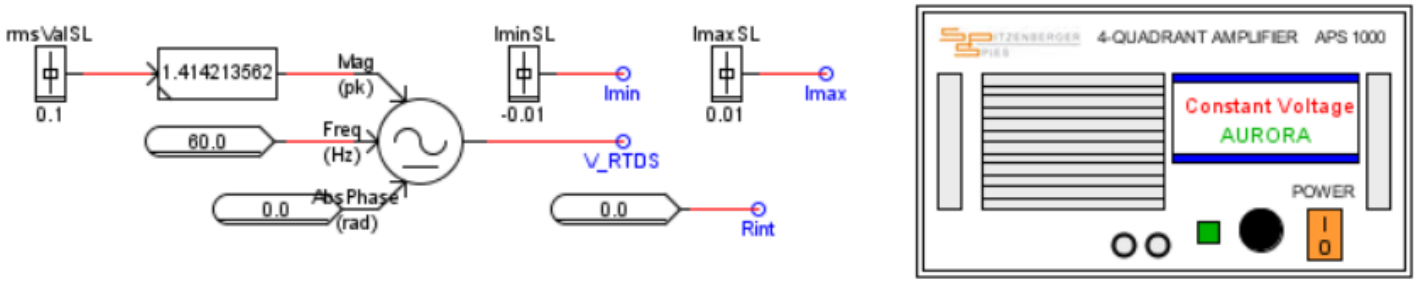


Figure 3-2 Draft canvas for interface noise investigation

Figure 3-3 shows a plot of the control value for output of the voltage APS1000 and the measured output voltage from the APS1000. When observing the measured output from the APS1000 it is difficult to detect any noticeable noise superimposed on the signal.

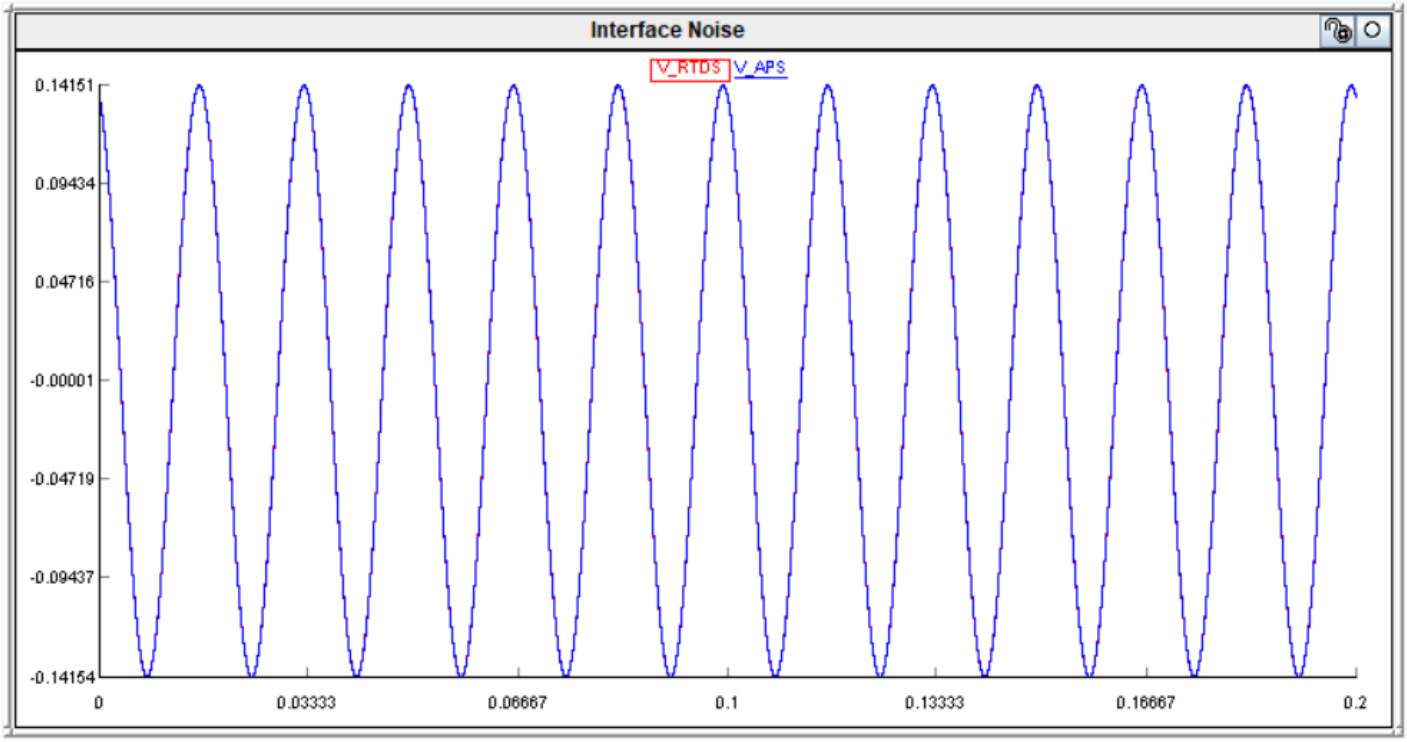


Figure 3-3 Voltage command and measurement waveforms (Zoomed out)

Zooming in on the waveform even further as shown in Figure 3-4, it is still difficult to identify any noticeable noise. However, one can clearly see a time delay between two signals. This is time delay is discussed in more detail later on in section 3.3.2 Time Delay.

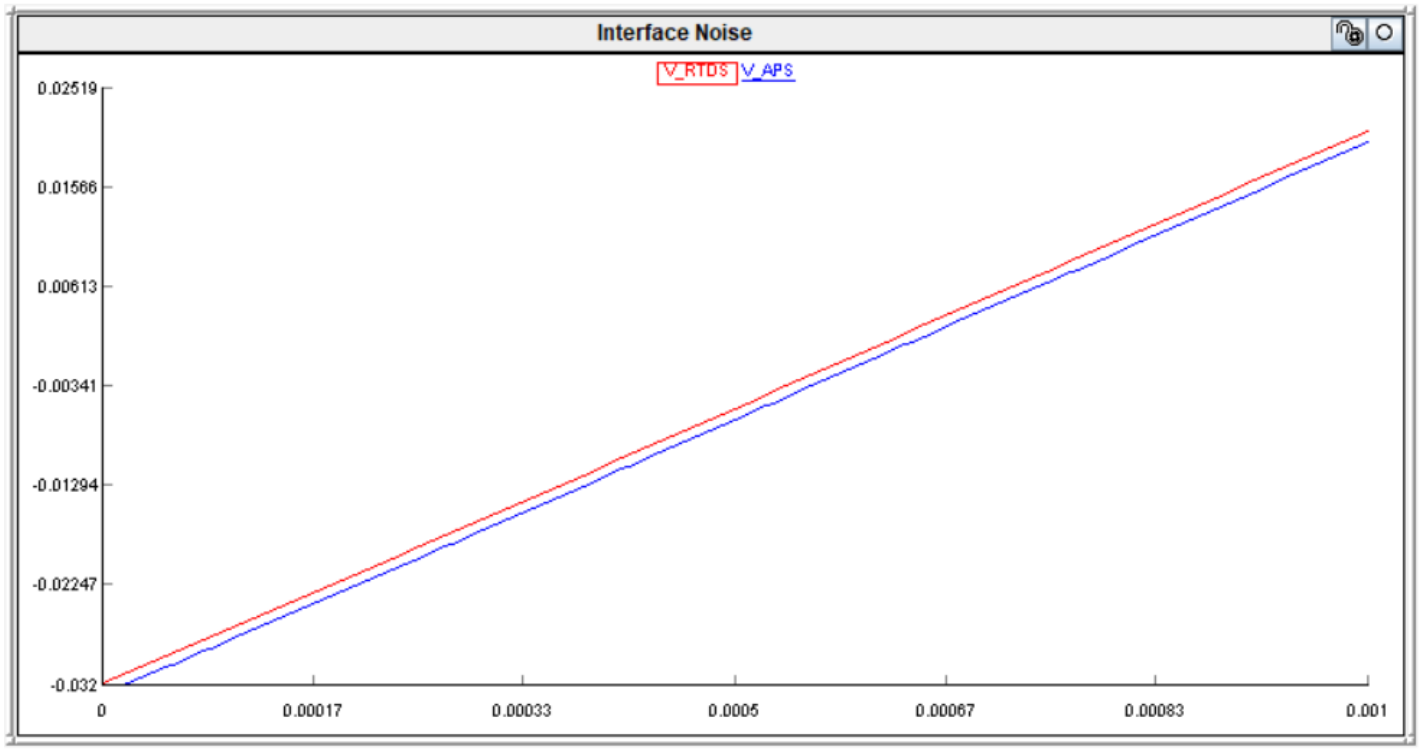


Figure 3-4 Voltage command and measurement waveforms (Zoomed in)

To better analyze the noise coming from the measurement within the APS1000, the control value voltage was held at constant value of 0.0 and the measured voltage was observed As shown in Figure 3-5, the noise of the output voltage measurements coming from APS1000 appear to have a voltage level of ~240mV peak to peak.

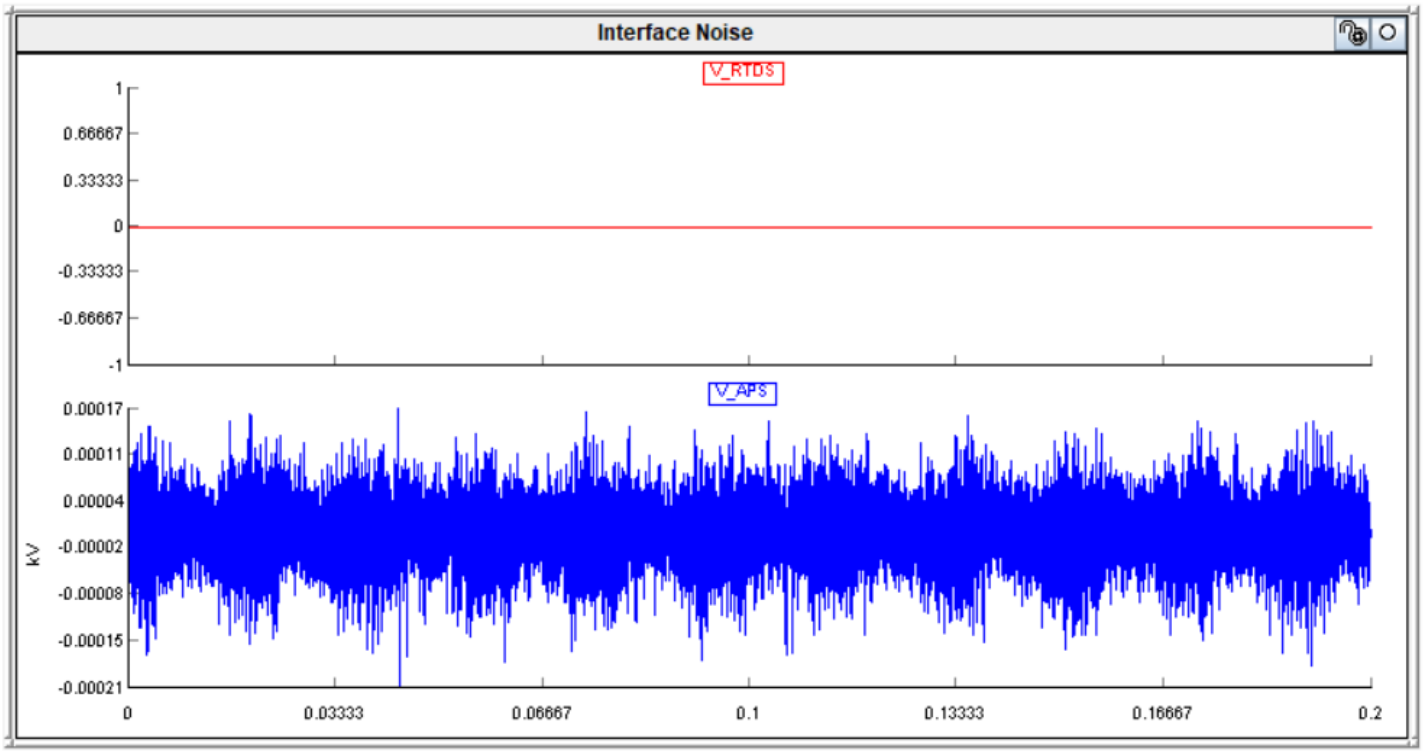


Figure 3-5 Interface noise for voltage measurement (Zoomed out)

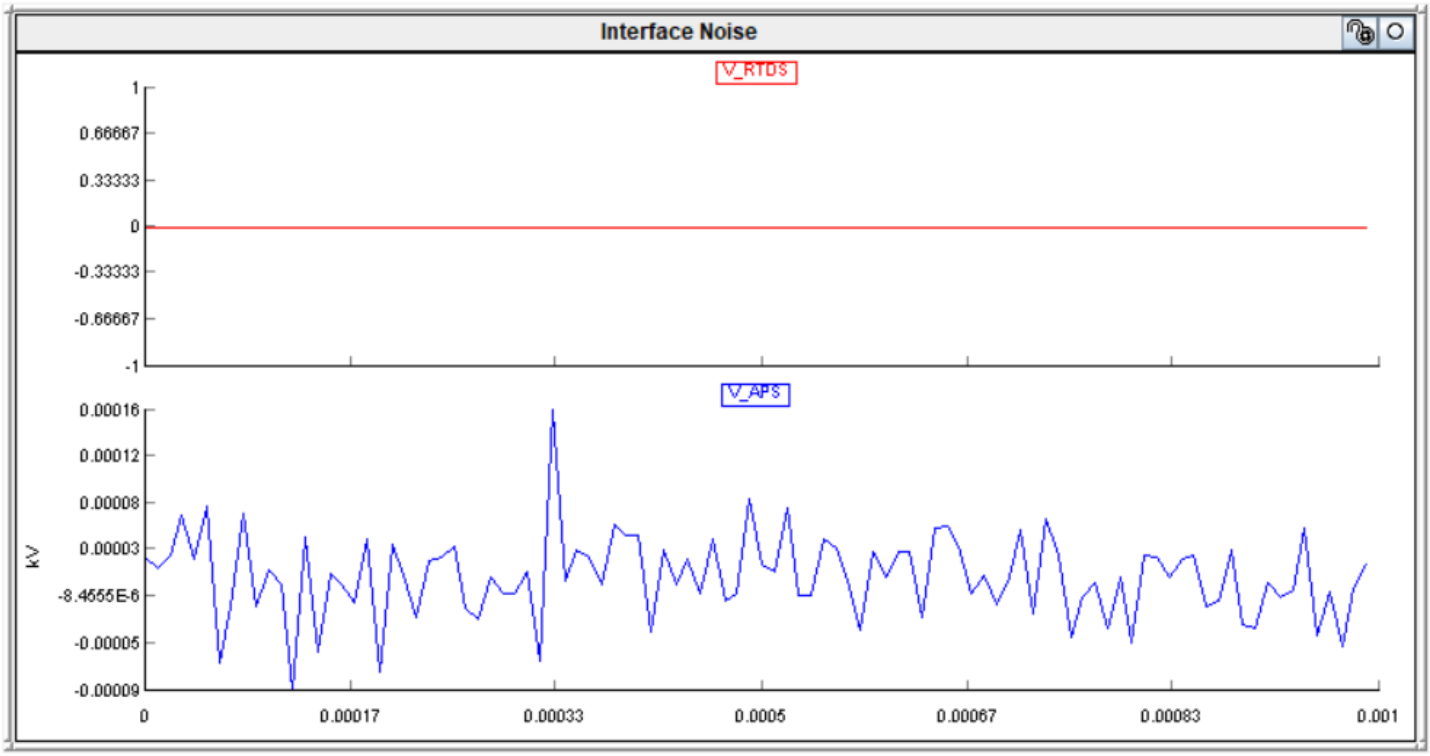


Figure 3-6 Interface noise for voltage measurement (Zoomed in)

As the measured signals of voltage and current from the amplifier's monitor channels will be sent back to the simulation, filtering techniques are required to reduce the high frequency interface noise to ensure accuracy and stability of the PHIL simulation. If necessary, a software filter could be implemented to further reduce the noise introduced by the PHIL interface, but may introduce additional attenuation and delay.

3.3 Stability and Time Delay

To investigate the stability and time delays associated with the PHIL interface, a simple voltage divider circuit is used. Figure 3-7 shows the PHIL interface of the voltage divider circuit using the ITM method. The load resistor R2 represents the hardware under test to be interfaced with the RTDS simulator, and is realized by connecting a 0.5kW, 110Vdc resistor bank was connected to the amplifier's output.

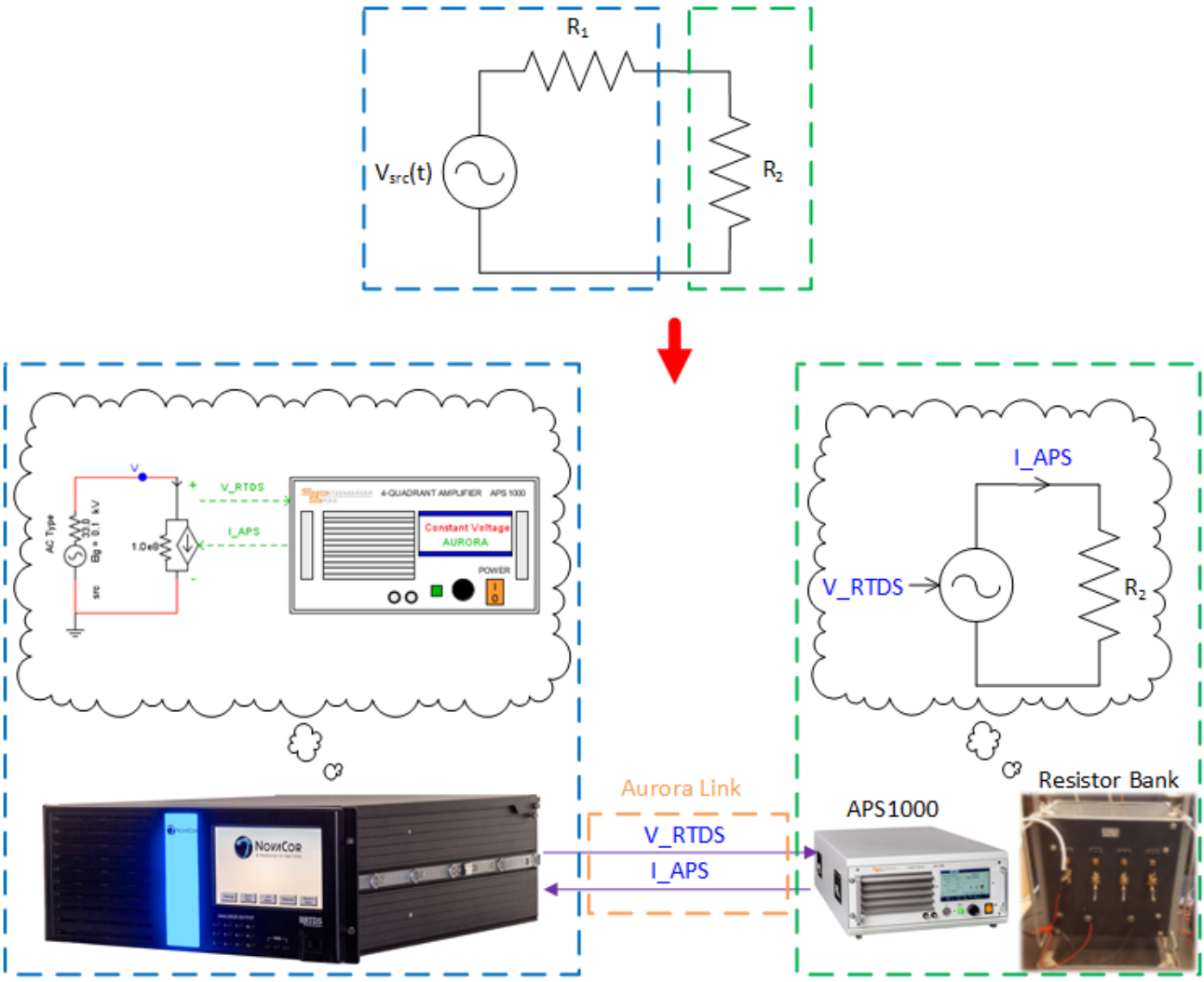


Figure 3-7 PHIL ITM interface for voltage divider circuit

3.3.1 Stability

Since the stability associated with the ITM method is closely related to the ratio of the simulated and physical impedances used, (i.e. R1/R2) three different test cases are investigated,

1. Case A: R1/R2 < 1 with stable simulation results
2. Case B: R1/R2 > 1 with stable simulation results
3. Case C: R1/R2 > 1 with unstable simulation results

Figure 3-8 & Figure 3-9 show the settings for the APS 1000 used in the following three test cases,

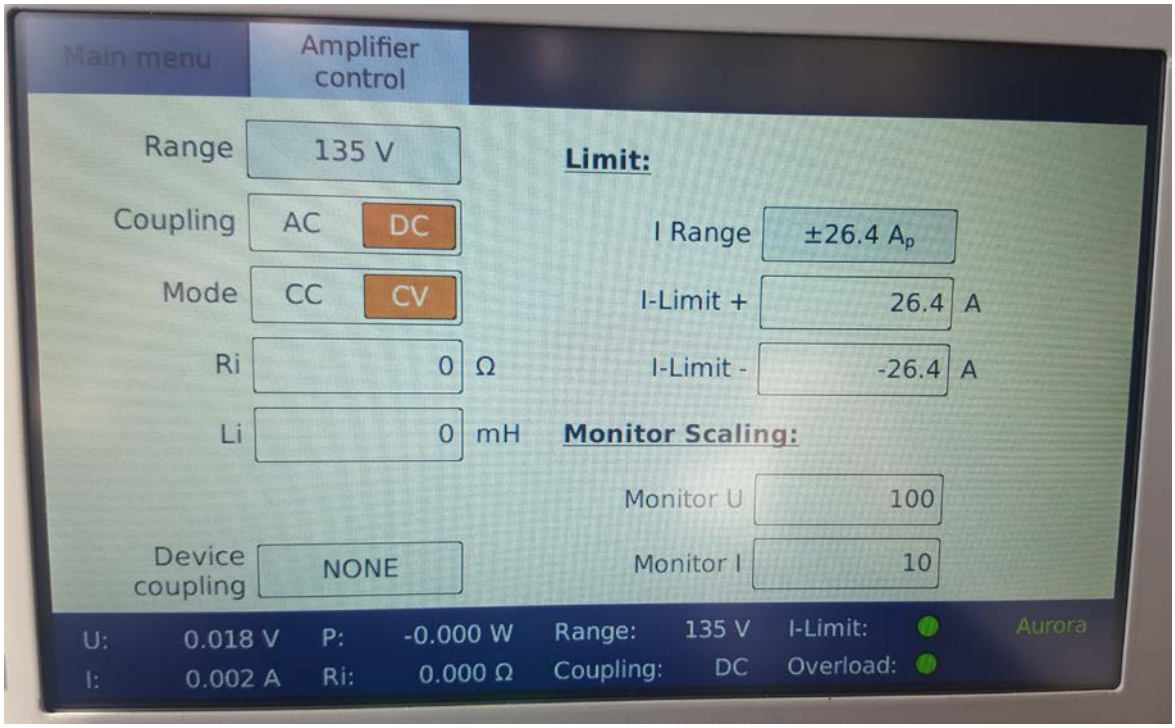


Figure 3-8 APS 1000 Amplifier Control settings

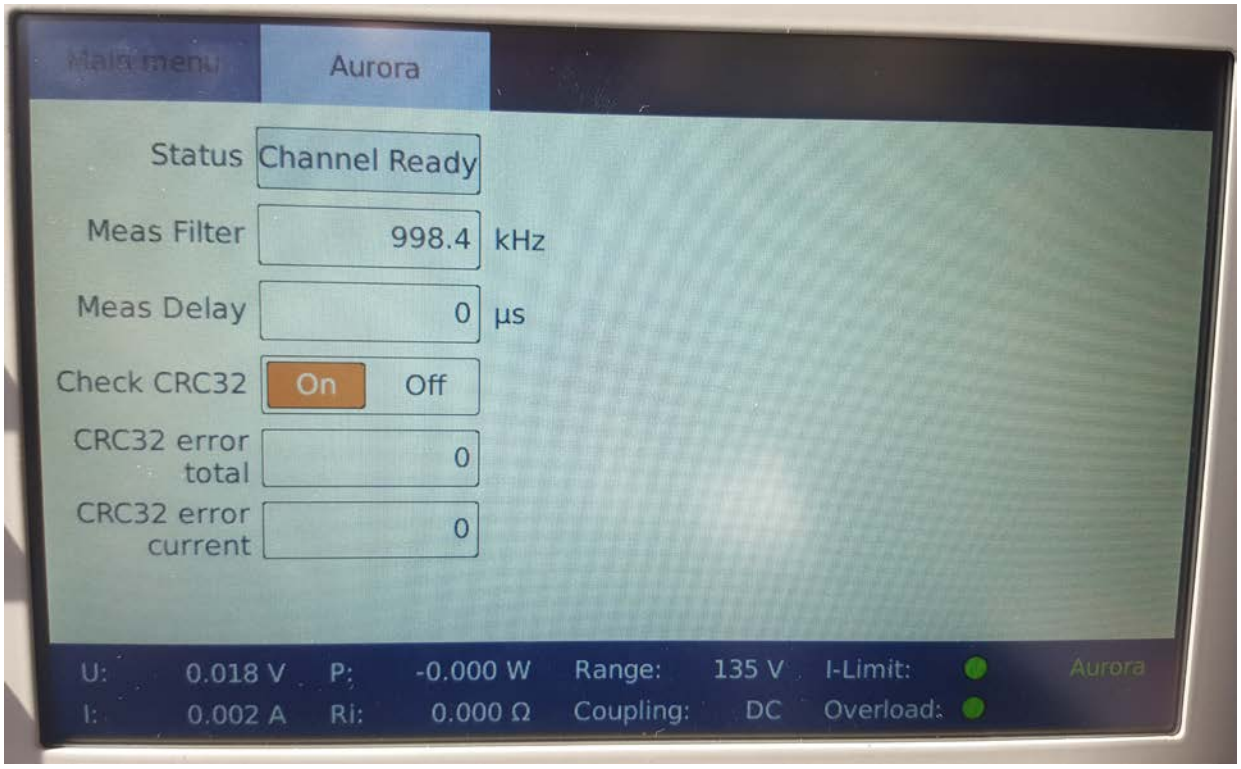


Figure 3-9 APS 1000 Aurora settings

PHIL Start up Procedure

In addition the individual test case descriptions shown below, the following start-up procedure was used in all three test cases,

1. Power up both the NovaCor and the APS 1000
2. After the boot sequence has completed, verify the status of the Aurora link.
    a. On the RTDS side, the status of the Aurora link can verified by inspecting the LED next to the transceiver on the back of the NovaCor chassis. If the LED is lit, then the link is valid.
    b. On the APS 1000 side, the user can navigate through the touch screen menus on the front display of the APS 1000 to check the link status. If the Aurora link is valid, then the "Status" on the Aurora tab should display "Channel Ready".
3. Configure the remainder of APS 1000 settings according to your specific application. (i.e. Coupling, Mode, Voltage/Current range etc.)
4. Configure the _rtds_AuroraSPS.def component according the amplifier settings from the previous step.
5. Compile the associated Draft case and proceed to Runtime.
6. Prior to starting the simulation on the RTDS, ensure that the feedback switch embedded within the SPS Aurora Link component is set to "Open Loop". With the feedback switch set to "Open Loop", a value of 0.0kA is applied to the current source on the simulation side of the PHIL interface, regardless of the actual measurement values returned by the amplifier.
7. Start the simulation case.
8. Verify that the simulation results are as expected when the feedback switch is set to "Open Loop".
9. Verify that the commanded value from the simulation matches the values shown on the front display of the APS 1000.
10. Using a digital multi meter, verify that the output voltage of the amplifier is as expected. This can be accomplished by,
    a. Setting the digital multimeter in the corresponding setting. (i.e. AC Voltage)
    b. Ensuring that the amplifier output is disabled.
    c. Connecting the output terminals of the amplifier to the corresponding input terminals of the digital multimeter.
    d. Enabling the amplifier output by pushing the Output On/Off button located on the front of the APS 1000.
    e. Verifying that the measurement shown on the digital multimeter is in good agreement with the values displayed on the front display of the APS 1000.
    f. Disabling the amplifier output by pushing the Output On/Off button located on the front of the APS 1000

11. With the amplifier output disabled, connect the output terminals of the amplifier to the terminals of the load resistor.
12. Enable the amplifier output and observe the voltage and current values on both the front display of the APS 1000 and on the plots within Runtime. The voltage and current values should be as expected and in good agreement with one another.
13. Set the feedback switch to "Closed Loop" to close the loop. Now the actual current measurements returned by the APS 1000 are being applied to the current source on the simulation side of the PHIL interface.
14. Observe the voltage and current values on both the front display of the APS 1000 and on the plots within Runtime RTDS simulation. The voltage and current values should be as expected and in good agreement with one another.

Next, a description of each of the individual test cases is provided including a brief summary of the simulation results.

Case A: R1/R2 < 1 with Stable Simulation Results

The circuit parameters used in this case are,

R1= 24.0 ohms, R2= 25.8 ohms, Vsource = 0.1kV-RMS, time step = 10usecs

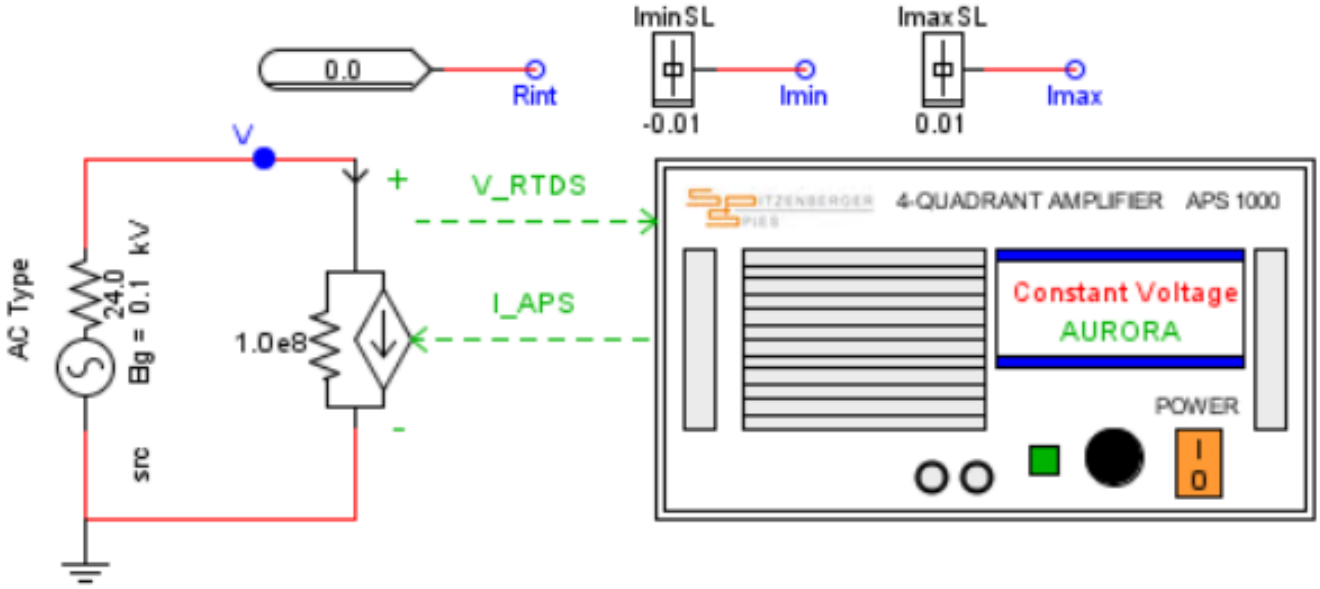


Figure 3-10 Case A: Draft canvas

Since the ratio of the simulated and hardware impedance is less than 1 (i.e. $\frac{R1}{R2} = \frac{24.0\Omega}{25.8\Omega} = 0.930 < 1$), the previous analysis predicts that the simulation results should remain stable. This is confirmed by observing the simulation results.

Figure 3-11 shows the simulation results when the loop is open, and Figure 3-12 &Figure 3-13 shows the simulation results when the loop is closed.

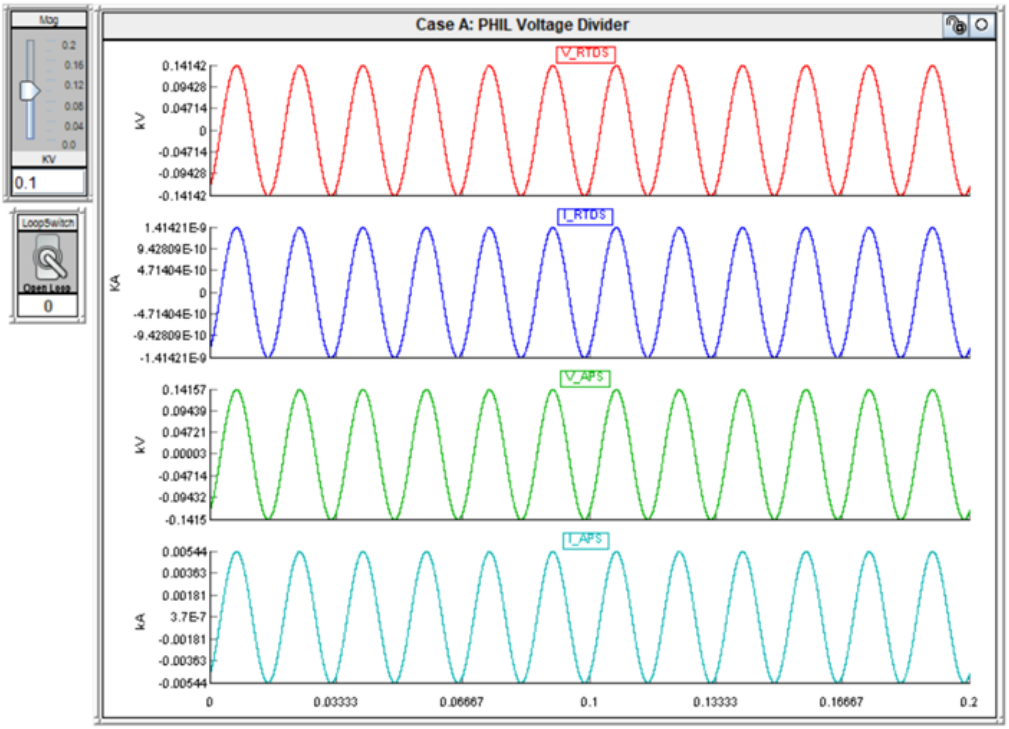


Figure 3-11 Case A: Open loop simulation results

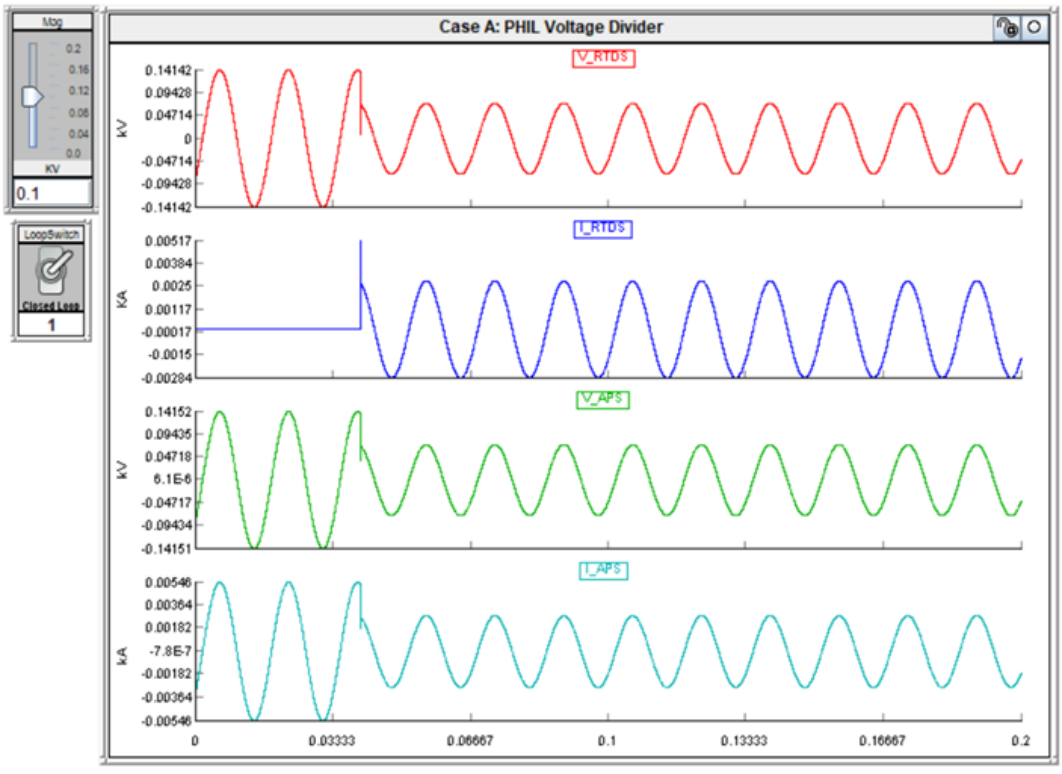


Figure 3-12 Case A: Transition from open to closed loop simulation results

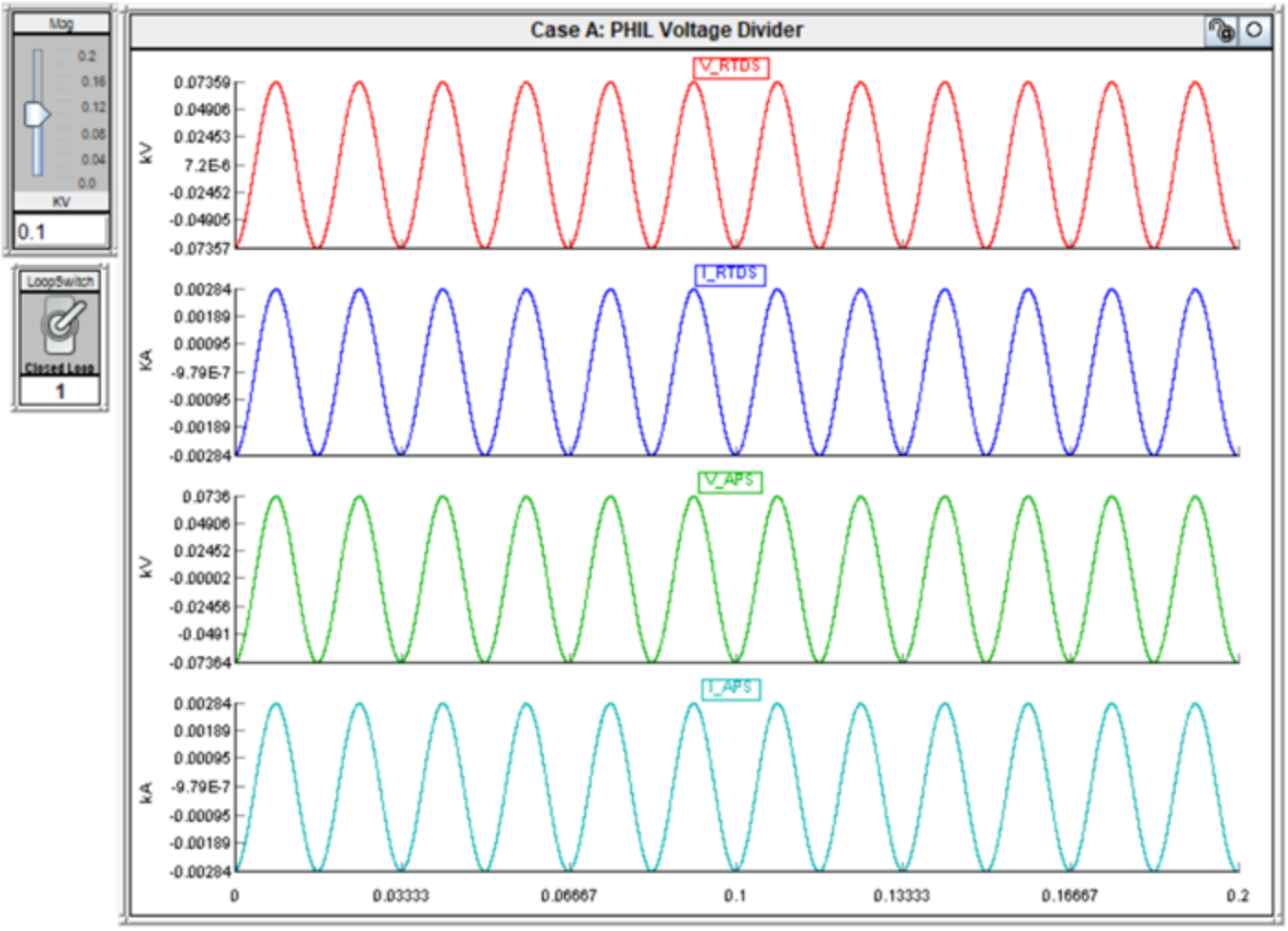


Figure 3-13 Case A: Closed loop simulation results

Case B: R1/R2 > 1 with Stable Simulation Results

The circuit parameters used in this case are,

R1= 51.6 ohms, R2= 25.8 ohms, Vsource = 0.1kV-RMS, time step = 10usecs

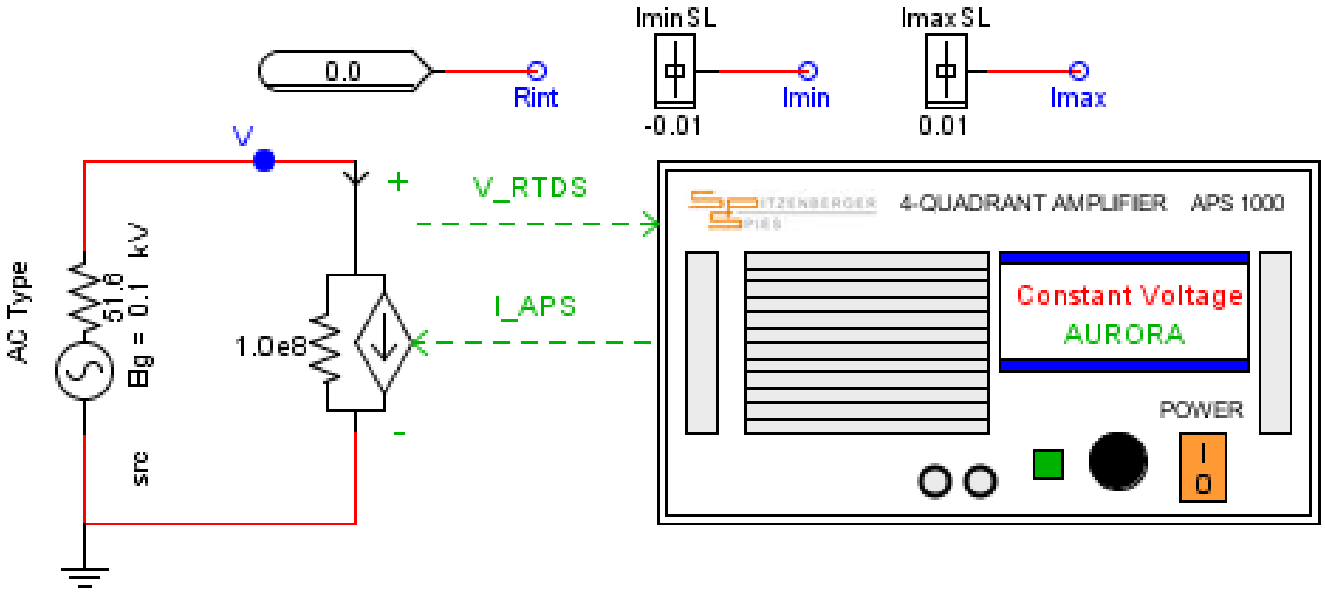


Figure 3-14 Case B: Draft canvas

Since the ratio of the simulated and hardware impedance is greater than 1 (i.e. $\frac{R1}{R2} = \frac{51.6\Omega}{25.8\Omega} = 2.0 > 1$), the previous analysis predicts that the simulation results should be unstable. This is refuted by observing the simulation results shown below.

Figure 3-15 shows the simulation results when the loop is open, and Figure 3-16 & Figure 3-17 shows the simulation results when the loop is closed.

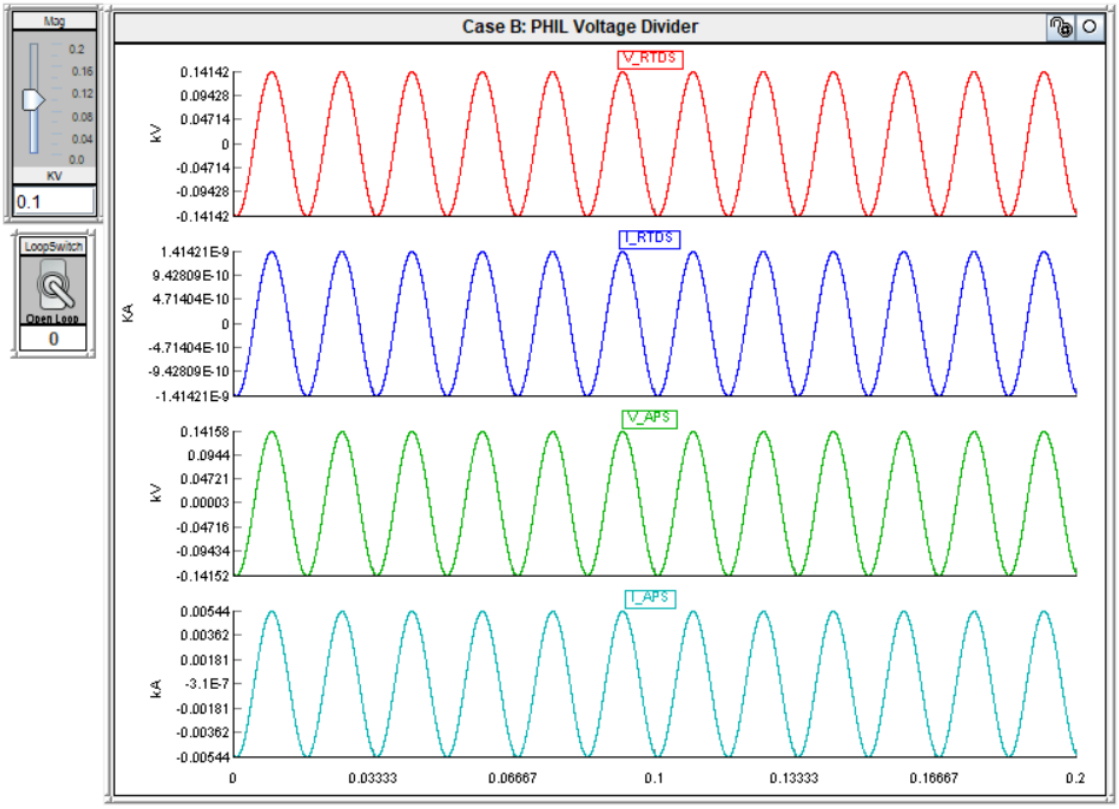


Figure 3-15 Case B: Open loop simulation results

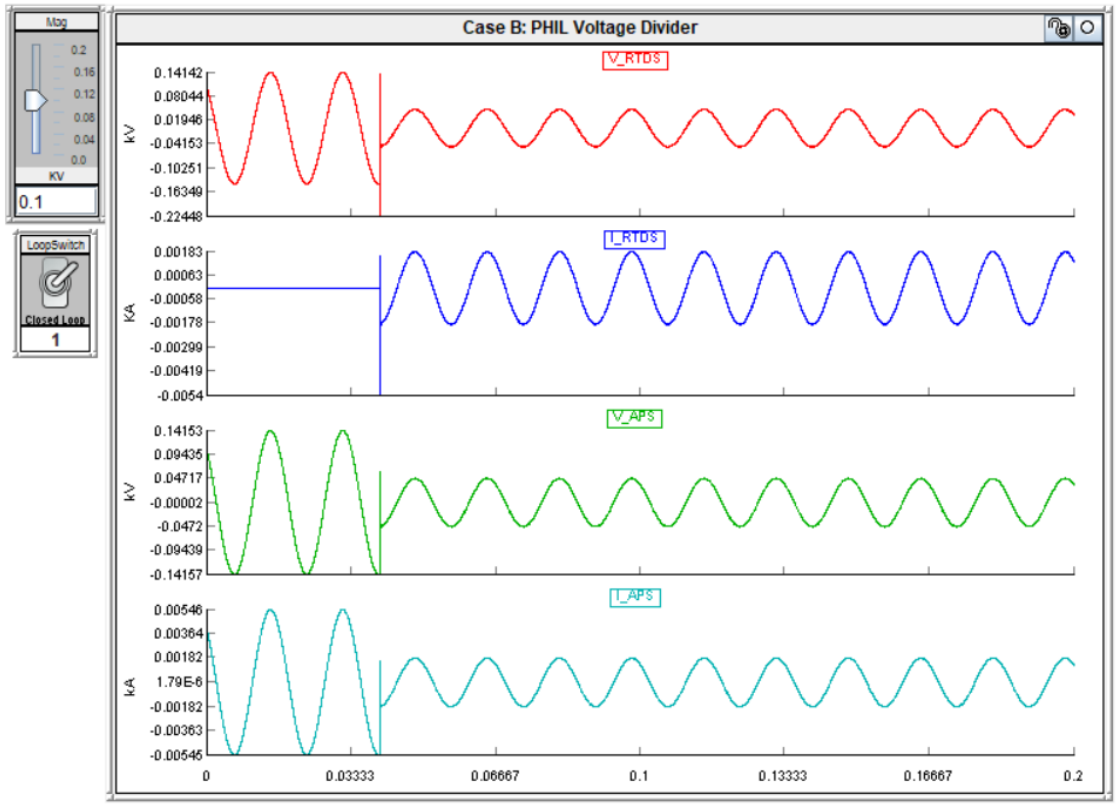


Figure 3-16 Case B: Transition from open to closed loop simulation results

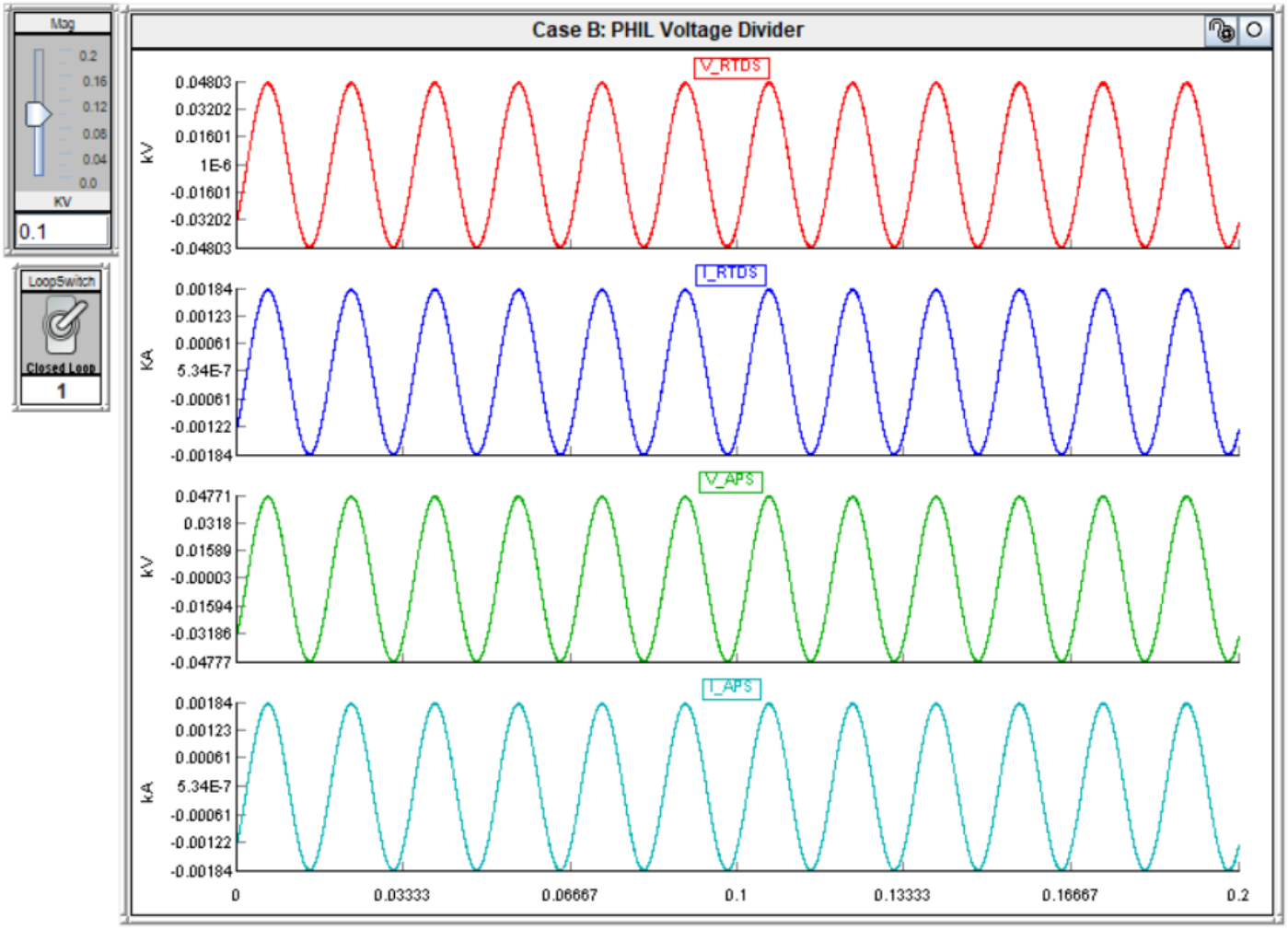


Figure 3-17 Case B: Closed loop simulation results

In next case, we will see that if we continue to increase the ratio of the simulated and hardware impedance, eventually the simulation results become unstable.

Case C: R1/R2 > 1 with Unstable Simulation Results

The circuit parameters used in this case are,

R1= 62 ohms, R2= 25.8 ohms, Vsource = 0.1kV-RMS, time step = 10usecs

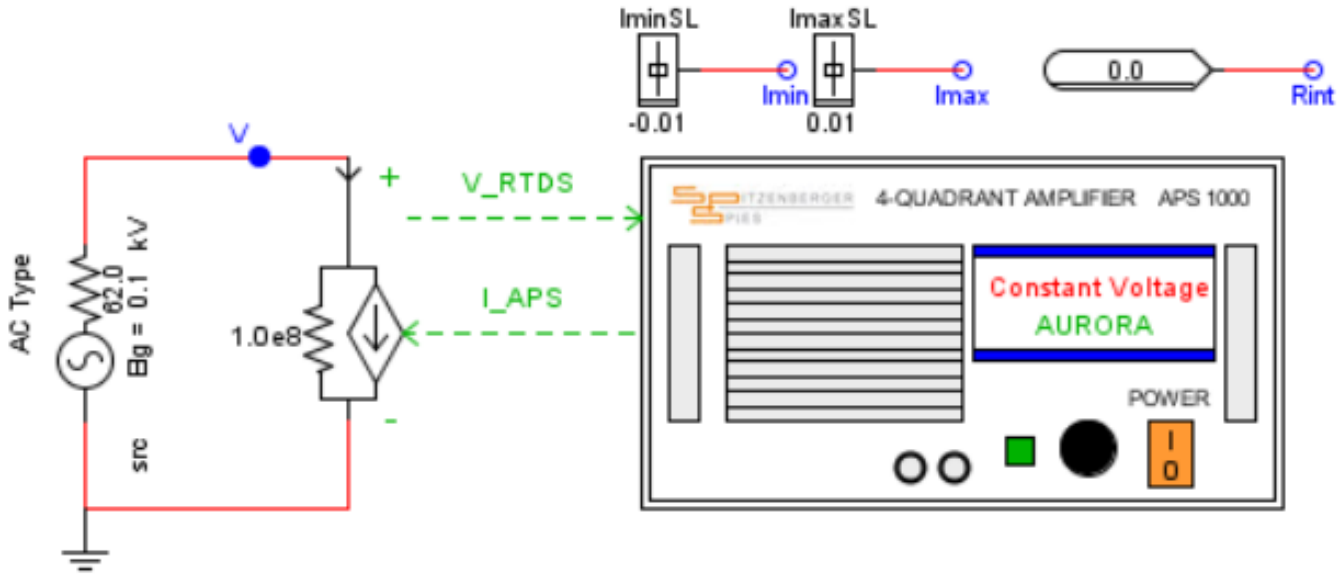


Figure 3-18 Case C: Draft canvas

Since the ratio of the simulated and hardware impedance is greater than 1 (i.e. $\frac{R1}{R2} = \frac{62.0\Omega}{25.8\Omega} = 2.403 > 1$), the previous analysis predicts that the simulation results should be unstable. This is confirmed by observing the simulation results shown below.

Figure 3-19 shows the simulation results when the loop is open, and Figure 3-20 shows the simulation results when the loop is closed.

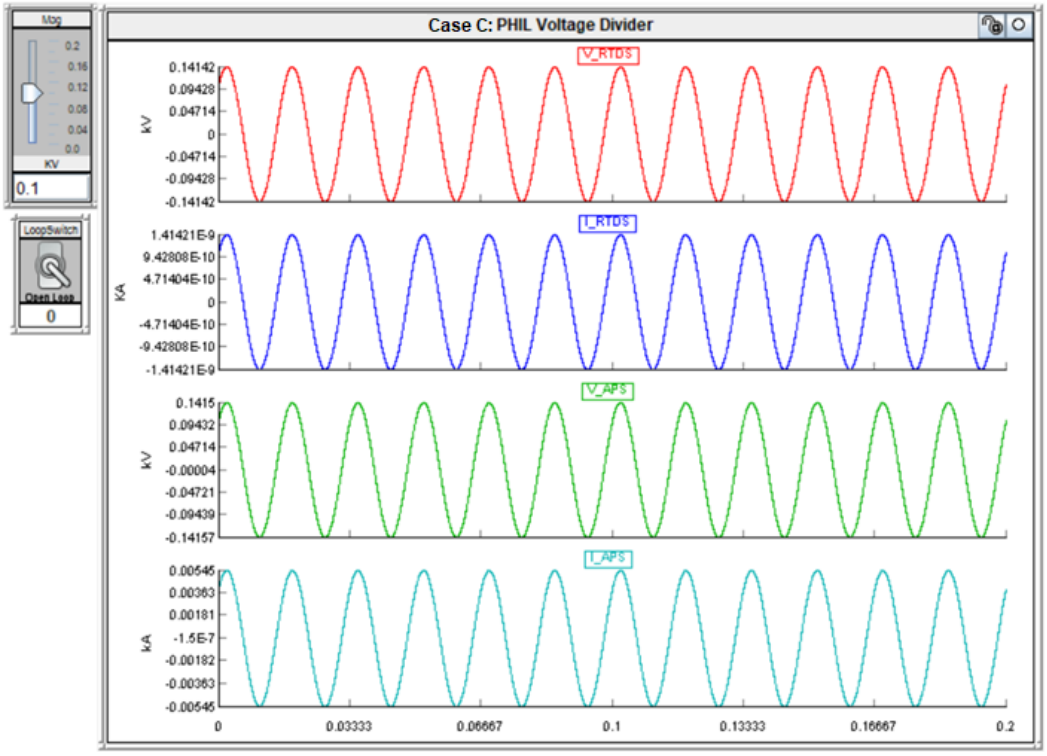


Figure 3-19 Case C: Open loop simulation results

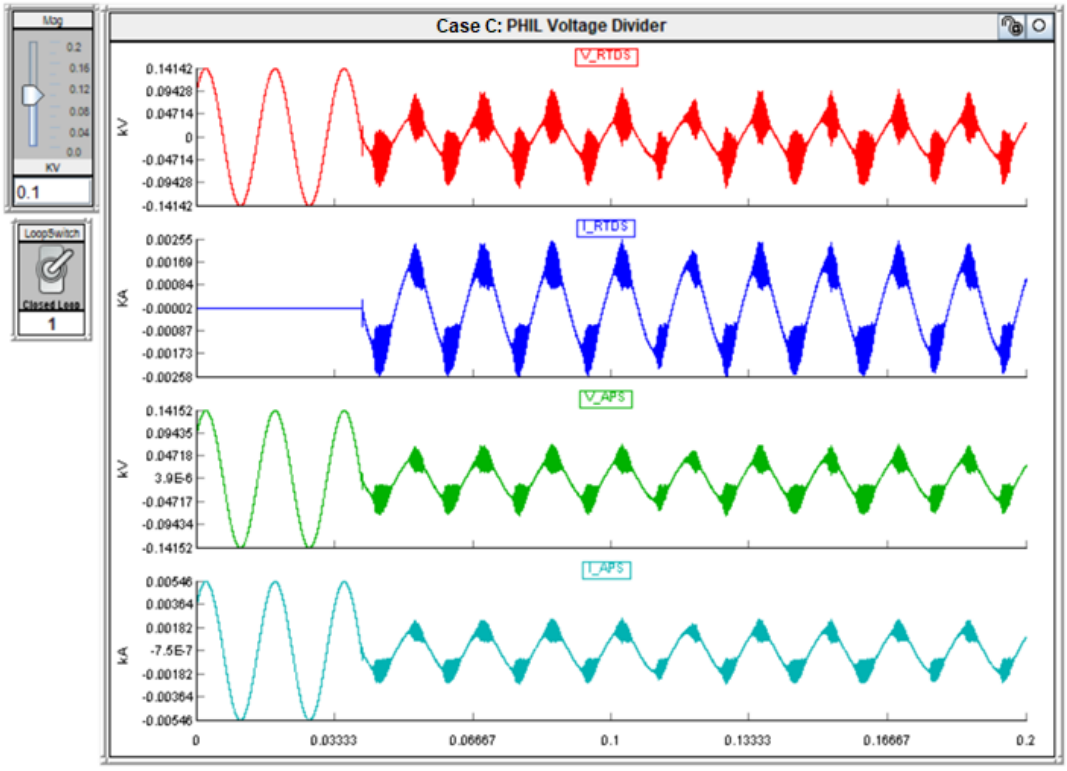


Figure 3-20 Case C: Transition from open to closed loop simulation results (unstable)

Next we will investigate the time delays associated with the interface.

3.3.2 Time Delay

The loop delay is measured as time elapsed from moment when the voltage 'V_RTDS' voltage is sent out to when the current 'I_APS' is applied to the circuit.

The loop delay can be broken down into two individual components, one component caused by the APS1000 and the other caused by the RTDS.

$$\tau_{Loop} = \tau_{APS} + \tau_{RTDS} \tag{3.1}$$

The delay related to APS1000, τ_{APS}, is amount of time elapsed between when the amplifier receives the control command, and when it returns the corresponding voltage and current measurements. This delay can be greatly influenced by a user defined measurement delay setting which can be configured within the settings menu of the amplifier. For our purposes, this measurement delay setting is configured to use the minimum value of $0.0\mu s$. In reality, this measurement delay cannot be $0.0\mu s$ as it takes some definite amount of time for the amplifier to receive and transmit the data across the digital link. As such, this component of the loop delay is going to depend on the user defined measurement delay setting and other device specific characteristics related to the amplifier.

The remaining portion of loop delay (i.e. τ_{RTDS}) is due to the computation and communication intervals that occur within a given time step on the RTDS. This portion of the loop delay will vary based on the specific details of the simulation case being simulated and how the available hardware is being utilized. In general, all that can be said with regards to this portion of the loop delay is that it will be less than one simulation time-step in duration.

$$\tau_{RTDS} < \Delta t \tag{3.2}$$

Therefore the worst case scenario for the total loop delay is,

$$\tau_{Loop} = \tau_{APS} + \tau_{RTDS} < \tau_{APS} + \Delta t \tag{3.3}$$

3.3.3 PHIL Interface using the small time step bridge box

In addition to the PHIL in the large time step environment, it is also possible to preform PHIL from within the small time step environment. Just like in the large time step environment, an Aurora link

is established between the RTDS and the APS1000 to facilitate data exchange between the two devices.

To illustrate this, one of the previous voltage divider cases will be simulated within the small time step environment.

Case A: R1/R2 < 1 with Stable Simulation Results

The circuit parameters used in this case are,

R1= 24.0 ohms, R2= 25.8 ohms, Vsource = 0.1kV-RMS, time step = 1.52usecs

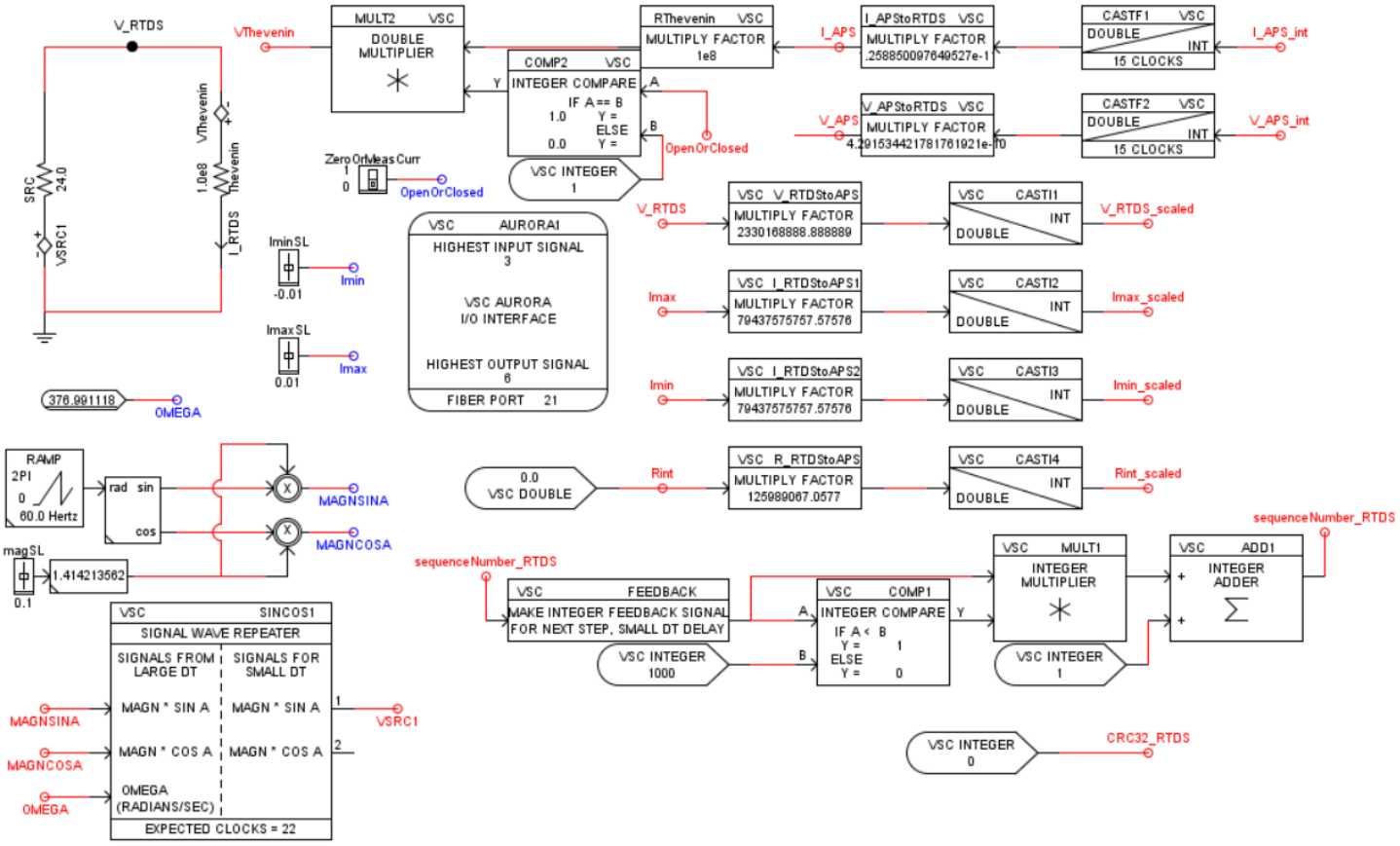


Figure 3-21 Case A: Draft canvas within VSC Bridge Box

Again, since the ratio of the simulated and hardware impedance is less than 1 (i.e. $\frac{R1}{R2} = \frac{24.0\Omega}{25.8\Omega} = 0.930 < 1$), the previous analysis predicts that the simulation results should remain stable. This is confirmed by observing the simulation results shown below.

Figure 3-22 shows the simulation results when the loop is open, and Figure 3-23 & Figure 3-24 shows the simulation results when the loop is closed.

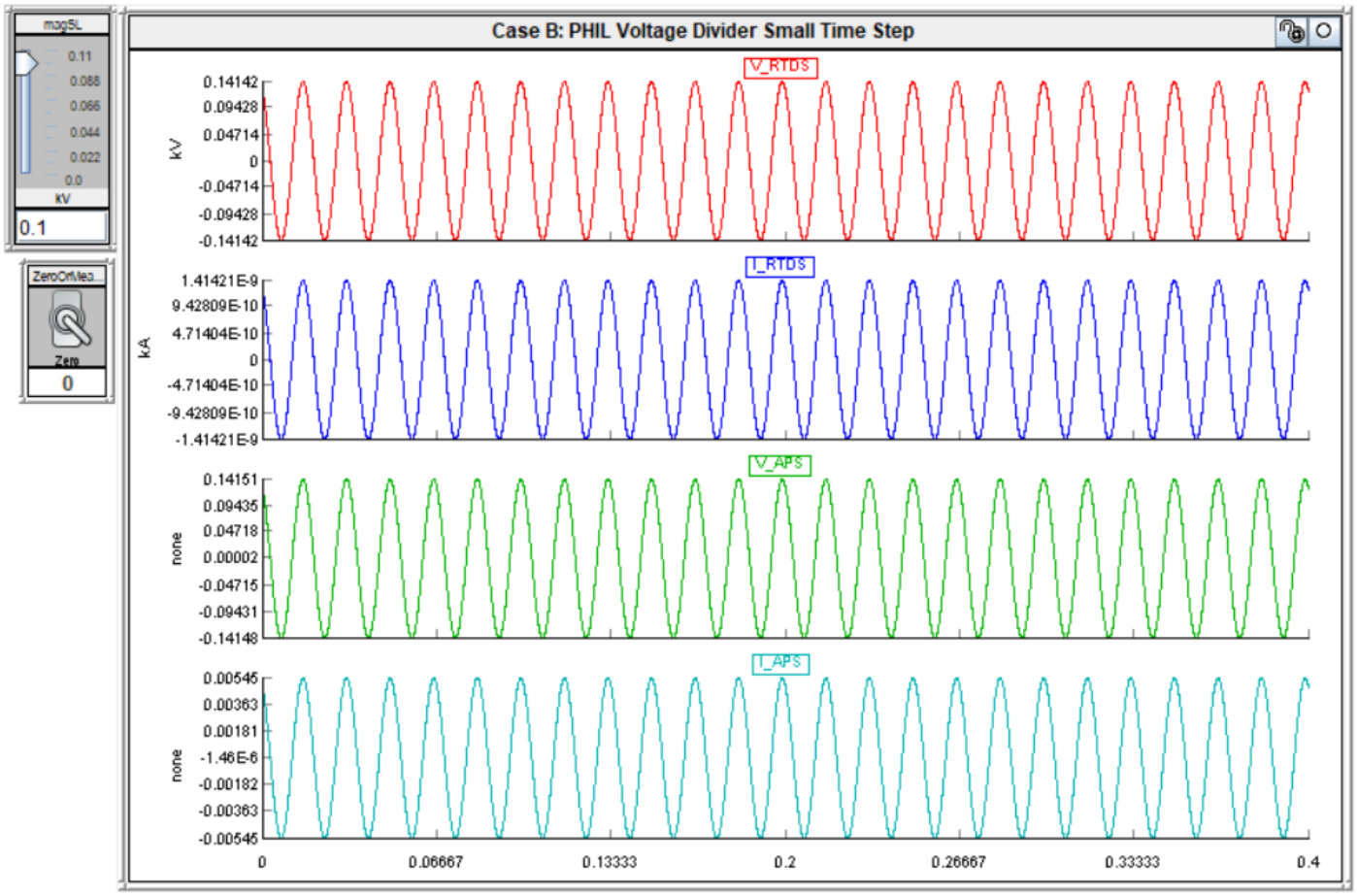


Figure 3-22 Case A: Open loop simulation results (Small Δt)

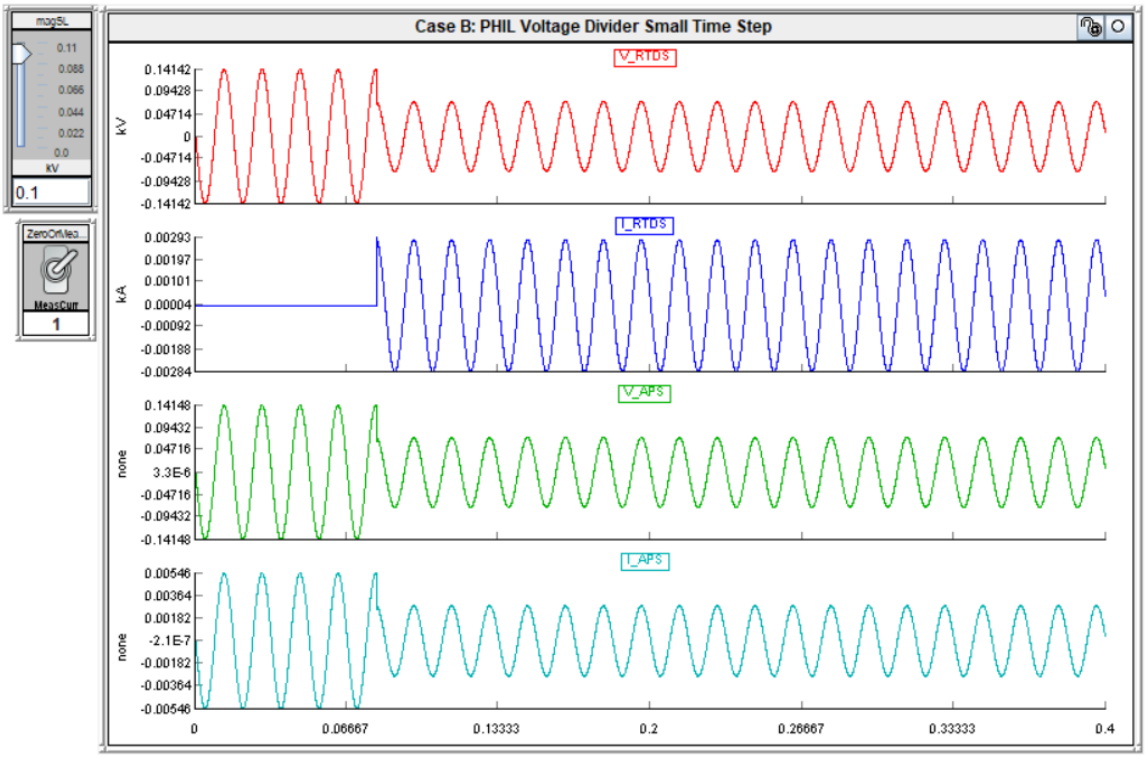


Figure 3-23 Case A: Transition from open to closed loop simulation results (Small Δt)

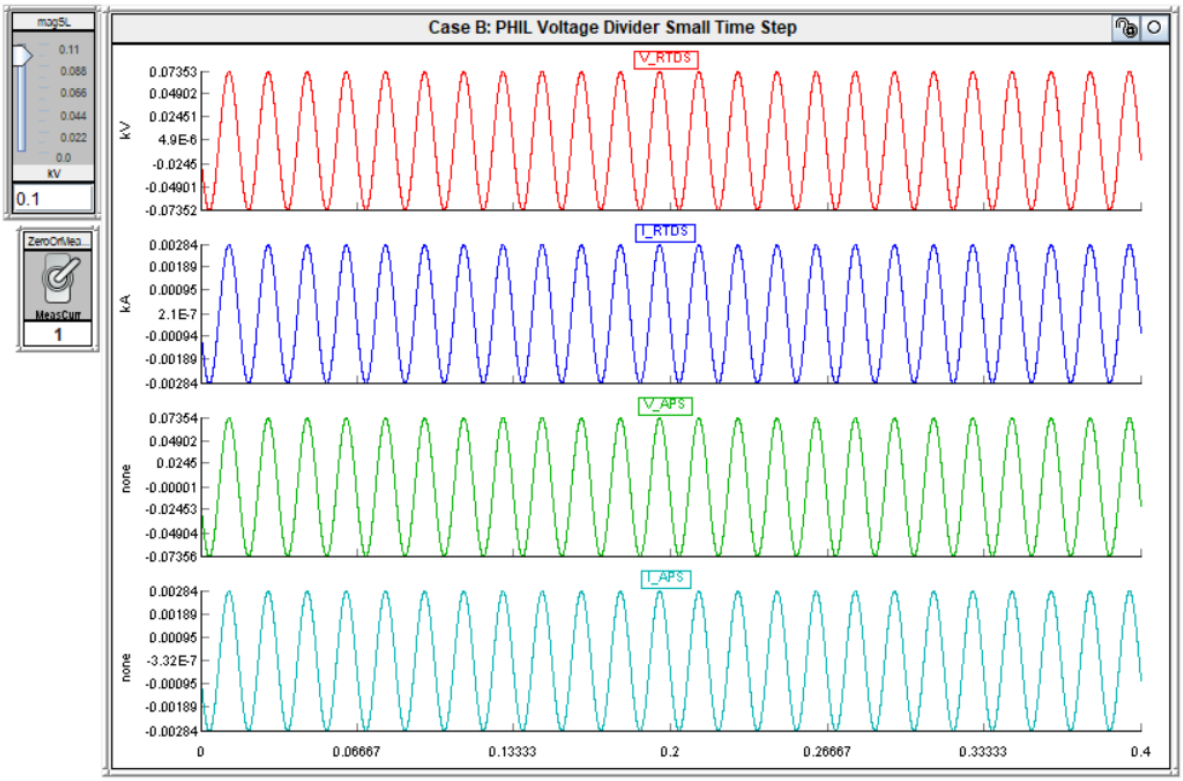


Figure 3-24 Case A: Closed loop simulation results (Small Δt)

a

4 PHIL Interface with a PV Micro inverter

A test setup of a PHIL interface with a PV inverter and the SPS amplifier is shown in Figure 4-1. The DC side of the inverter is connected to a solar panel. The AC side of the inverter is connected to the amplifier output terminal which provides the grid simulation at 240Vrms, 60Hz. The inverter current measured by the amplifier is sent back to the simulated grid in the RTDS.

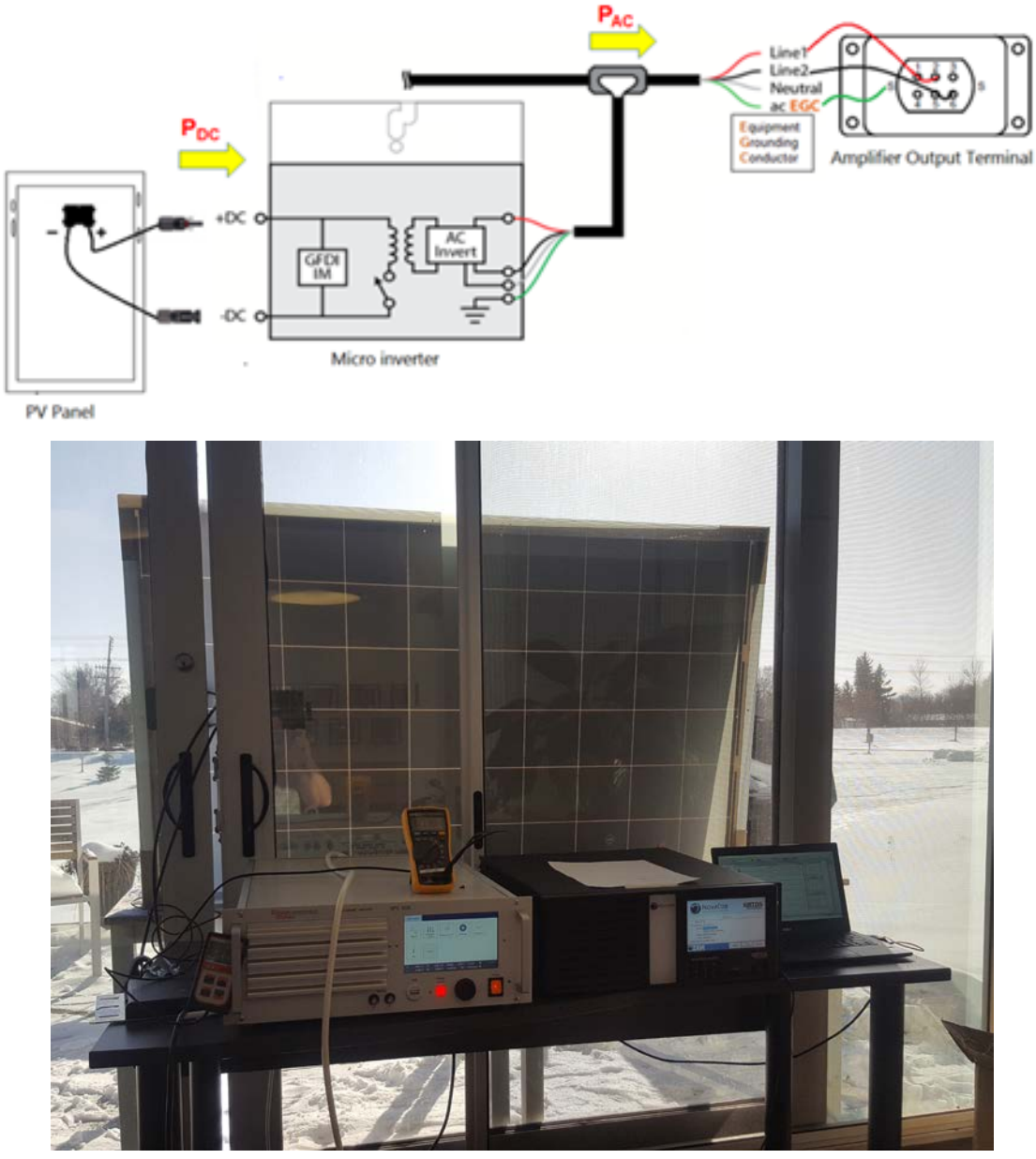


Figure 4-1 PHIL interface with PV inverter

The settings for the APS 1000 are shown below in Figures Figure 4-2 & Figure 4-3.

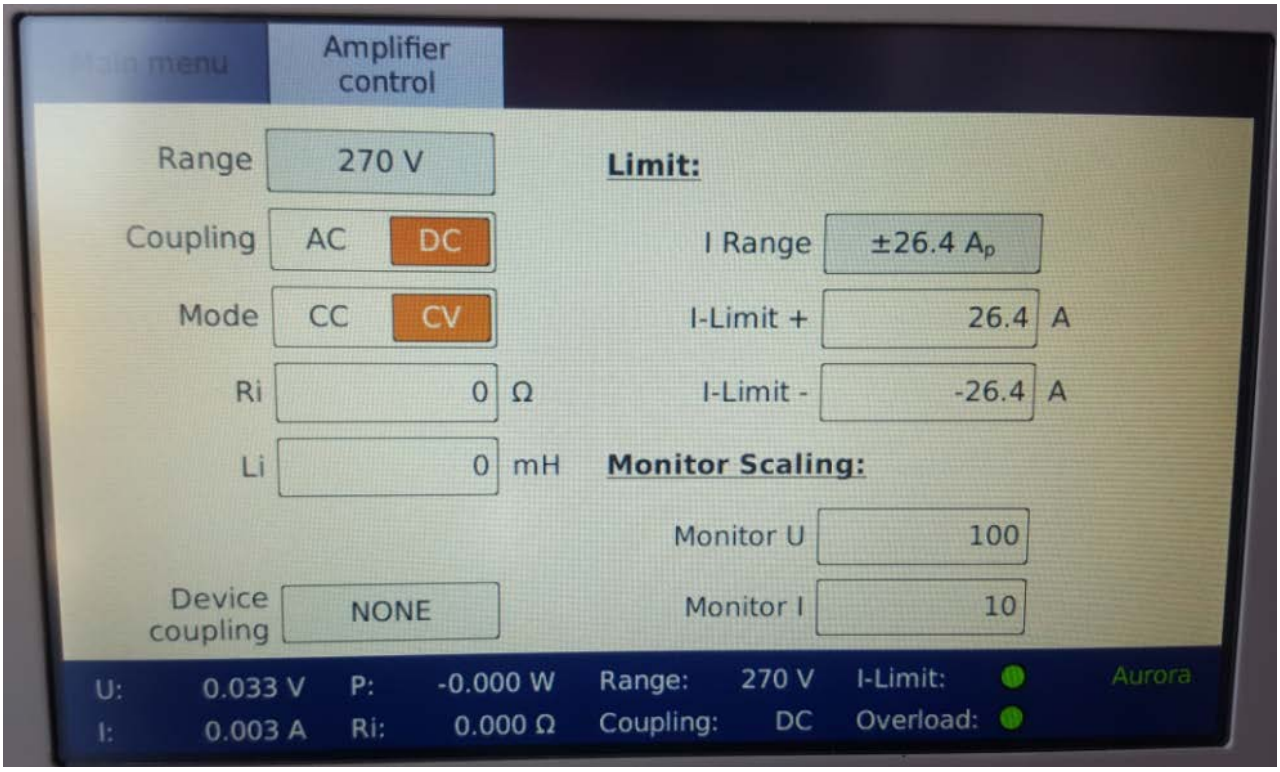


Figure 4-2 APS 1000 Amplifier Control settings

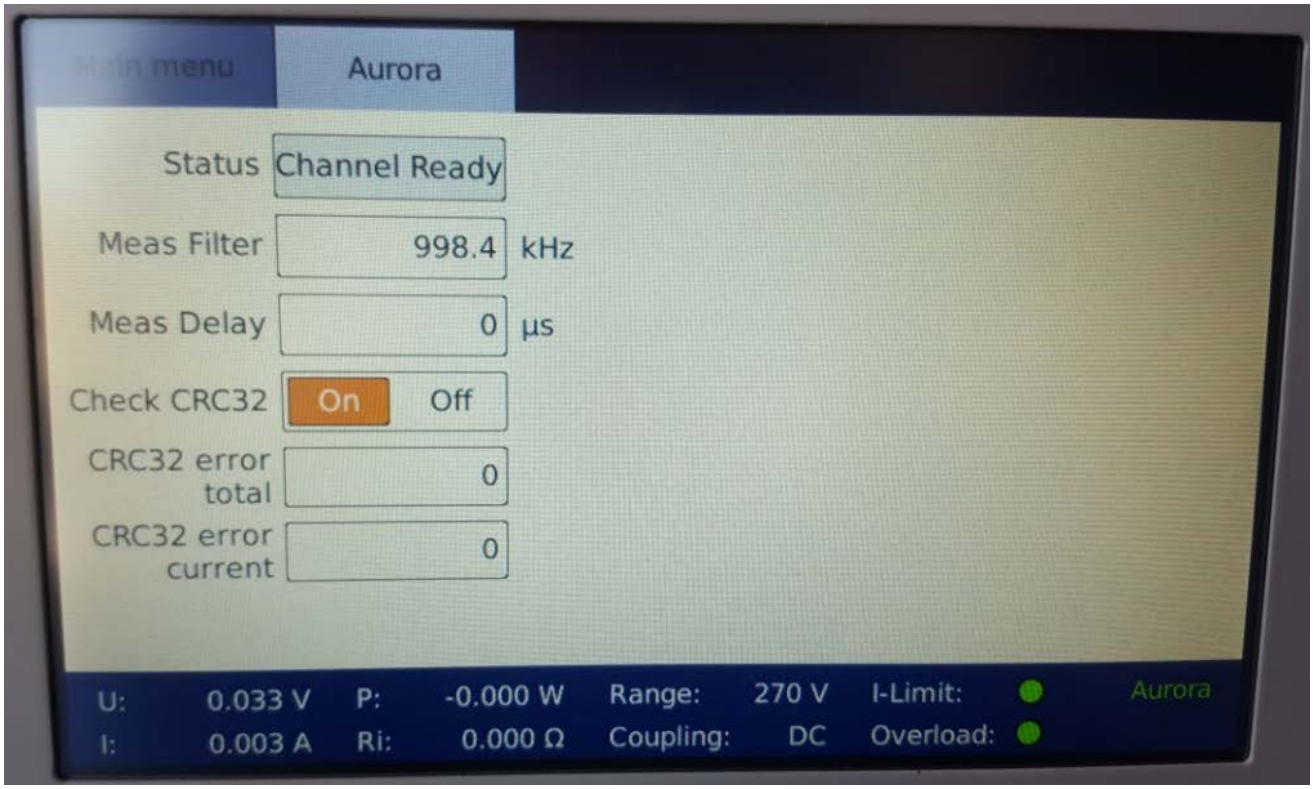


Figure 4-3 APS 1000 Aurora settings

The inverter has a 5 minute start up period from the moment in which the AC voltage must be maintained at AC side of the inverter. Figure 4-4 shows a plot of the voltages and currents prior to inverter start up. Figure 4-5 shows the front display of the SPS amplifier during this peroid.

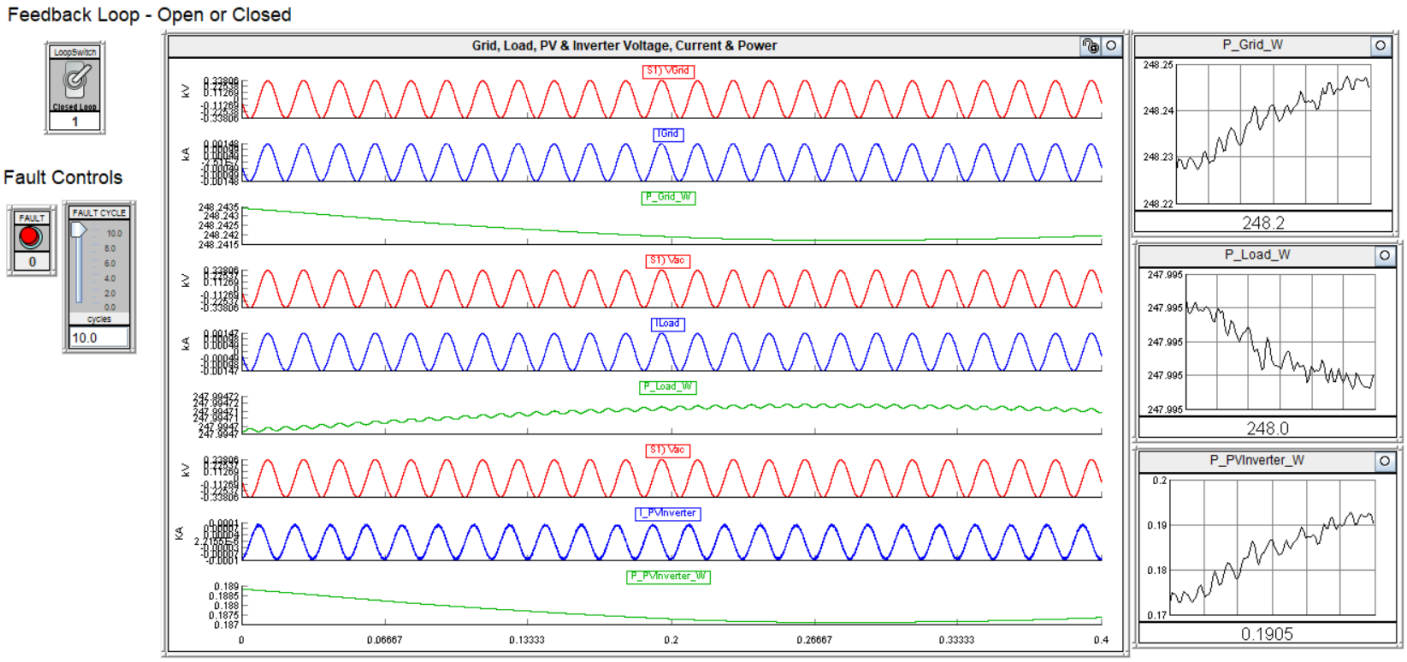


Figure 4-4 Grid, Load, PV and Inverter Voltage, Current & Power (Prior to Inverter Start-up)

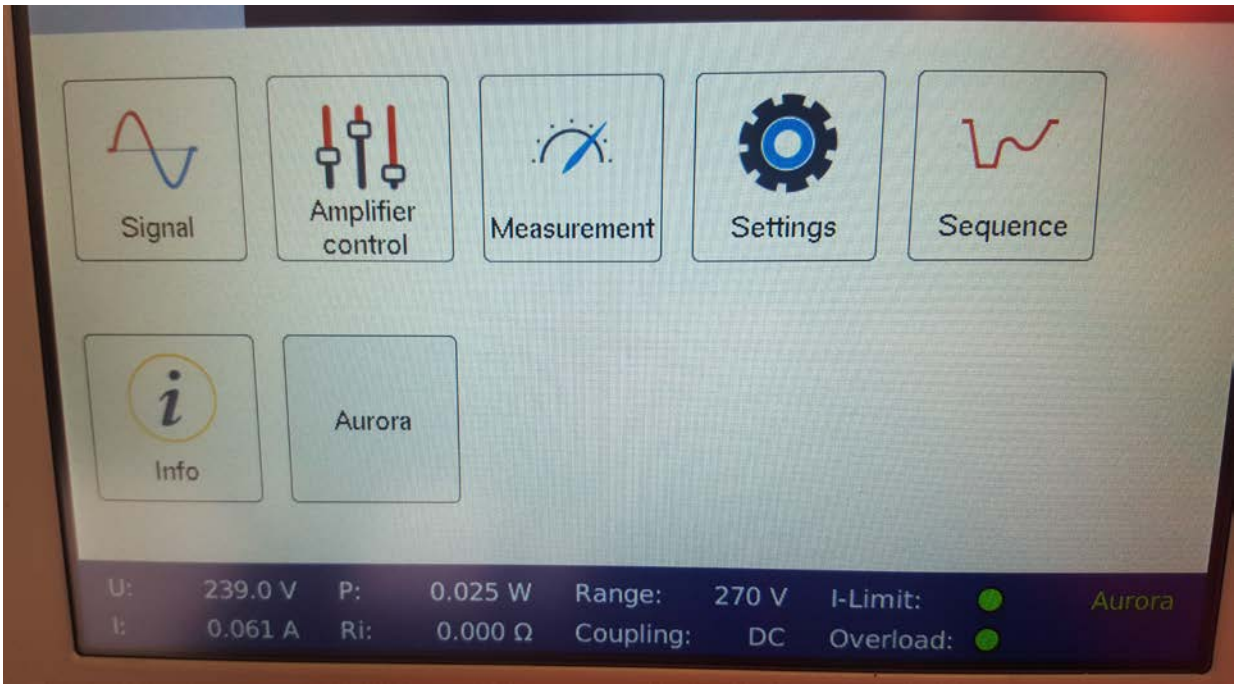


Figure 4-5 Front Display APS 1000 (Prior to Inverter Start-up)

Next, Figure 4-6 shows the voltages and currents after the inverter start up. Figure 4-7 shows the front display of the SPS amplifier during this peroid.

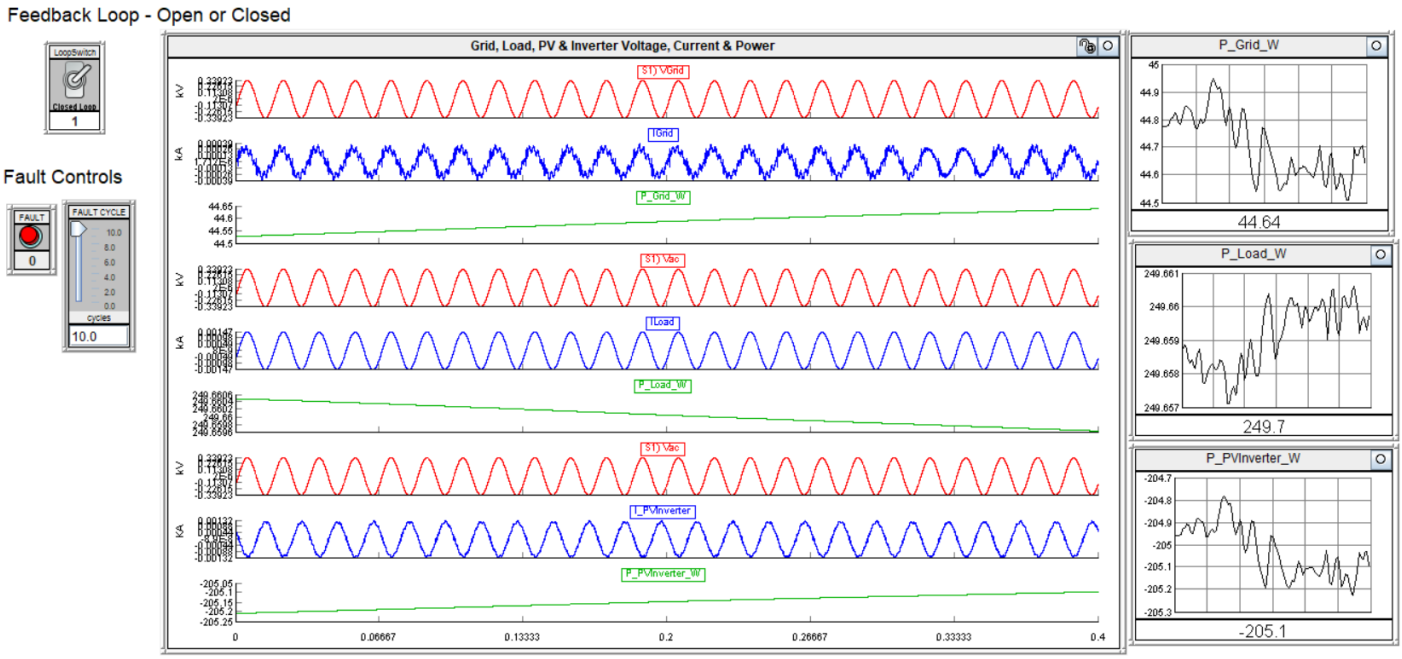


Figure 4-6 Grid, Load, PV and Inverter Voltage, Current & Power (After Inverter Start-up)

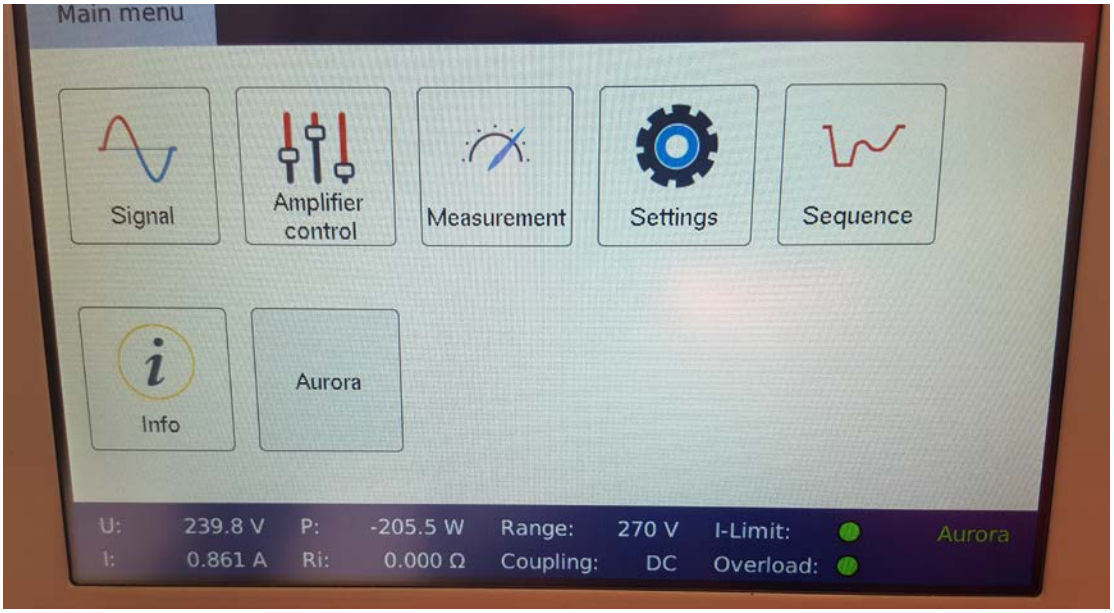


Figure 4-7 Front Display APS 1000 (After Inverter Start-up)

Figure 4-8 shows the inverter response to a line to ground fault simulated in the RTDS. The current response shows that the inverter disconnects from the grid after a fault with a 5 cycle duration was applied. It should be noted that the contingency scenarios to be tested in the PHIL interface should

be well within the protection limits of the device under test as well as the amplifier ratings to prevent unstable operation.

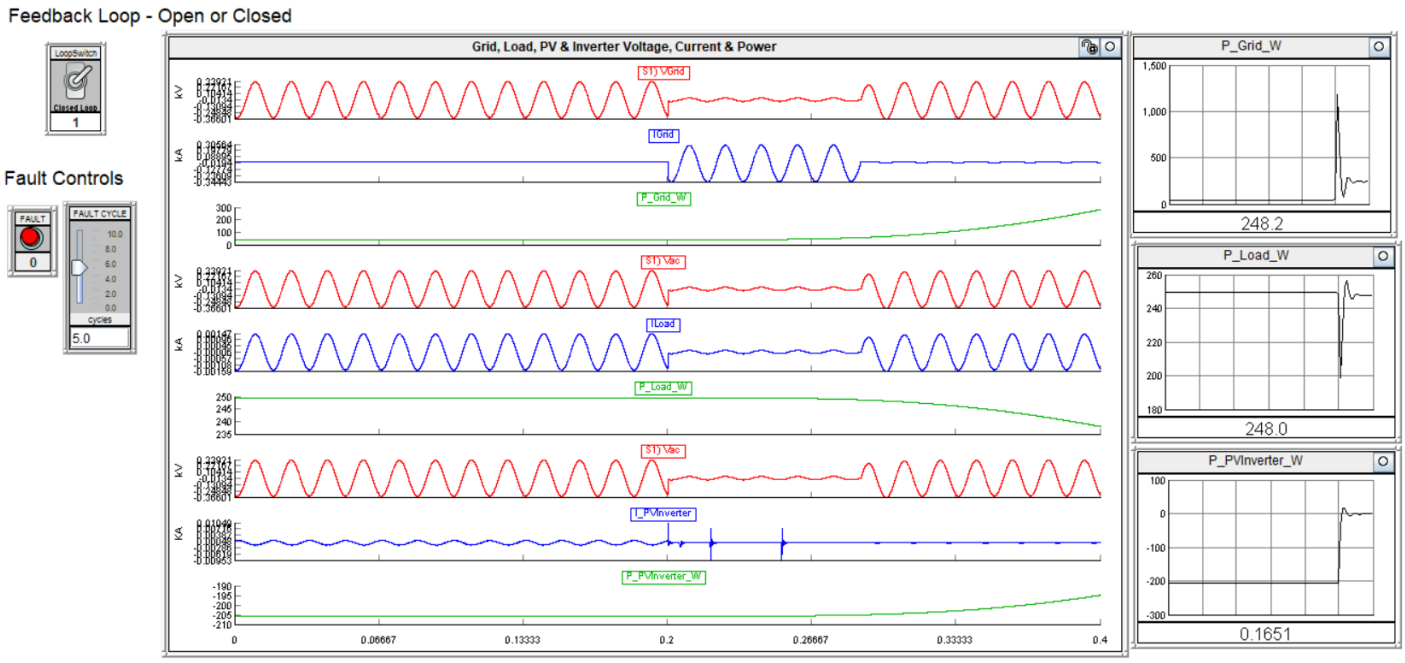


Figure 4-8 Grid, Load, PV and Inverter Voltage, Current & Power (5 Cycle LG Fault)

5 References

[1] X. Wang, W. J. Giesbrecht, R. Kuffel, D. Woodford, L. Arendt and R. P. Wierckx, "Enhanced Performance of a Conventional HVDC Analogue Simulator with a Real-Time Digital Simulator," in *Proceedings of the 11th Power Systems Computation Conference*, Avignon, France, 1993.

[2] R. Kuffel, R. P. Wierckx, P. Forsyth, H. Duchen, M. Lagerkvist, P. Holmberg and X. Wang, "Expanding an Analogue HVDC Simulator's Modelling Capability Using a Real-Time Digital Simulator (RTDS)," in *International Conference on Digital Power System Simulators (ICDS'95)*, College Station, 1995.

[3] H. Dommel, "Digital Computer Solution of Electromagnetic Transients in Single and Multiphase Networks," *IEEE Transactions on Power Apparatus and Systems,* Vols. PAS-88, no. 4, April 1969.

[4] W. Ren, M. Steurer and T. Baldwin, "Improve the Stability and the Accuracy of Power Hardware-in-the-Loop Simulation by Selecting Appropriate Interface Algorithms," *IEEE Transactions on Industry Applications,* vol. 44, no. 4, pp. 1286-1294, 23 July 2008.

[5] I. D. Yoo and A. Gole, "Compensating for Interface Equipment Limitations to Improve Simulation Accuracy of Real-Time Power Hardware In Loop Simulation," *IEEE Transactions on Power Delivery,* vol. 27, no. 3, pp. 1284-1291, July 2012.

[6] G. L. P. K. N. H. P. C. a. A. R. F. Lehfuss, "Comparison of multiple power amplification types for power Hardware-in-the-Loop applications," *2012 Complexity in Engineering (COMPENG). Proceedings,* pp. 1-6, June 2012.