Predicting Switch ON/OFF Statuses in Real Time Electromagnetic Transients Simulations with Voltage Source Converters

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***Abstract*—Power converters in system-level real-time simulations are usually emulated by using an L/C associated discrete circuit (L/C-ADC) in a fixed time-step simulation. However, there are several potential inaccuracies in L/C-ADC based simulation results: unrealistically high virtual loss especially at high PWM frequencies, fictitious current oscillations between the L and C represented devices, and limitations in the impedance ratio between OFF and ON switch representations. Therefore, there are potential benefits from using switched-resistance representations of electronic switch devices. Fortunately, such simulation has recently become feasible due to the higher performance of newer computer processor cores. However, the switched-resistance representation of switches requires reliable prediction of the ON/OFF statuses of the switch devices before each simulation time-step. This paper describes a method for highly reliable prediction of ON/OFF switch statuses for voltage source converters with switched-resistance switch representations in fixed time-step simulation. Real-time simulation results are presented for systems containing 2-level and 3-level voltage source converters. The technique could be practised in non-real-time simulation for much more complicated converters.**

***Index Terms* — real-time simulation, voltage source converter, switched resistance simulation**

I. Introduction

1.1. Background

Switched-resistance representation of switch devices has existed in EMTP type programs since the beginning years of Dommel-method power system simulation [1]. At first, breakers and faults were represented as binary switched-resistances in EMTP-type simulation. In that case, a resistor branch with large resistance represented the OFF switch status and a resistor branch with small resistance represented the ON switch status. Later, the use of switched resistance extended to the representation of thyristors in Line Commutated Converters and then to representing IGBT and other gate-controlled devices in Voltage Source Converters.

The power converter switches in off-line simulation tools, such as PSCAD/EMTDC, are usually modelled with the two-value-resistor model. In that case, a switch is represented as a large resistance when it OFF and as a small resistance when it is ON [2]. However, the PSCAD/EMTDC algorithm employs interpolation to zero-crossing points within each time-step to adjust the system to times of switching events within a time-step. At a switch point, the statuses of the switches is adjusted and the Nodal Admittance Matrix (NAM) is re-factorized before the time-step calculations continue. There may be several consecutive time points within a single simulation time-step when the status of a switch may need to be changed. In that case, there is a need to be able to re-factorize the Nodal Admittance Matrix multiple times within a single time-step. The heavy computational burden associated with multiple NAM re-factorizations within a single time-step has resulted in the adoption for real-time simulation of fixed time-step network solutions with no interpolation in simulators such as the RTDS simulator [3]. Of course, fixed time-step simulation requires suitably small simulation time-step size.

Simulation algorithms that use an L/C Associated Discrete Circuit (L/C-ADC) model [3][4] generally use an inductor with small inductance L to represent an ON switch device and a capacitor with small capacitance C to represent an OFF switch device. It is well-known that the L/C-ADC switch representation can cause unrealistically high converter losses to appear in the simulation results, especially at high PWM frequencies. These high losses are related to switching back and forth between the OFF (capacitive) representation and the ON (inductive) representation of switches. Usually, whenever an inductance L is replaced by a capacitance C during a switching event, the energy in the inductor is lost. Similarly, whenever a capacitance C is replaced by an inductance L, the energy in the capacitor is lost. In addition, the L/C-ADC switch representation introduces, in any given time-step, a number of inductive and capacitive branches that do not actually exist in the real circuit. Inclusion of these L and C branches provides modes of current oscillation that do not actually exist in the real circuit. These associated current and voltage oscillations appear as noise in the simulation results. In addition, the impedance of OFF switches, represented as capacitors, decreases as frequency increases. Similarly, the impedance of ON switches increases with frequency. One benefit of L/C-ADC switch

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representation is that the same conductance value is used in forming the Nodal Admittance Matrix for both the ON and OFF switch statuses. This is beneficial because it removes the need for NAM matrix re-factorization when a switch changes ON/OFF status.

Often the switching devices in a voltage source converter interact in a way that is difficult to handle in a non-iterating non-interpolating fixed time-step simulation. For instance, in a simple voltage boost converter, Figure 1, when the IGBT is switched ON for the next simulation time-step, the representation of the diode (in Valve 1) should be changed from an ON switch status to an OFF switch status for the next time-step. If the ON/OFF status for the diode is not properly predicted as OFF for the next simulation time-step, then the IGBT and the diode will both be ON in the next time-step. In that case, if a switched-resistance representation of devices is used, then there will be a large erroneous spike of current backward through the ON status diode and the ON status IGBT in the next simulation time-step. The erroneous spike of current can be expected to be very large because both switches would be represented by a small resistor. The erroneous one time-step spike of current may be so large in magnitude that the accuracy of the simulation result could be ruined.

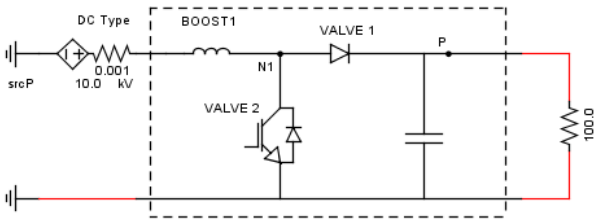

Figure 1. Voltage Boost Converter

When using L/C-ADC switch representations, the same value of resistance is used to represent the switch in the NAM matrix regardless whether the switch status is ON or OFF. However, the fixed resistance used in the NAM matrix for an L/C-ADC device will generally be much larger than the small ON resistance used to represent an ON device when using switched-resistance representation. This larger fixed resistance reduces the impact of erroneous predictions of ON/OFF switch status when using L/C-ADC by reducing the magnitude of any erroneous current spikes. Therefore, the prediction of switch ON/OFF statuses must be much more reliable when representing devices as switched resistances compared to when the devices are represented as L/C-ADC. Accordingly, in simulations using L/C-ADC switch representation, the ON/OFF status of a switch for the next simulation time-step is often predicted by simply using only the firing pulse input, prior ON/OFF status and the existing voltage and current of the particular switch. Occasionally simulators that use L/C-ADC switch representations will contain a table of specific events which can be detected so as to improve the prediction of switch ON/OFF statuses for the next simulation time-step for those events. However, those tables often only contain events that occur during the normal cycle of switching events that are expected in that type of converter. Sometimes the assumption is made that the voltage of the positive rail is always higher than the voltage of the negative rail in a voltage source converter. Unfortunately, that assumption is not always true during system start-up and severe disturbance situations. Consequently, the use of rule-based state transition logic and event tables for predicting ON/OFF switch statuses occasionally produces a wrong ON/OFF status prediction. This has very little impact when using L/C-ADC switch representation. On the other hand, a wrong prediction of ON/OFF switch status can ruin the accuracy of a simulation when using switched-resistance switch representation.

1.2. OUTLINE OF THE PREDICTION METHOD

An algorithm is described in this paper that provides a highly reliable method of predicting the ON/OFF statuses of switches in a voltage source converter (VSC) for the next simulation time-step when switched-resistance switch representation is used. The prediction method has been used in a range of VSCs including the 2-level VSC, 3-level T-Type VSC, 3-level NPC VSC and the simple voltage boost converter. Figure 2 shows a 3-phase 3-level T-Type VSC converter in a very simple circuit. The switch devices for one phase in a VSC bridge are typically referred to as a VSC leg.

A leg in a VSC bridge generally includes a group of switch devices which can be represented in a simulation using the switched-resistance switch representation. There is a strong electrical interaction between switched devices within the leg of a VSC. However, the switch devices in a particular leg have only very weak electrical interactions with switch devices outside the leg. That is because, by design, the devices within a given VSC leg only connect to the outside circuit at peripheral nodes where voltages are stabilized by large capacitors (DC Rails) or where currents enter through inductive elements, such as inductors, which smooth the currents. Therefore, switch ON/OFF statuses for the next simulation time-step are typically separately predicted for each leg independent of other legs. That technique is continued in the algorithm of this paper.

For the switched-resistance simulation, sometimes it is possible to treat more than one physical device as a single combined switch device in the simulation. For instance, in an IGBT 3-level T-type converter, there are typically 2 IGBT-diode devices connected in series in the path to the Neutral Rail peripheral node (for example, node O in Figure 2). These 2 series IGBT-diode physical devices can be treated as one combined switched device in the simulation. Each of these combined switch devices is represented as one switched resistance device in the simulation.

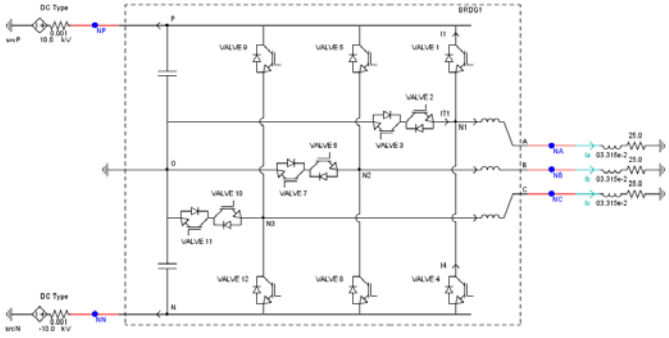

Figure 2. 3-phase 3-level T-Type VSC

The prediction algorithm involves creating a mathematical ADC test circuit for each leg to be used in the prediction of switch ON/OFF statuses before each simulation time-step. The test circuit for a particular type of VSC must contain N switched-resistance branches where N corresponds to the number of switched-resistance devices represented in the simulation of the VSC converter leg. For instance: N=2 for the 2-level VSC, N=3 for the 3-level T-Type VSC and N=6 for the 3-level NPC VSC. Each leg is also connected to peripheral nodes with stable voltages provided by the DC Rails. Also, each of the example converter types has a single inductive path connected into the leg from an external peripheral node. For a different VSC type, the algorithm can accommodate more than one inductive path into the leg from a peripheral node. The algorithm can also accommodate other branch types connected within the leg such as RC snubbers. An ADC test circuit for a leg of a T-type VSC is shown in Figure 3.

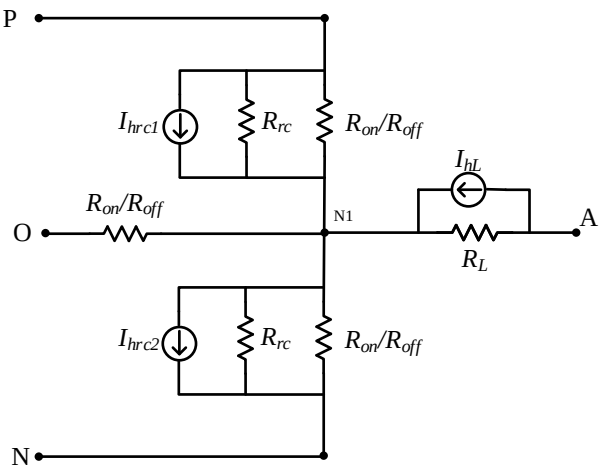

Figure 3. ADC Test Circuit for T-type VSC Leg

An ADC test circuit with N independent switched-resistance devices has 2 raised to the power of N combinations of ON/OFF switch statuses. For instance, for a 3-level T-type VSC leg, the test circuit has 8 possible combinations of ON/OFF switched statuses for the next simulation time-step. The task of predicting the correct combination of switch ON/OFF statuses for the leg involves testing the possible combinations to find the combination that is valid for the latest firing pulses, peripheral node voltages and ADC history currents of the passive branches (inductor and RC snubber). The latest ADC history currents are calculated only once before to each simulation time-step based on the latest peripheral and internal node voltages obtained in the previous time-step.

It is clear that one of the tested combinations of ON/OFF switch statuses will be a valid combination because all possible combinations are considered in the search for the valid combination.

This paper is organized as follows. Section II describes in detail the process of using the test circuit to make predictions of switch ON/OFF statuses. Section III presents simulation results for circuits containing 2-level VSC and 3-level T-type VSC converters. The virtual losses of the converters are low and the wave shapes are free of the signal noise associated with L/C-ADC simulations. Section IV provides conclusions including describing practical limitations when using the prediction algorithm on real-time simulators using existing high performance computing cores.

II. Algorithm for Prediction Switch ON/OFF Statuses in VSC Converters

Figure 2 shows a typical 3-phase IGBT-based 3-level T-type VSC converter in a very simple system. This VSC converter contains 3 legs which are each handled separately when predicting the ON/OFF statuses of switch devices. Peripheral nodes for the leg include the DC rail nodes (P, O and N) and the node on the external end of the leg inductor (A). The switch devices within the leg strongly interact with other switch devices within the leg. In addition to the switch devices, a leg includes the internal nodes, inductor and any other passive branches such as RC snubbers.

As described in the introduction, it is very important to have a reliable prediction of switch ON/OFF statuses when representing switch devices with switched resistances. A wrong prediction can ruin a simulation result. For the algorithm, a mathematical ADC test circuit is created for the leg (as in Figure 3 for a 3-level T-type VSC), in order to facilitate the prediction of ON/OFF switch statuses. There are 3 switched conduction paths in this particular test circuit. There are only 3 such paths in this test circuit because the two series IGBT-diode devices in the path to the Neutral Rail in the actual circuit are considered as a single switched device in both the test circuit and in the simulation of the larger overall system. The test circuit in Figure 3 also includes ADC representations for the inductor and RC snubber branches in the leg.

Since there are 3 (N=3) switched conduction paths in our example test circuit, there are 8 (2 raised to the power of 3) possible combinations of ON/OFF switch conductances that can be searched for a valid combination of ON/OFF switch statuses using the test circuit.

In order to configure the test circuit for the search, the voltages of the peripheral nodes in the test circuit (P, O and N)

are set to the voltages of the corresponding nodes in the actual circuit from the last time-step. The latest ADC branch history currents are also used in the test circuit as fixed values. The ADC history currents are updated only once before to each simulation time-step using the latest peripheral and internal node voltages obtained in the previous time-step.

When the test circuit is thus configured for the search, the internal nodes voltages within the test circuit for the leg can be calculated for any combination of ON/OFF switched conduction statuses. In our example test circuit, node N1 is the only internal node. However, there would be 3 internal nodes in the test circuit for a leg of a neutral point clamp (NPC) VSC. Any suitable network solution method can be used to obtain the internal voltages for a particular test. The associated branch voltages on the switched devices in the test circuit are readily obtained from the internal and peripheral node voltages.

The switch devices represented in the simulation will each behave as a known ON branch, a known OFF branch or a diode branch based on the firing pulses applied to the device. For instance, Valve 1 in Figure 2 will behave as a known ON branch when the IGBT is fired ON. However, Valve 1 will behave as an upwardly-directed diode when the IGBT is not fired ON. Similarly, in Figure 2, Valves 2 and 3, which are treated as one switched device in the simulation, can behave as a known ON branch when both IGBT devices are fired ON, a known OFF branch when neither IGBT device is fired ON, a diode directed toward node N1 when only IGBT 2 is fired ON or a diode directed toward node O when only IGBT 3 is fired ON. Of course, a switch device consisting of a single diode always behaves as a diode branch in the actual circuit and the test circuit. Similar logic could be developed for other types independent switched devices. For instance, a thyristor in some other type of converter could behave either as a known OFF branch or a diode depending on both the firing pulse and the previous conduction status of the thyristor. The behavior of the independent switch devices needs to be determined only once prior to commencing the search for a valid combination of ON/OFF switch statuses.

A simple implementation of the algorithm uses the test circuit to consecutively test all combinations of ON/OFF conduction statuses. For example, the tests would begin with all conduction statuses OFF (for instance, combination 0b000) and end with all conduction statuses ON (for instance, combination 0b111). In each test, the test circuit provides the forward voltages on branches that behave as diodes. Fortunately, in the search for a valid combination of ON/OFF switch statuses, it is not necessary to use the test circuit to consider all combinations of ON/OFF conduction statuses. That is because, as discussed above, certain switch devices represented in the simulation may already be known to have ON conduction status or OFF conduction status. In that case, it is not necessary to consider combinations which to not reflect those known device statuses. Also, to improve efficiency, simple rules may be developed and applied to modify the order in which the possible combinations of ON/OFF conduction statuses are searched in order to find a valid combination. The search is complete when a valid combination of ON/OFF switch statuses is found.

Of course, it is necessary to be able to identify that a particular tested combination of ON/OFF conduction statuses is, in fact, a valid combination of ON/OFF conduction statuses when using the test circuit. As discussed above, those branches in the test circuit that will behave as diodes are identified prior to beginning the search, as are the diode directions. Also, for any particular combination of ON/OFF conduction statuses searched, the test circuit provides the diode forward voltages. Therefore, the algorithm can readily determine which diodes would be ON or OFF based purely on the forward diode voltages. If the pattern of ON/OFF diode statuses indicted by forward voltages in the test matches the tested combination of ON/OFF conduction statuses, then the tested combination of ON/OFF conduction statuses is a valid combination.

As described above, a valid combination of ON/OFF conduction statuses can be identified by a search of the possible combinations of ON/OFF conduction statuses using the test circuit. Once a valid combination is identified, it is used to set the switch resistances for the next simulation time-step of the overall simulation system.

III. Simulation Results

The results from two simulation cases are presented. The cases were both executed on POWER8 processor cores in an RTDS NovaCor simulator. In both cases, some of the higher level controls were executed on a separate core. However, all of the power circuit components were executed on a single core including a re-factorizing Nodal Admittance Matrix network solver and the converter models. The processor core operates at 3.496 GHz. The switched-resistance branches in the converters are embedded in the matrix of the NAM solver.

The purpose in presenting these cases is: to show the very clean wave shapes produced by the models (reflecting the nearly ideal converter representation provided by the switched resistances); to show that the virtual losses in switched-resistance convertor models approximate or are lower than those in real converters; and to demonstrate the size of the time-step size that can be achieved.

The first case is a 3-level T-type VSC bridge in a very simple circuit. The second case is a simple back-to-back DC link with 2-level switched-resistance VSC bridge models.

A. Case 1

Figure 2 shows a 3-phase 3-level T-type switched-resistance VSC bridge in a very simple circuit.

The Figure 4 shows plots of the AC-side load currents, the voltage on internal node N1, the upward current in Valve 1, the current through Valves 2 and 3 directed toward the load, and

the current upward through Valve 4. The plots are clear and without the noise that is often seen in simulations that use L/C-ADC device representations.

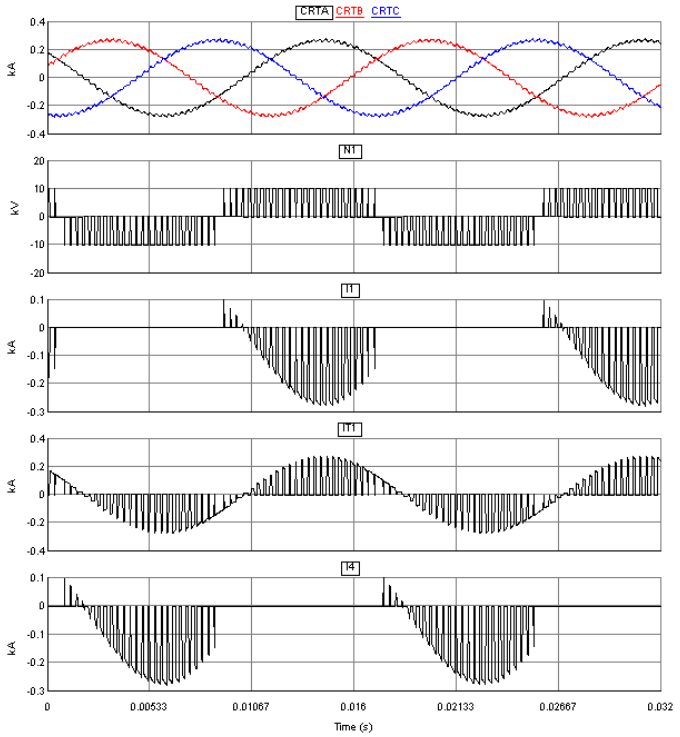

Figure 4. Plots for T-Type VSC Bridge

The switching shown in the plots is for 3,060 Hertz PWM. At that frequency of PWM, the virtual losses between the power going into the DC side and the power going out the AC side is 0.259 percent. At 9,900 Hertz PWM, the losses are 0.333 percent. These losses are very likely lower than the losses in an actual physical T-type converter operating at those PWM frequencies. However, if necessary, the virtual losses in the model can be increased as required to match the losses in a real converter by decreasing the OFF resistance of the switched-resistance device representations or increasing the ON resistance.

The number of nodes in the re-factorized NAM network is only 8 in this case. There are the 5 external nodes for the DC and AC connections. There is also an internal node for each phase, shown as N1, N2 and N3 in Figure 2. The model actually layers all of the branches and switches shown in the bridge icon onto the network that is solved by the NAM solver. The VSC bridge model sends conductance values for each valve to the NAM solver before the network is re-factorized in each simulation time-step.

With the limited number of nodes, the case runs with a real-time simulation time-step of 1.66 uSec. All of the power components run of one processor core, including the NAM solver and the converter model. The required simulation time-step size will increase as the number of nodes is increased.

At the present time, some of the models that we have used in our Sub-step modelling (such as some breakers, sources, transformers, controls and loads) are exactly the same models that we use in the Main-step modelling on our NovaCor simulator. These Main-step models were initially created to run with simulation time-steps of 20 uSec and upward. Therefore, going forward the models will be optimized to make them more suitable for execution in a Sub-step environment where time-steps of 2.5 microseconds might be closer to the norm. Fortunately, all the models have been written in C using the RTDS CBuilder facility. Therefore, optimizing will be relatively easy compared to the days when models were hand-written in assembly.

B. Case 2

Simulation Case 2 is the back-to-back 2-level VSC DC link case that contains 28 nodes in the NAM network solver. A basic schematic is shown in Figure 5. We forced all of the power system components and the network solution to be solved on a single core. Normally, we would probably solve this case using two cores joined by a stub t-line connection having a one sub-step travel time. However, in this case we wanted to force as much network as presently feasible onto one core to demonstrate the minimal effect of a larger simulation time-step size on the quality of the waveforms and on the level of virtual losses.

In this case, each bridge sends 6 conductance values to the network solver before the network solution for each real-time simulation time-step. There are also 6 single-phase breakers represented as switched-resistances in the case which are used to switch two 3-phase loads. Therefore, there are 18 conductance values sent to the network solver before each simulation time-step. Of the 28 nodes, 22 nodes have switched-resistance branches connected to them. Therefore, the NAM solver decomposes a 22 node portion of the matrix in each real-time simulation sub-step. The NAM solver also does backward and forward operations for the entire 28 node matrix in each simulation sub-step. Therefore, the case is a heavy computational burden, even for a POWER8 processor core. As a result, the simulation time-step needed to be 3.89 microseconds for this size of case. That time-step size is approaching the upper limit for the time-step that would normally be used due to the need to have adequate resolution in applying firing pulses.

The Figure 6 shows plots for an A-phase converter current in the circuit of Figure 5. Figure 6 also shows the voltage on a node between the upper and lower valves in a leg as well as the upper and lower valve currents. The plotted signals are virtually free of the noise that would typically exist if L/C-ADC device representation was used.

The plots shown in Figure 6 are those that exist for 3,000 Hertz PWM. In that case, the difference between power entering the primary of one transformer and exiting the primary of the other transformer was 0.5 percent of the power entering.

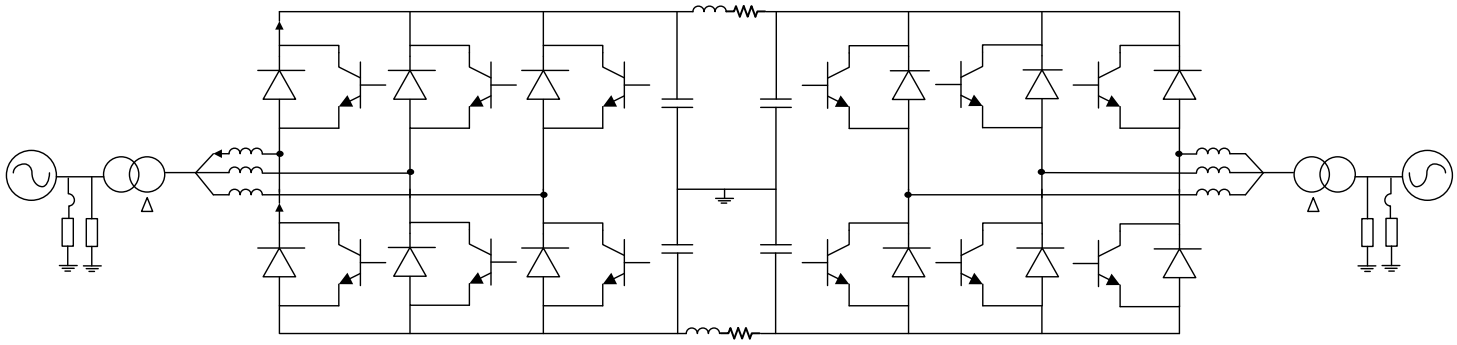

Figure 5. Back to Back 3 phase 2 level VSC

The power losses remained almost the same at 0.51 percent for 5,000 Hertz PWM and reached 1.0 percent for 10,000 Hertz PWM. This would probably be less than the losses of a real system operating at this PWM rate. Again, the virtual losses could be increased by decreasing the switched-resistance OFF resistances or increasing the switched-resistance ON resistances.

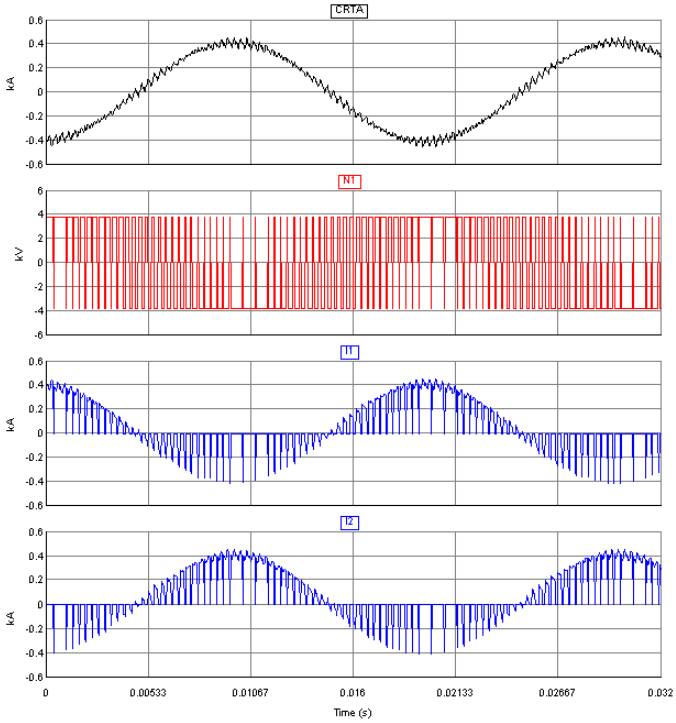

Figure 6. Plots for 2-level VSC Bridge

Case 2 has demonstrated that switched-resistance switch device representation substantially prevents the quality of the simulation result from decreasing when the simulation time-step size increases. This is an improvement with respect to L/C-ADC switch representation where one would typically expect a decrease in the quality of the simulation result. However, for higher PWM frequencies, the time-step size must still be limited in order to provide the necessary resolution of firing in a fixed time-step simulation. The computational burden when using switched-resistance switch representation is significantly higher than when using L/C-ADC switch representation. Therefore, for the same real-time simulation time-step size, the size of the converter system that can be simulated using switched-resistance representation of devices is less than the size of the system that can be modelled when using L/C-ADC switch representation. Case 2 has been presented in an effort to show the size of the converter network that can be simulated in real-time on a single processor core with a simulation time-step of 3.89 microseconds (35 uSec/9 substeps) when using switched-resistance device representation.

Unfortunately, the network in Case 2 is perhaps one-half of the size that might be solved when using LC/ADC device representation for simulation in real-time with the same time-step size. Fortunately, improvements in processor hardware continue to be made. For instance, the newly released POWER9 processor chip has two tightly-coupled processor cores on each of the 10 “chiplets” within the POWER9 chip instead of the single processor core per “chiplet” in the POWER8 processor chip. Therefore, over the next couple of years, we will investigate the possibility of using the POWER9 processor core in real-time simulation to accommodate the ever higher computational burdens.

The technique described in this paper could be applied directly to produce a switched-resistance model of an NPC VSC bridge. However, the computational burden presented by such a model would be very heavy. Therefore, we have created a switched-resistance NPC bridge model indirectly by using a switched-resistance T-type bridge model as a surrogate network in the NPC bridge model. The NPC firing-pulse input is mapped to provide the same 3-level simulation result in the T-type surrogate network. To provide NPC model current outputs, the T-type converter currents are converted to the currents that would exist in an NPC converter. Other refinements are included in the T-type converter that is used as a surrogate network for the NPC converter. Since the NPC model involves many computational methods used in the T-type converter, the execution time and the quality of the outputs are similar. For the present processor cores, it is probably not practical to directly create switched-resistance bridge models that are much more complicated than a 3-phase NPC model.

IV. Conclusion

This paper has presented a technique for reliably predicting the ON/OFF statuses of switch devices in VSC converter models for the next simulation time-step. The technique is particularly useful when switch devices are represented as switched-resistances.

Using switched-resistance representation of switch devices gives much higher quality of simulation result at a given time-step with regard to freedom from noise in output signals and the virtual elimination of excessive virtual losses.

However, switched-resistance device representation that generally produces a higher quality simulation result also creates a higher computational burden compared to L/C-ADC device representation. This means that the size of network that can be simulated with a given real-time simulation time-step size when using switched-resistance device representation is smaller than the size of the network that can be simulated when using L/C-ADC device representation. A rough estimate of the network size is one-half. Therefore, for the present, switched-resistance device representation and L/C-ADC device representation will both continue to be used depending on the quality of simulation that is required and the size of the system network that must be simulated.

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