Modelling a 3-level NPC bridge with resistive switching by conditioning a 3-level T-type bridge

INTRODUCTION

With the vast increase in processing power introduced with the POWER8 processor cores used by the RTDS NovaCor simulator, it is possible that networks of a certain size can have their Nodal Admittance Matrix (NAM) re-factorized in real time with time steps in the range of 1-4 usec. This supports the use of resistive switching to model power electronic switches as oppose to the LC Associated Discrete Circuit (LC-ADC) [1] method used in the small time step simulation. In [2], the algorithm used in RTDS for predictive resistive switching for ON/OFF statuses has been described which is highly reliable for modelling power electronic converters with a fixed time step. The simulations presented in the paper show results that have low virtual losses and are free of the signal noise that is associated with the LC –ADC method.

The prediction of proper switch resistances described in the paper focuses on a single leg of a VSC (ex. 2 level, 3 level) at a time. There will be strong electrical interactions between the switching devices within a VSC leg and the algorithm reliably predicts the switch ON/OFF statuses for the next simulation time step. For example, in a 2-level VSC leg, if the upper half valve is newly fired ON for the next time step, the free-wheeling diode in the complimentary lower half may be ON and should be switched to OFF. If this is not properly predicted, then the upper valve and the complementary diode will both be ON for the next time step. That results in a very small resistance placed across the DC link capacitor and will generate a large inaccurate spike of current for one time step that can ruin the simulation results. In offline tools, interpolating techniques are used to prevent such numerical inaccuracies but this cannot be used so effectively for real time. The purpose of the predictive switching algorithm is to prevent this scenario from occurring. The algorithm creates a mathematical ADC test circuit for each leg to be used for the prediction of the switch ON/OFF statuses before each simulation time step. The algorithm will go through all the possible switch status combinations on the test circuit to determine the valid combination and use it for the real model. The algorithm does not need to consider switches in different legs because they will have weak electrical interaction with switches in the prediction leg. The separation between legs occurs because each leg is connected at external nodes where on the DC side the voltage is stabilized by large capacitors and on the AC side the currents enter through inductors which will smooth the currents.

The paper [2] describes the switched-resistance prediction algorithm for a 3-level VSC T-type leg. Each leg of the 3-level T-type VSC leg in the model contains three (3) switched resistances. This corresponds to 8 possible switching combinations and the prediction algorithm will utilize a test circuit shown in Figure 1 to find the valid combination for the ON/OFF switch statuses for the next time step. The mathematical test circuit facilitates the prediction of the ON/OFF switching statuses. [2] showed the successfully results obtained from the predictions switching algorithm for the 3 level T-Type bridge model.

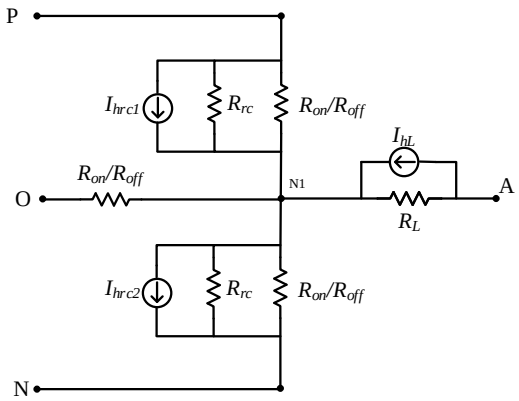

Figure 1 ADC test circuit for T-type leg

A similar approach could be adopted for the 3-level NPC leg. Each leg of an NPC configuration will have six (6) switched resistances. This would correspond to 64 difference switching combination. Compared to a T-type configuration, there is significantly more combinations that would need to be tested in each time step to find a valid ON/OFF statuses for each leg. Furthermore, a three-phase 3-level NPC type bridge would send 18 conductance values to the network solver compared to 9 from a 3 phase T-type bridge thereby placing greater computational burden on the re-factorization of the matrix in real time.

However, due to the similarities of the NPC bridge model and the T-type bridge model, it is possible to develop a switched-resistance 3-level NPC VSC bridge by using a switched-resistance T-type bridge model as a surrogate network for the NPC bridge model. The NPC firing pulses will be mapped to the T-type converter and it is possible to produce accurate simulation results from a T-type configuration conditioned to act as an NPC bridge model. For monitoring purposes, the T-type valve currents can also converted to the currents that would exit in a NPC bridge model. The execution time of the NPC bridge model as well as it computational burden to the network solver will be reduced to that similar to a T-type converter bridge.

FIRING PULSE DIFFERENCES BETWEEN THE T-TYPE AND NPC VSC CONVERTERS

Consider Figure 2 which shows a single leg for the NPC converter and a T-type converter

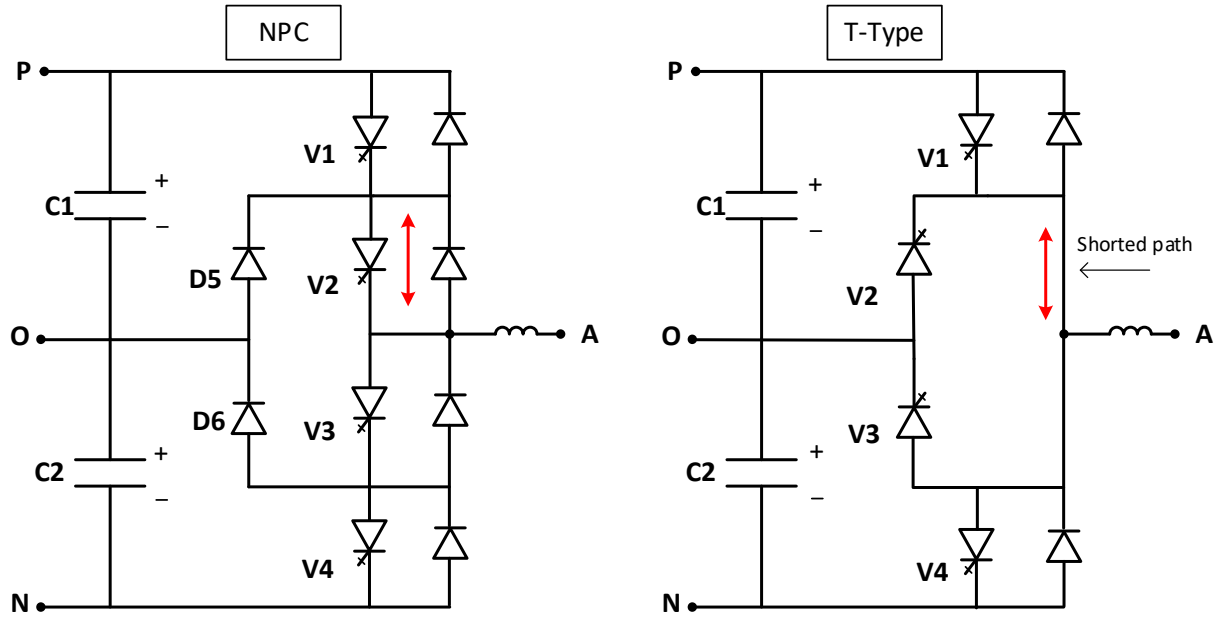

Figure 2 Single leg for NPC and T-type converter

The upper and lower halves of a leg act the same way and therefore it is sufficient to analyze the top half only. Consider the current paths marked in red in Figure 2 that are located at similar places in the NPC and T-type converter leg. In the NPC leg, the current path marked in red is the current in Valve 2. In the T-type leg, the current path marked in red is the current in the "Shorted path". When Valves V2 in the NPC leg and the T-type leg are fired, then the upper half of both legs will be electrically identical because Valve V2 in the T-type will act like the Diode D5 in the NPC bridge, and Valve V2 in the NPC leg will act like the shorted path in the T-type leg. Both legs will continue to act in an identical way as long as Valve 1 is fired in the same way in both legs. Valve V3 in the bottom half will have the same characteristic.

The more interesting case occurs when Valve V2 is NOT fired as there will be difference in the behaviour for the NPC leg and the T-type leg. When Valve V2 is NOT fired ON in either leg type, then there is NO available path in the upper half of either leg for current to flow DOWNWARD in the red path from the Neutral DC rail (O) towards the load. This is the case regardless of whether Valve V1 is fired in either leg or NOT. When both Valve V2 and Valve V1 are NOT fired ON in either leg, then there is no available path in the upper half of either leg for current to flow DOWNWARD in the red path from the Positive rail (P) towards the load.

However, when Valve V2 is NOT fired but Valve V1 is fired ON then the NPC and T-type legs will behave differently with respect to providing a path in the upper half for current to flow DOWNWARD from the Positive rail (P) towards the load. T-type leg will provide a path for current but the NPC leg will not since Valve V2 is OFF. Therefore, to have the T-type leg behave as an NPC leg, Valve V1 for T-type surrogate network should only fire ON when both Valves V1 and V2 are fired ON from the NPC leg.

This requires conditioning the 4 bit NPC firing pulse word (Valve V1-V4) before applying it to T-type surrogate network acting as an NPC leg. This conditioning is very simple. Valve V1 in the T-type leg should only get an ON firing signal when the NPC firing word contains an ON bit for both valves V1 and V2. Similarly, Valve V4 in the T-type leg should only get an ON firing signal when the NPC firing word contains an ON bit for Valves V3 and V4. Valve V2 and V3 firing bits for the NPC leg does NOT require any conditioning and are passed to the T-type surrogate leg unchanged.

GENERAL MONITORING ISSUE

Creating the basic monitoring signals for the NPC converter leg is actually quite simple. Reference to Figure 1 above is helpful. As discussed below, adjustments are made later to the basic NPC monitored currents for D5 and Valve V1 involving capacitor C1. Similar adjustments are made to the basic NPC monitored currents NPC diode D6 and Valve V4 currents. The simulated currents upward through Valve V1 and Valve V2 in a leg of the surrogate T-type converter are sufficient to provide the basic monitored valve currents for the upper half of a leg in the NPC converter model. The basic monitored upward current for Valve V1 in the NPC model is the same as the upward current in Valve V1 of the T-type simulated leg. The basic monitored upward current through Valve V2 in the NPC model is calculated as the upward current through Valve V1 in the T-type converter minus the upward current through Valve V2 in the T-type converter. The basic monitored upward current through diode D5 in the NPC model is the same as the current upward through Valve V2 in the T-type converter. As discussed above, adjustments are made later to these basic monitored valve current signals to account for currents upward through a discharged C1. Basic monitored valve current signals for the lower half of the NPC leg are made in a similar way to those in the upper half of the leg.

CAPACITOR MODELING ISSUE

The behavior of the DC side capacitor for the two bridge models needs to be considered due to a difference. Referring to the upper half, the NPC type bridge is always able to pass current UPWARD in a current path through Diode D5 and the diode in Valve V1. However, a T-type leg provides a similar path only when T-type Valve V2 is fired ON. Therefore, the capacitor C1 in the NPC bridge can never charge to a negative voltage due to the permanent path through D5 and V1. A current that would build negative voltage on C1 would instead bypass capacitor C1 and pass upward through diode D5 and the diode in valve V1. On the other hand, the capacitor C1 in the T-type bridge could charge to a negative voltage if Valve V2 was not fired ON in the T-type bridge. Therefore, measures are needed to assure that the C1 capacitor in the T-type bridge (acting as a surrogate network) will never charge to a negative voltage in order to make the T-type bridge act like an NPC type bridge. Fortunately, this can be done by modifying the capacitor branch model so that it cannot accumulate a negative voltage.

For the Dommel algorithm [3] used by the RTDS simulator, a discrete model of the capacitor branch consists of a Dommel resistance ($R=\Delta t/2C$) and a parallel downwardly-directed history current. When the capacitor C1 accumulates a positive voltage, the downwardly-directed history current source will have a negative current value. On the other hand, in order to accumulate a negative voltage, the history current would need to go positive. Therefore, when a new capacitor C1 history current is calculated for the T-type converter bridge (acting as the NPC surrogate network), an upper limit of 0.0 kA is placed on the calculated capacitor history current so that it cannot go positive. Adding this condition prevents the capacitor C1 in the T-type converter from accumulating a negative voltage in the simulation and therefore capacitor C1

voltage will behave the same as in the NPC bridge model. In this way, the discharged capacitor C1 in the T-type converter is made to act as a low-resistance path to upwardly-directed current that would otherwise tend to charge C1 to a negative voltage. In the NPC type bridge, such an upwardly-directed current would bypass C1 and pass through the diode D5 and the diode in valve V1.

This creates a monitoring issue. In circumstances where such an upwardly-directed current flows through a discharged C1 in the T-type surrogate converter, the monitored capacitor C1 current for the NPC converter is set to 0.0 and the upwardly-directed C1 current in the T-type surrogate is divided between the valves in the N legs of the NPC converter. In particular, a fraction 1/N of the upwardly-directed T-type capacitor C1 current is added to the basic monitored currents for diode D5 and Valve V1 in each of the N legs of the NPC model. A similar approach is taken for the bottom half of the leg including capacitor C2, Diode D6 and Valve V4.

SNUBBER AND VALVE RESISTANCE ISSUE

A current flowing between the Positive DC rail (P) and the load (A) must pass through two valves in the NPC converter but passes through only one valve in the T-type surrogate converter that is actually used in the simulation. Therefore, when a User specifies valve ON/OFF resistances in the NPC converter model, those specified resistance values are doubled for use in the T-type surrogate converter. Similarly, the snubber capacitance specified by the User in the NPC model are reduced to half in the T-type surrogate model. This keeps the valve Ron/Roff resistance losses for the NPC model equal to those that the User would expect based on simple power calculations.

SIMULATION RESULTS

Results are presented for the NPC bridge model. Figure 3 shows a 3-phase 3-level NPC VSC bridge in a very simple circuit. While the icon shows a NPC configuration, as the described above, the converter bridge actually used in the simulation is a T-type bridge conditioned to perform as a NPC bridge. The case is executed on a RTDS NovaCor simulator. The circuit runs in the **Substep** network which is an environment that will run certain optimized model at time steps as lows 1-4 usec and which performs a matrix re-factorization in each time-step to support resistive switching. This is only possible due to the high performance of the NovaCor POWER8 processor cores.

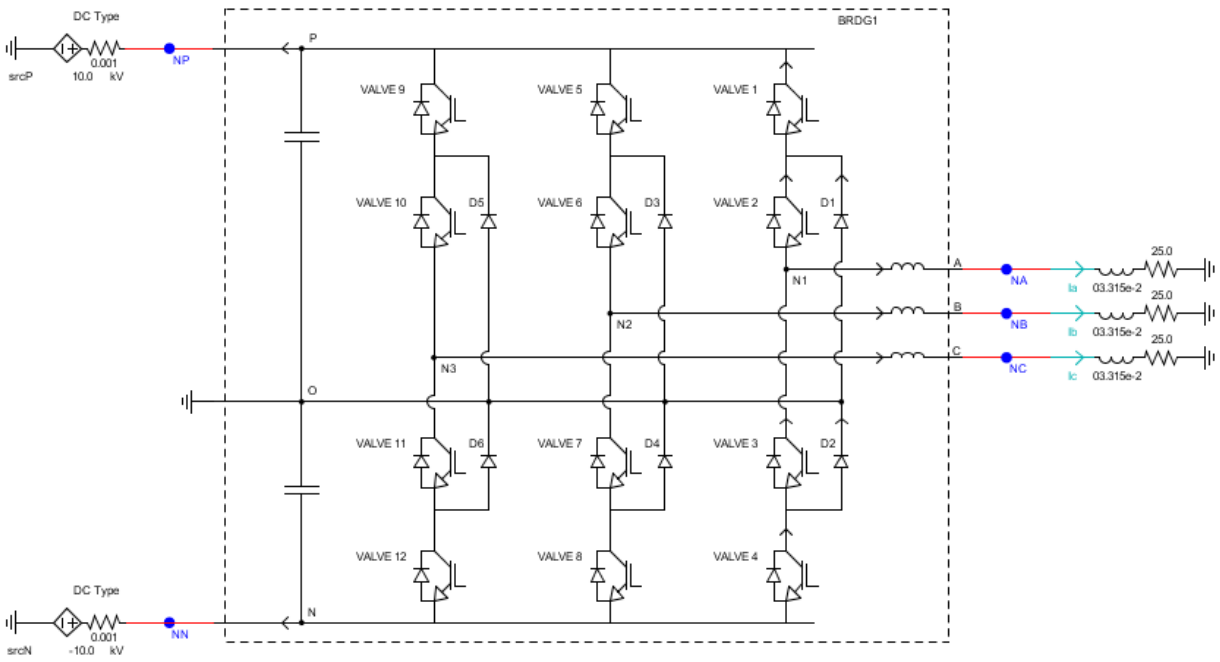

Figure 3 3-phase 3 level NPC leg from T-type surrogate network.

One of the purposes of presenting the case is to show that the bridge model is in fact performing as a 3 Level NPC. Therefore, the same circuit is built in the small time step environment as shown in Figure 4 and the results are compared.

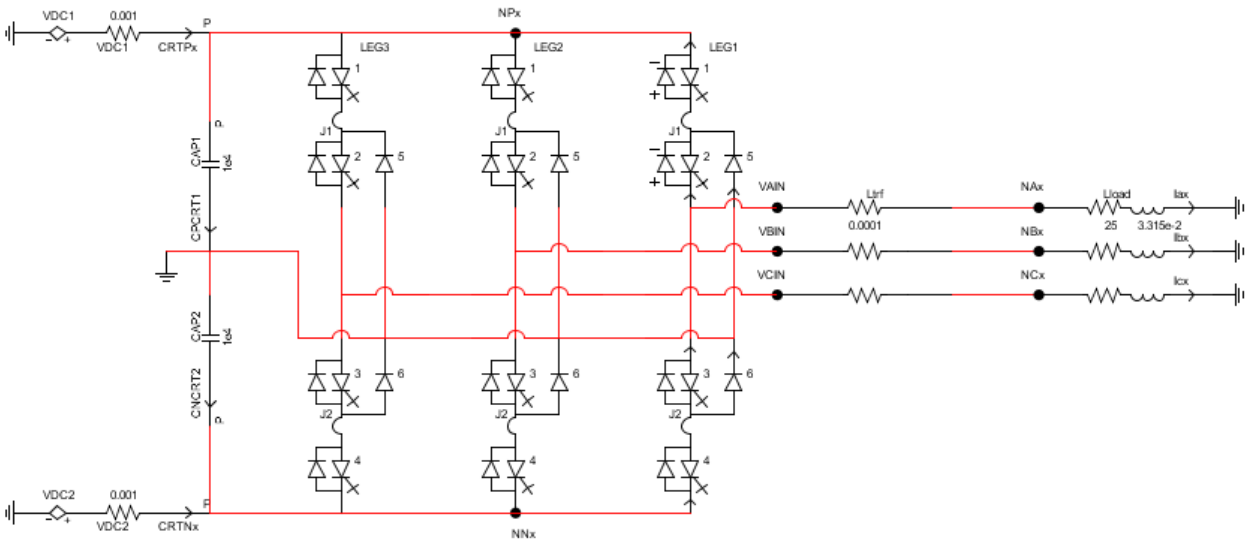

Figure 4. 3 phase 3 phase 3-level NPC circuit in small time step

The 3 level NPC model in the small dt does not use predictive resistive switching, but instead the L/C ADC method. It is well known that this method is associated with higher converter losses and current/voltage oscillations that do not actually exist in the real circuit. Therefore, while results will show the NPC leg modelled with resistive switching based on the T-type leg will have the same voltage and current wave

shapes as the small time step model, it will also show that the virtual losses are lower and the wave shapes are cleaner. The time step for the Substep case is 1.66 usec and small time step case is 1.56 usec.

Figure 5 shows the comparison plots with the NPC type bridge in Substep and in the small time-step. The plots shows the AC side load currents (CRTA, CRTB, CRTC), the internal phase A voltage (VN1), and currents through Valves 1, 2, 3, and 4 (IV1, IV2, IV3, IV4). The switching frequency is set to 1260 Hz. This was chosen mainly due to the limitation for the switching frequency supported by the L/C-ADC method used for the small time-step NPC bridge model. From the plots, the wave shapes are the same showing the correct current paths for the NPC leg in Substep i.e. the T-type bridge conditioned to act as a 3-level NPC bridge. The difference in the quality of waveforms is due to the LC-ADC modelling method used in the small time-step environment which generates the usual L/C oscillations and small spikes in the voltage and current. As shown in the plots, the NPC Leg with resistive switching produces clean waveforms with no oscillation due to the ideal representation of the bridge by resistive switching. At 1260 Hz PWM, the virtual losses for the power going into the DC side and the power going out the AC side was 0.18 % for the NPC bridge in Substep compared to 3.0% for the small dt LC-ADC NPC model.

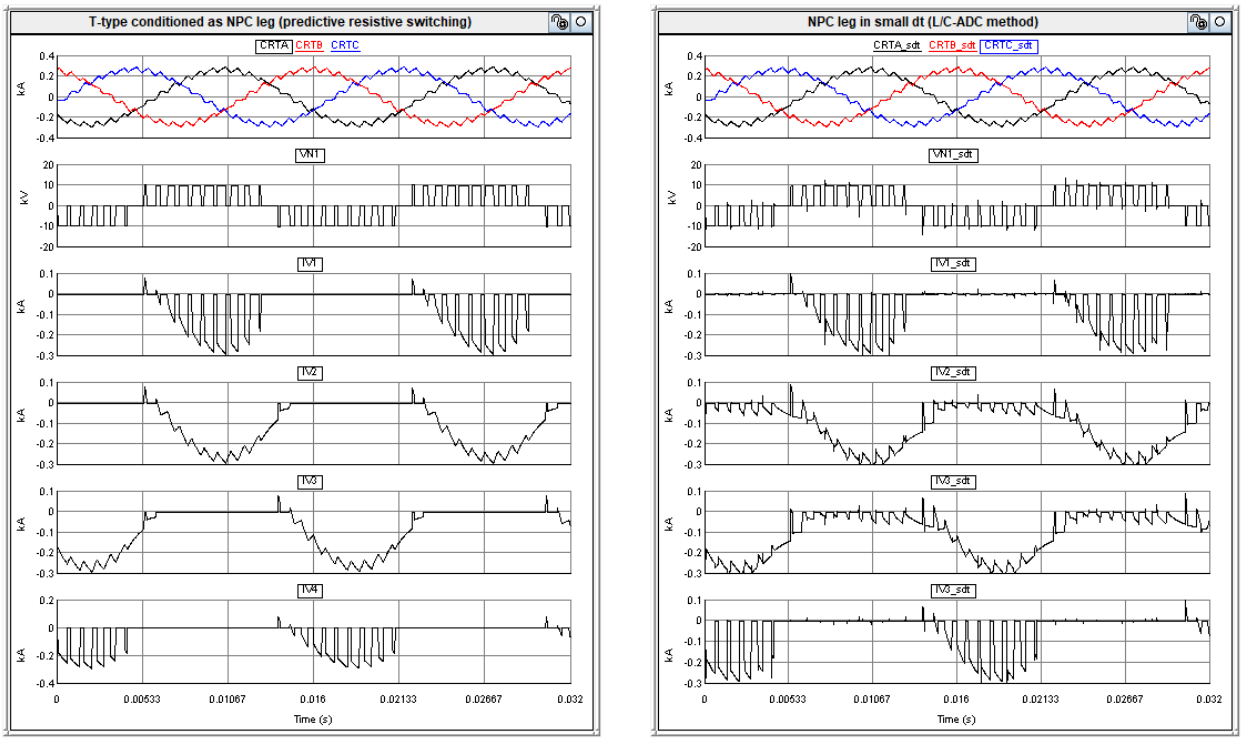

Figure 5. Plots for T-type conditioned for NPC (left) and NPC in small dt (right)

At 3060 Hz PWM, the virtual losses are 0.22% and 6.5% respectively for the Substep resistive switching model and L/C-ADC small dt model. The losses from the NPC resistive switching model are likely smaller than the losses from a real device. However, the ON and OFF resistance can be modified to increase the switching losses.

To further validate using a T-type bridge to act as a 3-level NPC bridge, an identical case is developed in the offline EMT tool PSCAD as shown in Figure 6. PSCAD employs interpolation and chatter removal

techniques to improve the quality of the waveform. The predictive resistive switching employed in the 3 level NPC Substep model is aimed at the same objective.

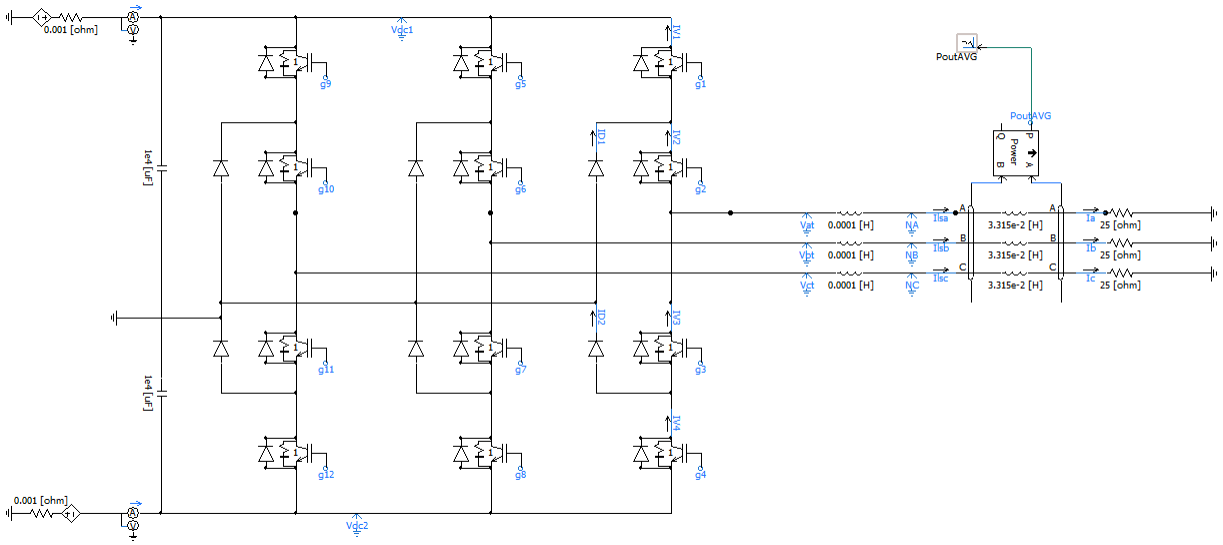

Figure 6. 3 phase 3 Level NPC converter in PSCAD

The results are shown in Figure 7. The plots show the AC side load currents, the internal phase A voltage, and currents through Valves 1, 2, 3, and 4 and are plotted in RTDS (suffix _R) and PSCAD (suffix _P). From the plots it is clear that both simulation produces nearly identical results. This further shows that the T-type configuration conditioned to act as a NPC bridge will produce accurate results and the predictive switched resistance algorithm will produce clean waveforms that produce the same waveforms as offline EMT tools that can use interpolation to resolve numerical inaccuracies.

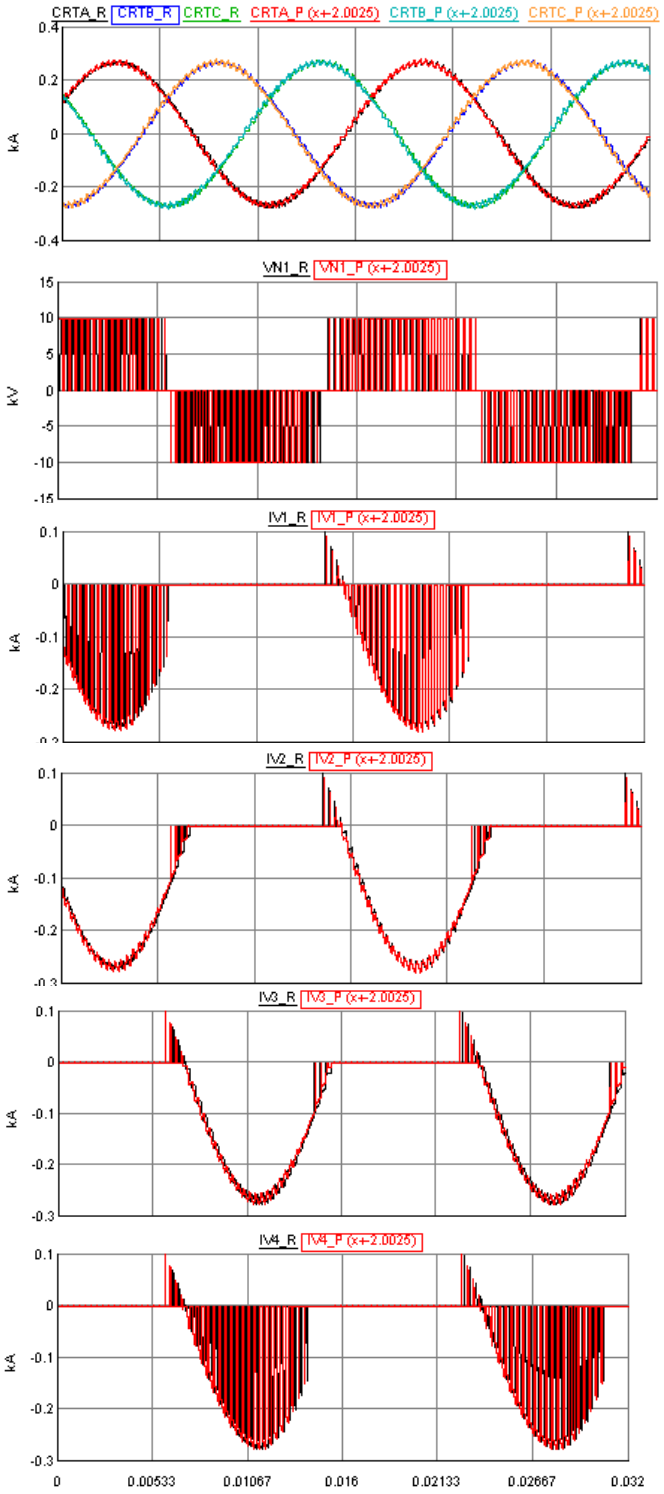

Figure 7. RTDS(_R) and PSCAD(_P) comparison of NPC converter

SUMMARY

Using the approach above enables the NPC 3 level VSC converter to be modelled using a T-type converter model internally as a surrogate network. By the conditioning the T-type leg to act as a NPC leg, the T-type model will produce the same behaviour as a real NPC leg. The benefits of using this approach is to reduce the computational requirement for the model and sending less switched elements to the network solver.

Sumek Elimban

October 5th 2018

REFERENCES

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[2] T. Maguire, S.Elimban, E. Tara and Y. Zhang " Predicting Switch ON/OFF Statuses in Real Time Electromagnetic Transients Simulations with Voltage Source Converters," *RTDS website www.rtds.com*

[3] H. Dommel, "Digital Computer Solution of Electromagnetic Transients in Single-and Multiphase Networks", IEEE Transactions on Power Apparatus and Systems, 1969, Vol. PAS-88, No. 4. April 1969, pp. 368-399.