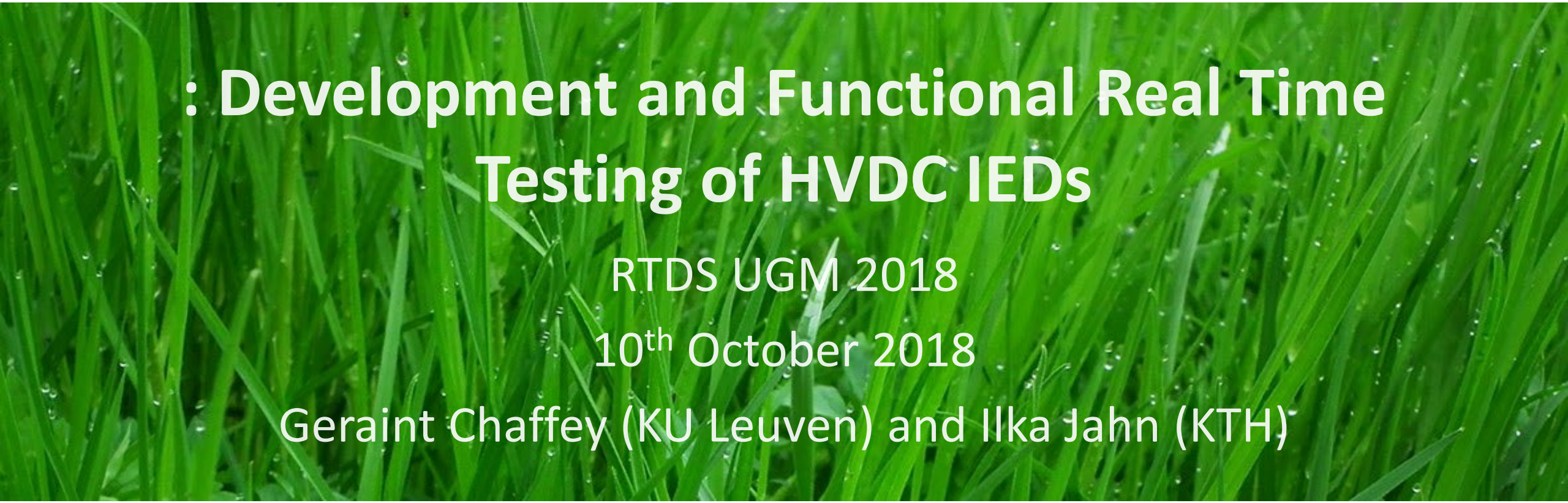


: Development and Functional Real Time Testing of HVDC IEDs

RTDS UGM 2018

10th October 2018

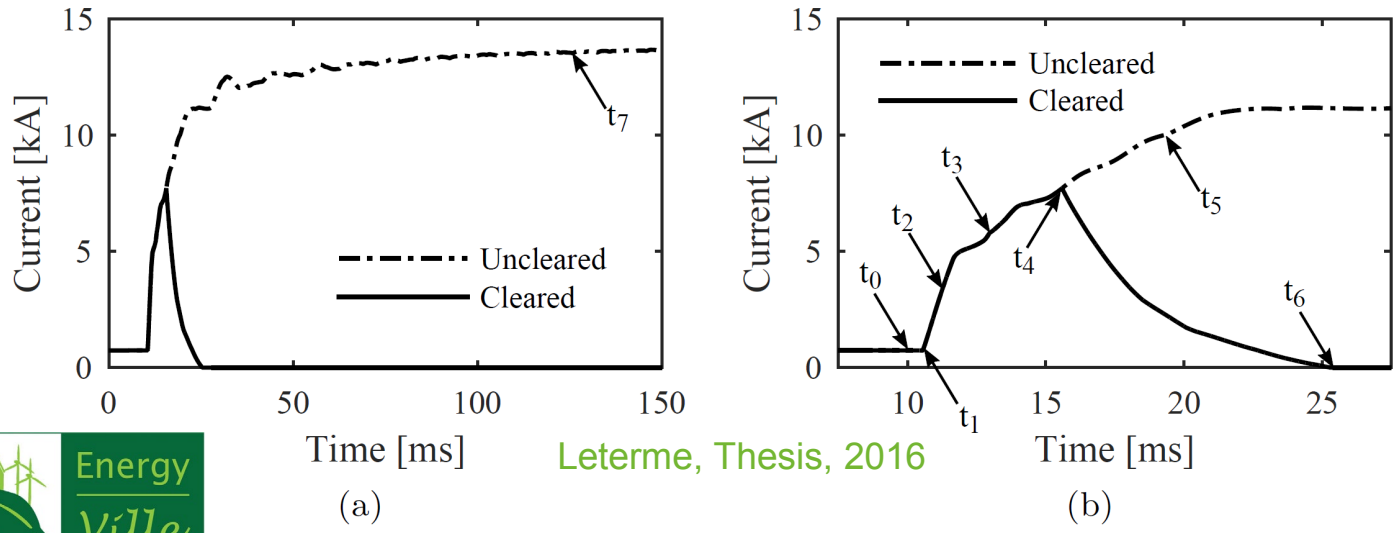
Geraint Chaffey (KU Leuven) and Ilka Jahn (KTH)

Outline

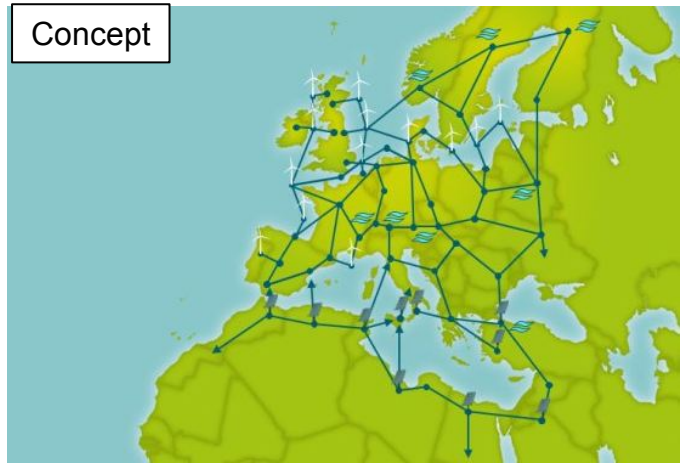
- Introduction to HVDC protection and HVDC IEDs
- IED test procedures
- Hardware IED implementation
- Real time testing with RTDS

Introduction - Protection of HVDC networks

- Future multiterminal HVDC systems demand novel protection equipment
- Expectation of fast protection
  - Detection/discrimination e.g. <1 ms
  - Circuit breaker operation e.g. ≈5 ms (?)



Leterme, Thesis, 2016



Friends Of The Supergrid

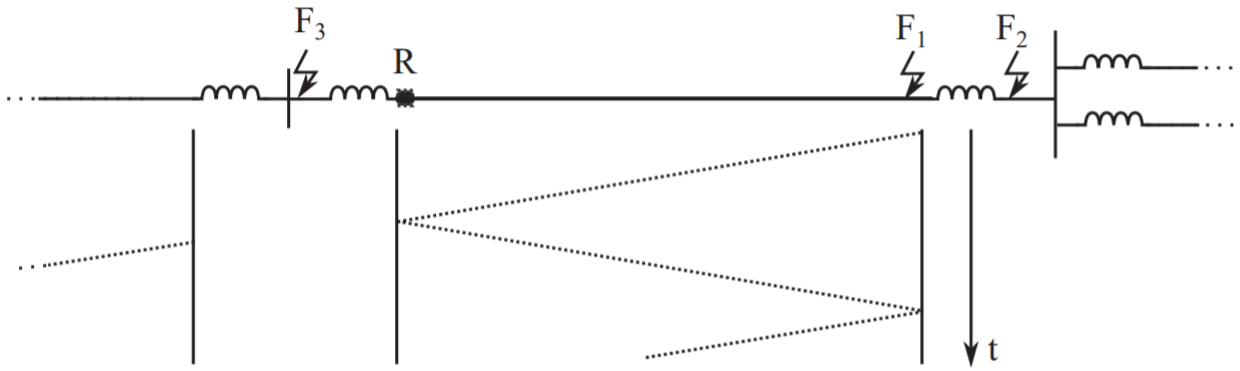
GEIRI, SGCC

Introduction - HVDC IEDs

- Requirement for HVDC IEDs
  - Calculation of protection algorithm(s)
  - Detection, discrimination; primary, backup; robust/reliable; …
  - Much faster operation requirement than typical AC IED
- State of the art HVDC IEDs
  - Advanced algorithms not yet implemented in real systems
  - Requirement for increasing confidence/TRL

Introduction - HVDC Protection Algorithms

- Non-unit protection algorithms
  - Use local voltage and current measurements
  - *Voltage differential (dU/dt)*
  - *Current differential (di/dt)*
  - *Travelling wave extraction (dTW/dt)*
- Unit protection algorithms
  - Use communicated measurements
  - *Travelling wave directional*
  - *Travelling wave differential*



W. Leterme, J. Beerten, D. Van Hertem, “Nonunit protection of HVDC grids with inductive dc cable termination,” IEEE Transactions on Power Delivery, vol. 31, no. 2, pp. 820-828, Apr. 2016.

Introduction – HVDC Protection at KU Leuven/EnergyVille

- PROMOTioN – towards meshed offshore networks
  - Protection of HVDC networks (KUL lead)
  - Development of HVDC IEDs (KTH lead)
  - Testing of protection strategies in MTTE RTDS environment (SSE lead)
- Protection strategies for multiterminal systems
- Circuit breaker and protection strategy co-design
- Protection interoperability and impact
- Development of protection algorithms
- HVDC IED test methods and towards pre-standardisation

PROMOTioN
PROGRESS ON MESHED HVDC OFFSHORE TRANSMISSION NETWORKS

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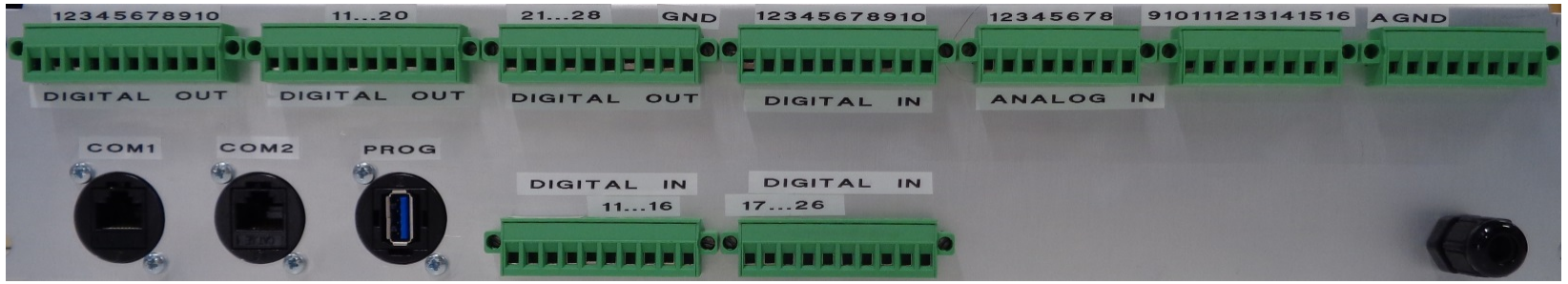
IED hardware



IED hardware

- Main component: Zedboard (off-the-shelf)
- Custom-made peripheral modules (PMOD) for interface with RTDS
- Communication module (off-the-shelf)
- “plug and play”

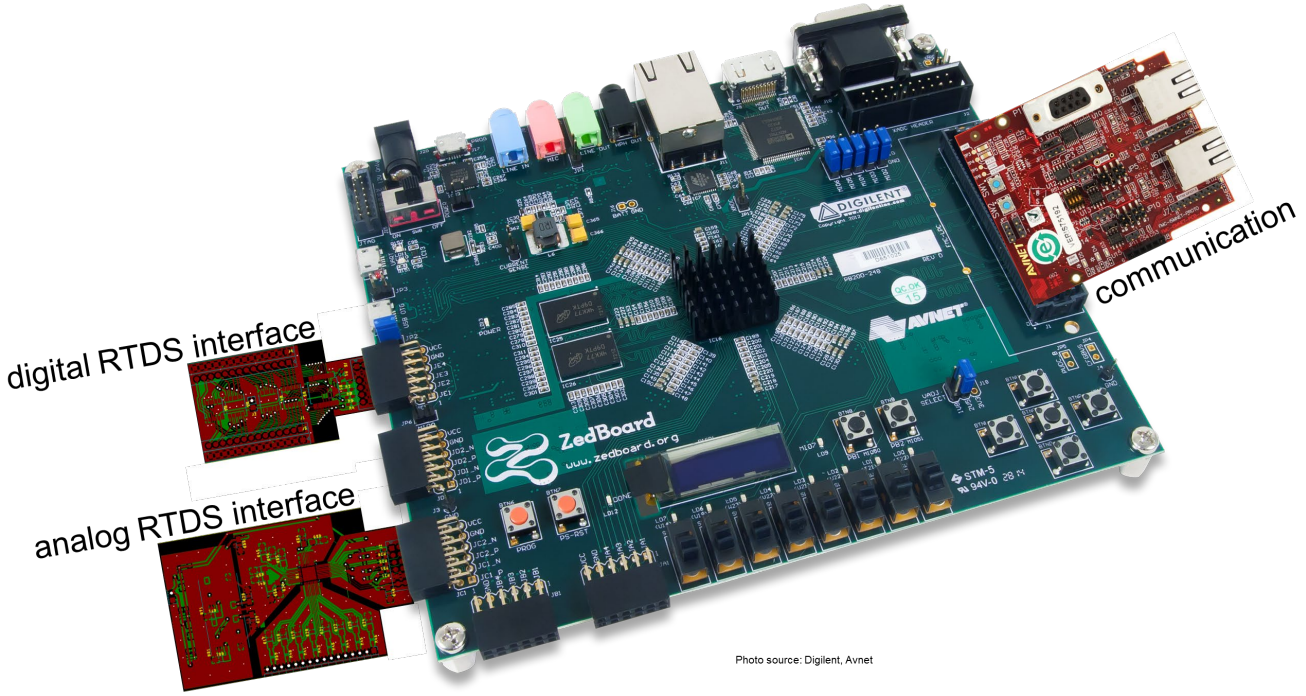


Photo source: Digilent, Avnet

IED software - algorithms

- Primary
  - Voltage / voltage derivative ✓ (+ current direction) ✓
  - Current / current derivative ✓
  - Traveling wave extraction ✓
  - Undervoltage ✓
  - Overcurrent ✓
  - Directional comparison (double-ended) (✓)
  - Differential (double-ended) (✓)
- Backup
  - Breaker failure
  - lokal
- Busbar
  - Sum of currents ✓
- Realtime Ethernet for substation communication (✓)
- 2/3 option

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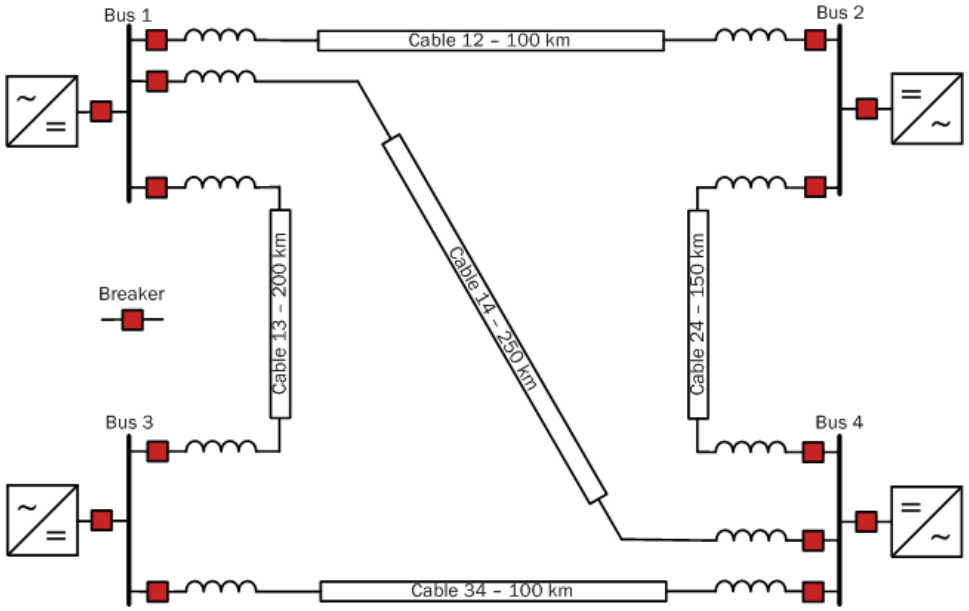
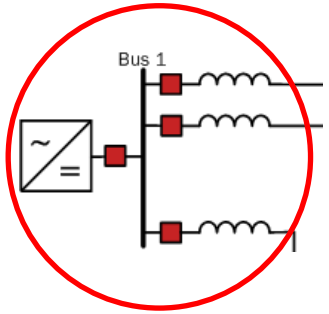
IED software – substation communication

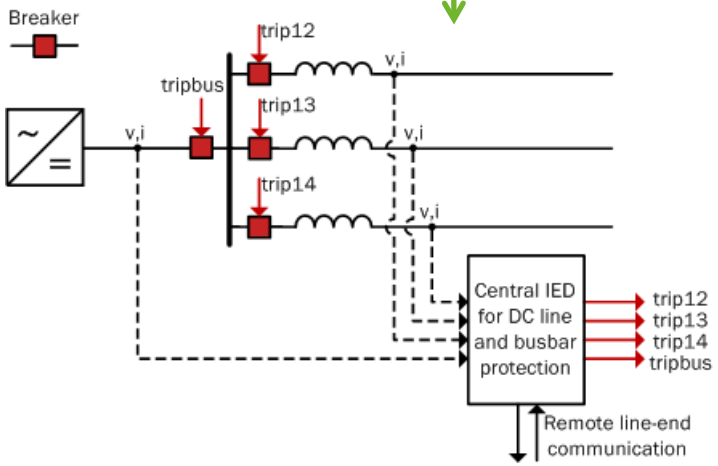


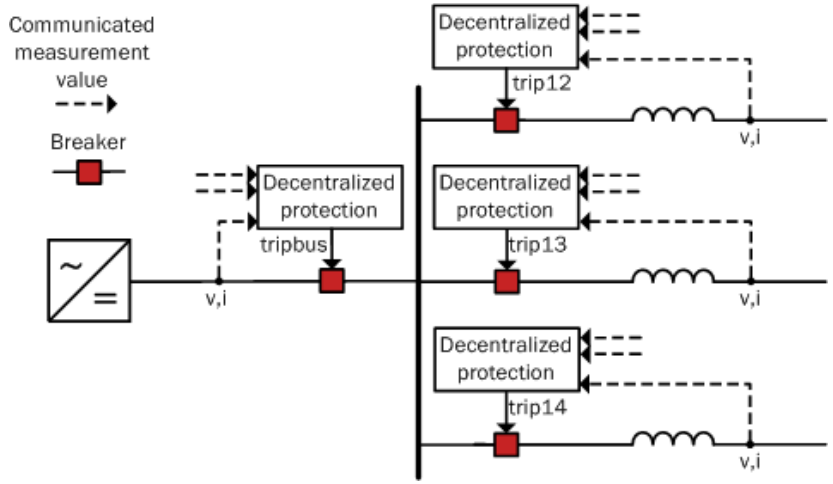
IED software – substation communication



Many decentral protection IEDs

Central protection IED

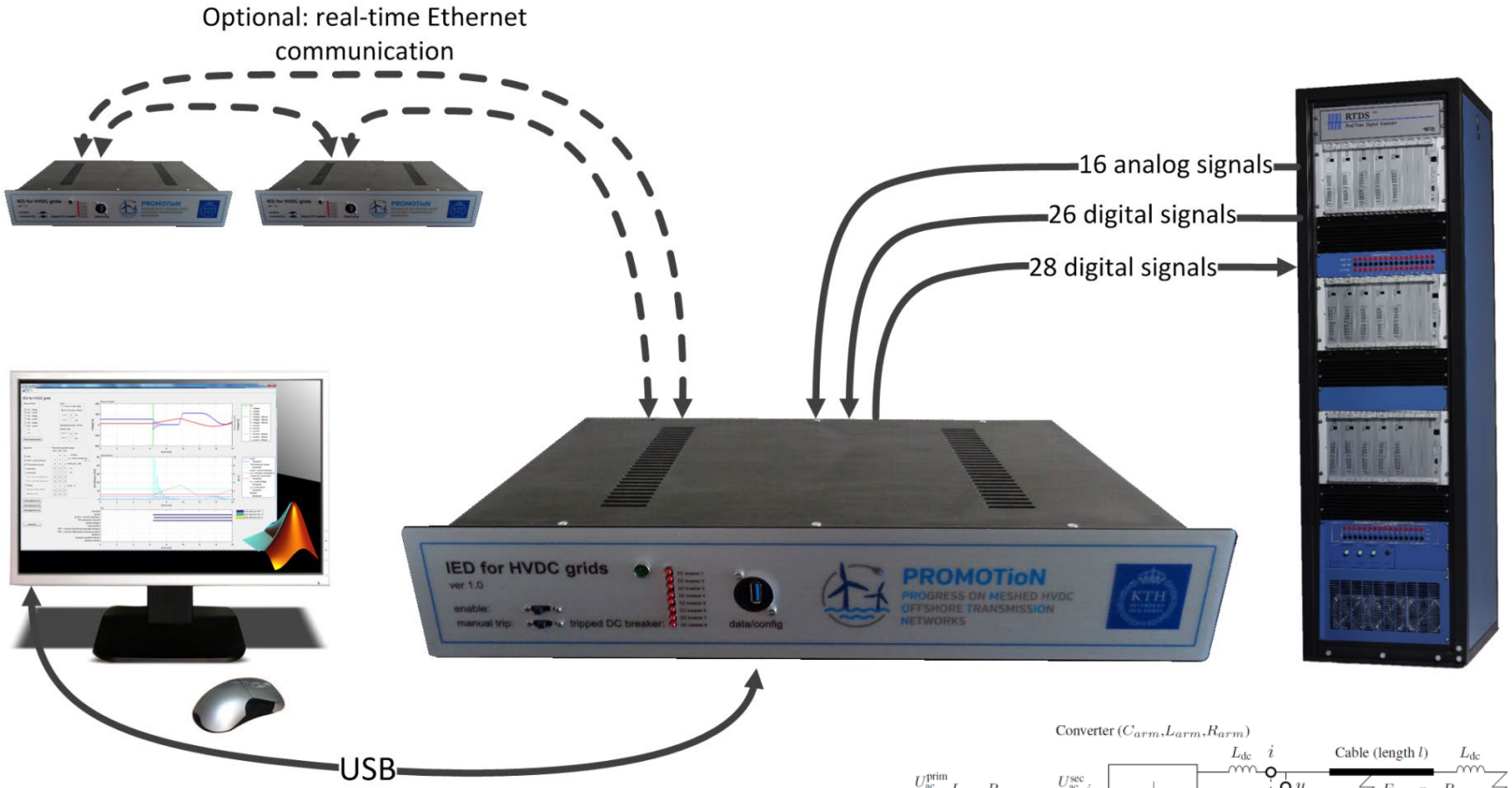


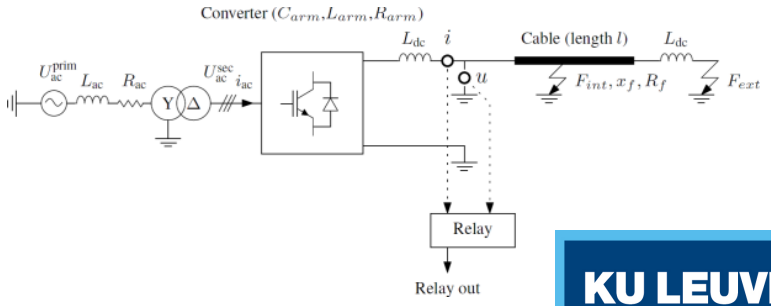


Communication for decentral protection

- **Standardized realtime Ethernet**
- **Vendor-interoperability**

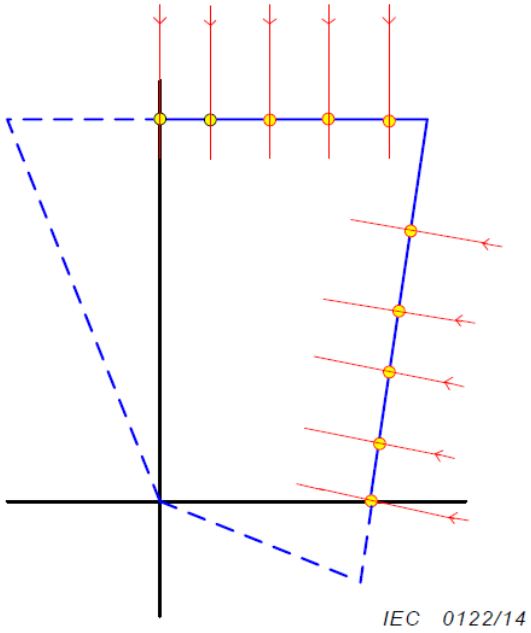
Test with RTDS



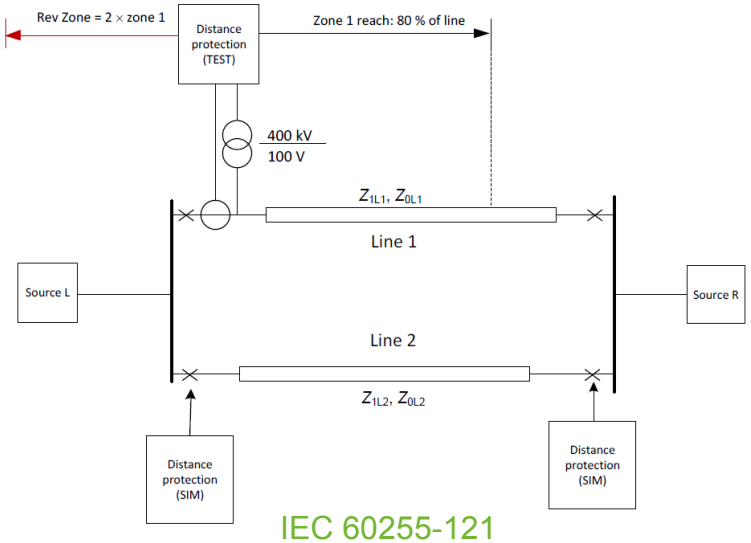


Standardised testing of AC IEDs

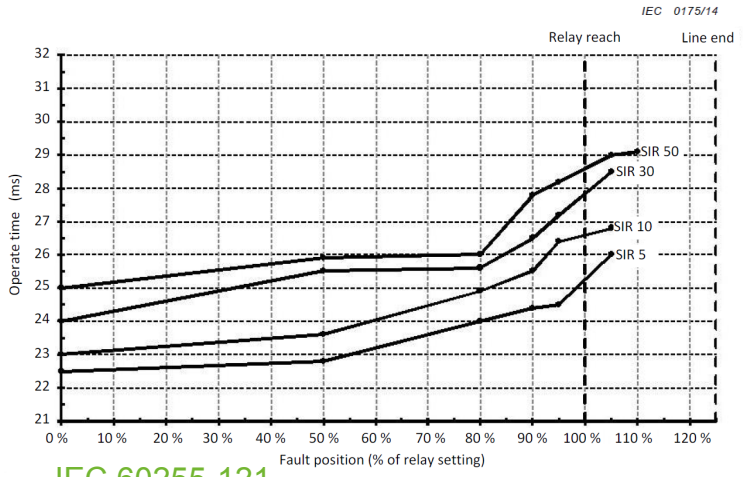
- AC IEDs have well developed standards:



IEC 60255-121



IEC 60255-121



IEC 60255-121

NETWORK PROTECTION & AUTOMATION GUIDE

Protective Relays, Measurement & Control

Relay Testing and Commissioning

21.1 Introduction
21.2 Electrical Type Tests
21.3 Electromagnetic Compatibility Tests
21.4 Product Safety Type Tests
21.5 Environmental Type Tests
21.6 Software Type Tests
21.7 Dynamic Validation Type Testing
21.8 Production Testing
21.9 Commissioning Tests
21.10 Secondary Injection Test Equipment
21.11 Secondary Injection Testing
21.12 Primary Injection Tests
21.13 Testing of Protection Scheme Logic
21.14 Tripping and Alarm Annunciation Tests
21.15 Periodic Maintenance Tests
21.16 Protection Scheme Design for Maintenance

Network Protection and Automation Guide, Alstom Grid, 2011

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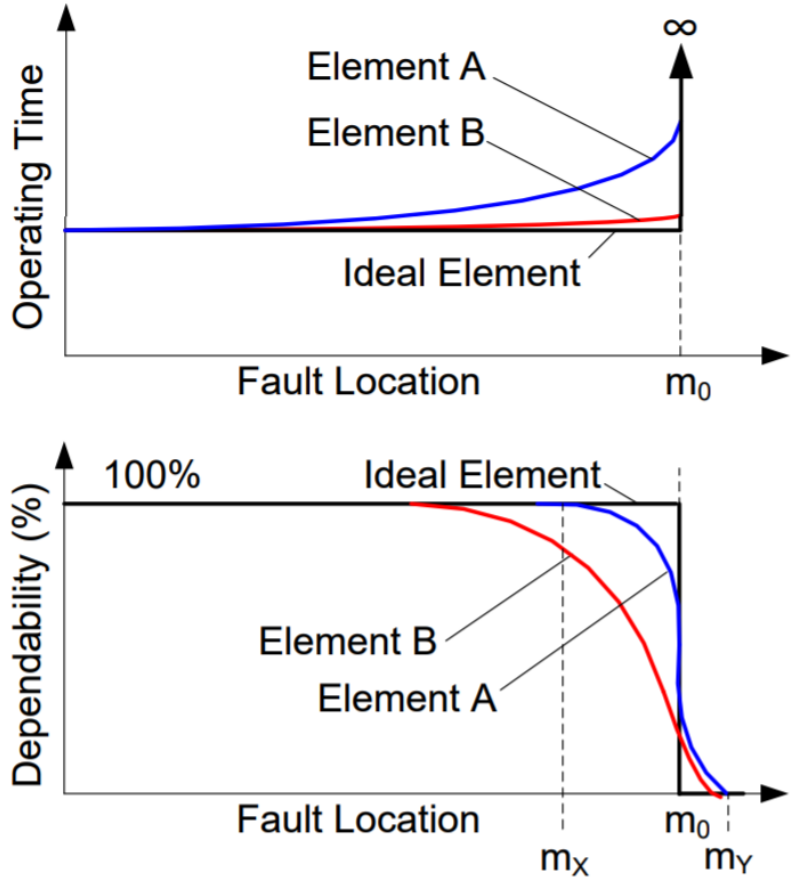
Towards Standardised Testing for HVDC IEDs

- Standardised tests will be required for future HVDC IEDs
- Such tests are not well defined
- Requirements quite different to existing AC IED testing
- KUL/EnergyVille are developing the required ‘dynamic validation type tests’
- Testing planned of academic and industrial IEDs

IED Testing – Terminology and Measuring Success

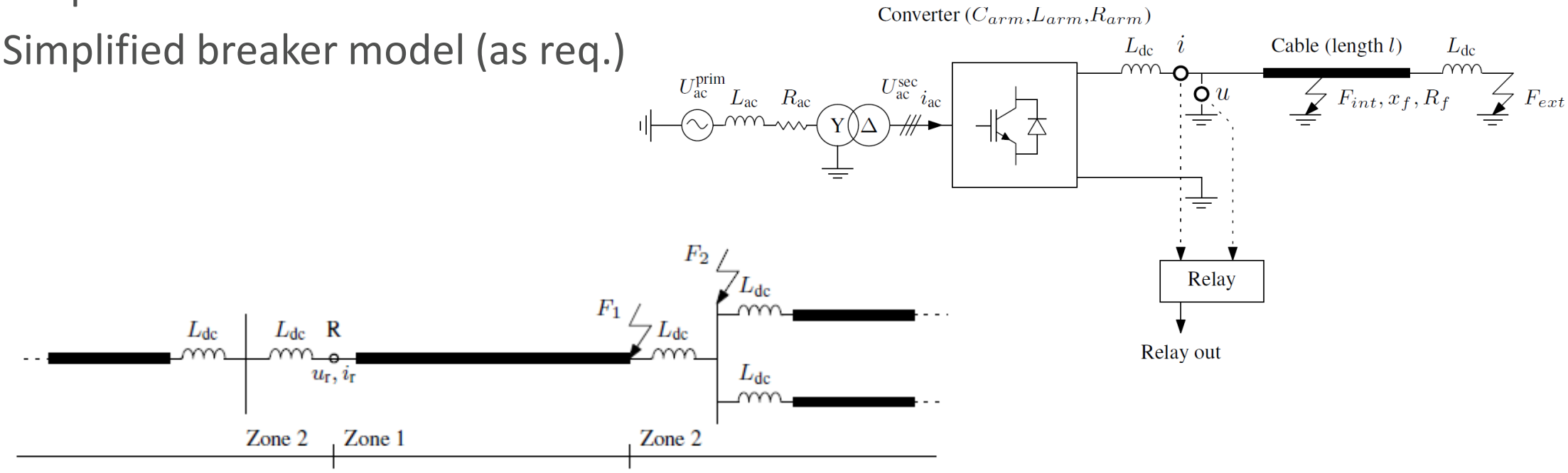
- Dependability
  - IED operates for a fault in the protection zone
- Security
  - IED does not operate for a fault outside the protection zone
- Selectivity
  - Correct IEDs within system operate to isolate fault



E Schweitzer et al. "Defining and Measuring the Performance of Line Protective Relays" 43rd Annual Western Protective Relay Conference, 2016.

IED Testing – Test Circuit Requirements

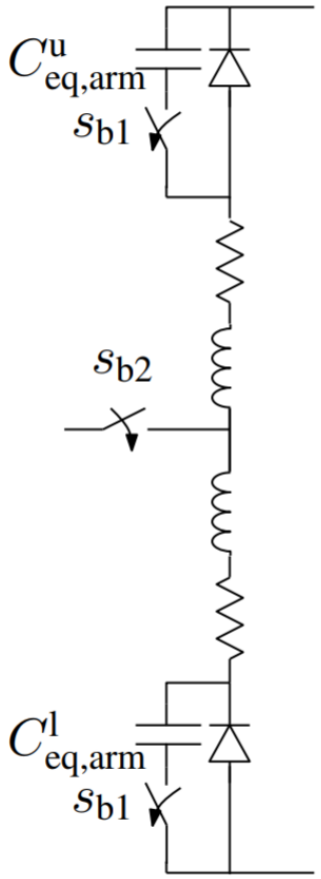
- System can be represented by simplified network
  - 1 to 4 cables is sufficient
  - Simplified converter model
  - Simplified breaker model (as req.)

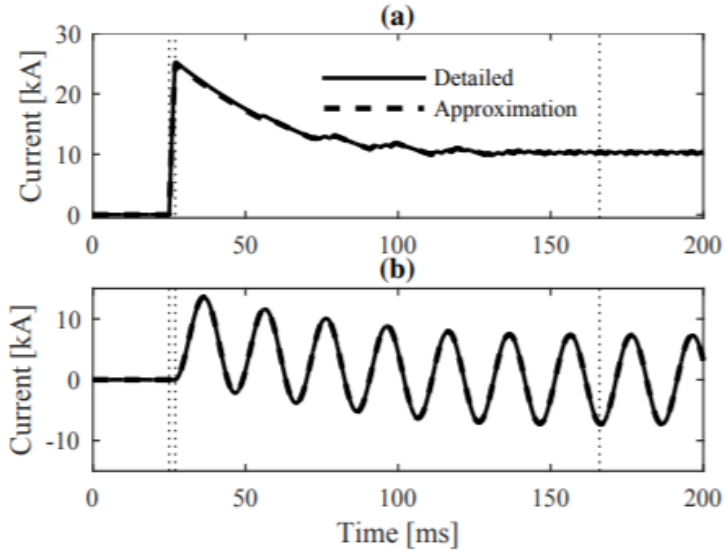


Real Time Testing with RTDS – Modelling

Modelling and application to HVDC protection studies

- MMC:
  - Detailed representation of each SM – CPU or FPGA – ✓
  - Reduced representation of each SM – CPU or FPGA – ✓
  - Reduced model, representation of each valve – CPU – ✓
  - DC source and equivalent impedance – CPU ✘





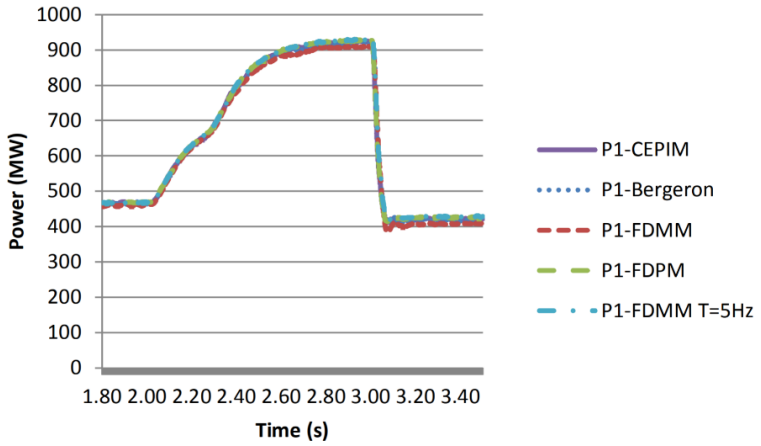
Reduced order MMC model for HVDC fault studies

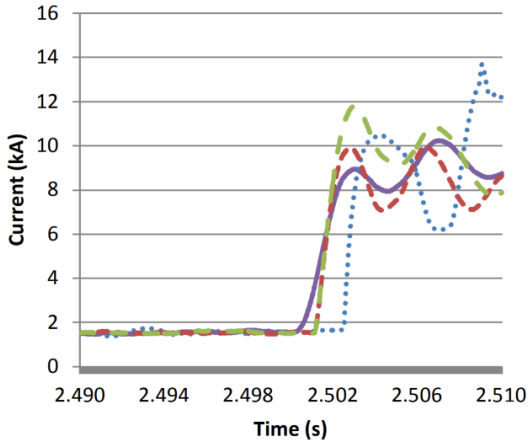
W. Leterme, J. Beerten and D. Van Hertem, "Equivalent circuit for half-bridge MMC dc fault current contribution," *2016 IEEE International Energy Conference (ENERGYCON)*, Leuven, 2016, pp. 1-6.

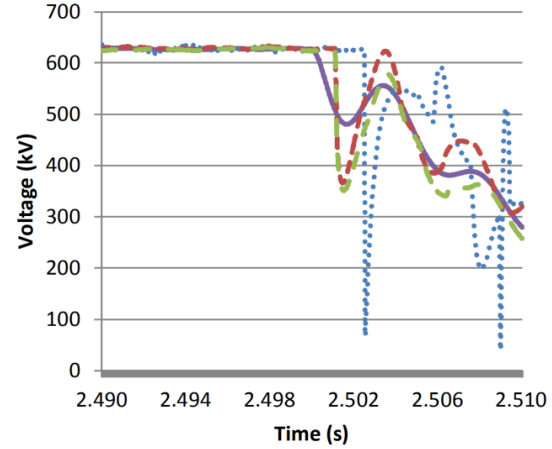
Real Time Testing with RTDS – Modelling

Modelling and application to HVDC protection studies

- Cable
  - Pi section (CPU) – ✘
  - Bergeron (CPU) – ✘
  - FDPM (FPGA) – ✓





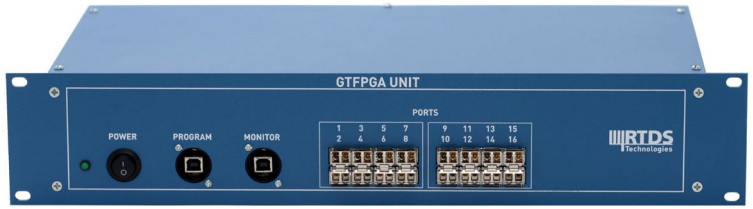


A. Beddard and M. Barnes, "HVDC cable modelling for VSC-HVDC applications," 2014 IEEE PES General Meeting | Conference & Exposition, National Harbor, MD, 2014, pp. 1-5.

Real Time Testing – Modelling Choices

For evaluation of HVDC IEDs (minimum complexity):

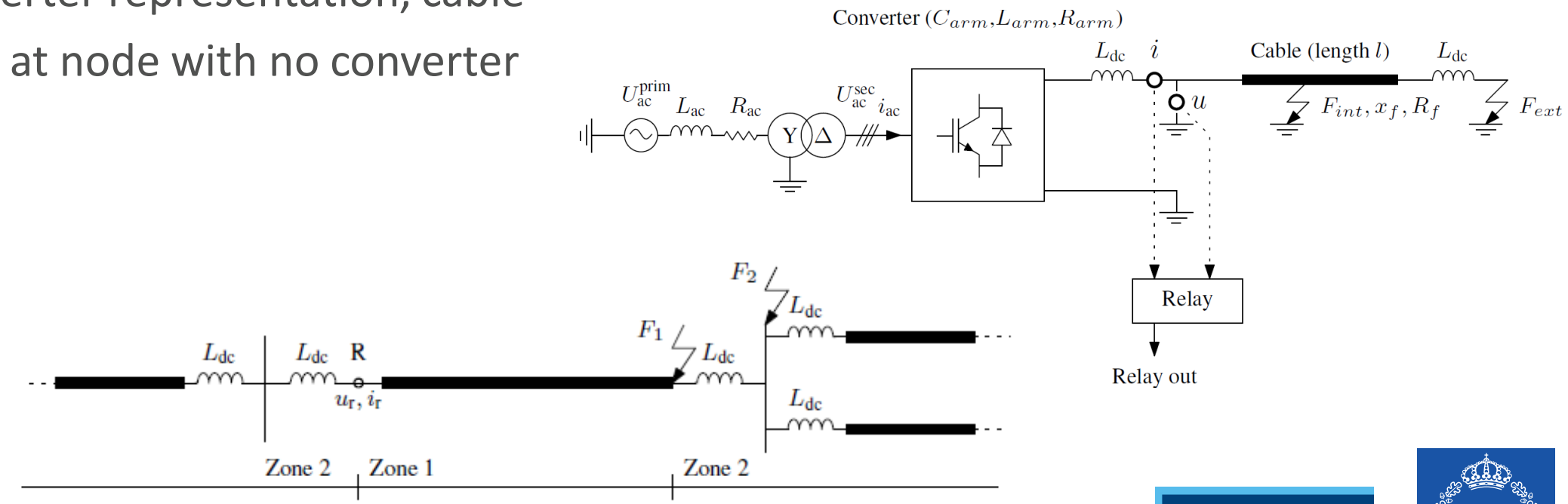
- Converter Model
  - Reduced order model for fault studies -> PB5 card
- Cable model
  - FDP line -> GTFPGA (present)
  - TWRT -> GTFPGA (future)
- Circuit breaker model:
  - Switch + MOV (suitable for network studies) -> PB5 card



Real Time Testing with RTDS – Preliminary Test Results

Test circuits/procedures for initial tests

- Varying: Fault location, fault impedance, protection algorithm, …
- Test circuit:
  1. Converter representation, cable
  2. Fault at node with no converter



Conclusions

- Real-world implementation of HVDC protection algorithms are of ongoing research interest
- RTDS applied for testing state-of-the-art HVDC protection IEDs
- PROMOTioN HVDC IED developed and initial testing complete
- Test procedures under ongoing development, working towards standardisation

- … more information in the lab tour/demo!

HVDC IED testing at EnergyVille

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