



Your world in real time.

RTDS
Technologies

RTDS.COM

New Developments on RTDS

On UGM China
October 17, Beijing



Outlines

1. Hardware Development
2. Architecture of Multi-rate Simulation: Superstep-Mainstep-Substep
3. Predictive Resistive Switching Algorithm
4. FPGA Development: GPES, MMC and TWRT
5. TRI – Hybrid Simulation
6. Electric Machine and Transformer
7. Other New Models
8. PHIL
9. New Features in RSCAD Software
10. PSCAD to RSCAD Conversion
11. P&A Updates
12. Improved Documentations

NovaCor: Hardware Platform



Existing rack structure replaced by single board!

Terminology: Rack -> Chassis

Background of NovaCor

- Existing rack structure with VME backplane has been in place since the early 90s
- Continuous advancements and an upgrade path has been provided to customers
 - TPC → 3PC → RPC → GPC → PB5
 - WIC → WIF → GTWIF
 - Backplane 175 ns → 125 ns → 60 ns → Fibre Enhanced Backplane (FEB)
- Backplane communication time is a limiting factor in the existing design
 - Communication of variable admittance elements to network solution and monitoring variables
 - Backplane communication could account for 30-50% of the timestep
- Customers are making excellent use of existing racks
 - RTDS Technologies will continue support for all equipment covered under maintenance
 - Sales of GTWIF/PB5-based simulators will continue indefinitely

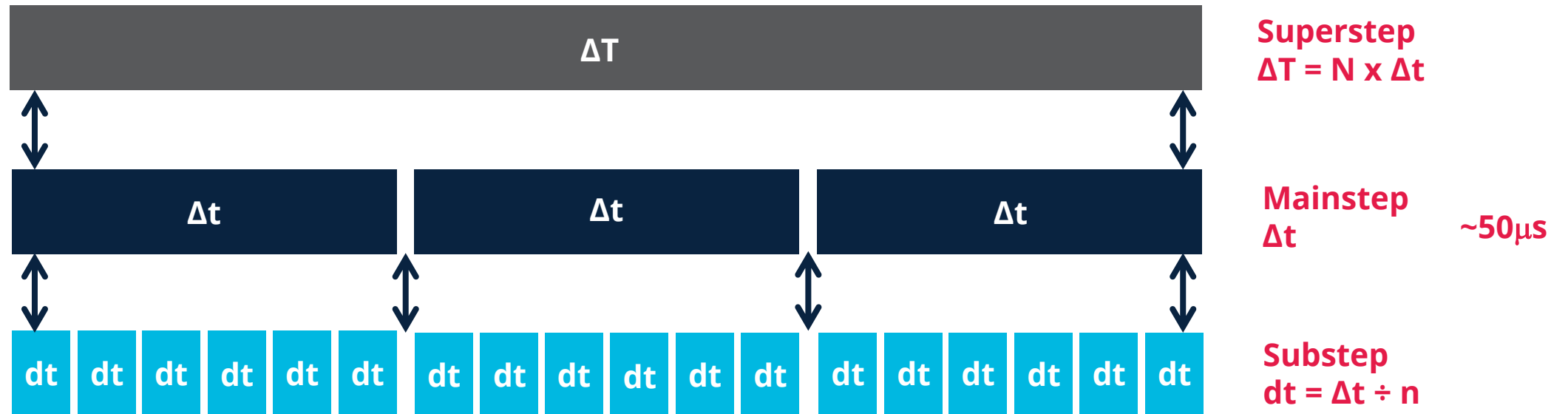
Design Philosophy Remains: **Bare Metal Design**

- RTDS Simulator hardware completely redesigned
- Nova = New.....NovaCor™ → new core of the RTDS Simulator
- Designed around IBM's POWER8® RISC-based 10-core processor
 - OpenPOWER Foundation provided access and support
- Clock speed increase: 1.7 -> 3.5 GHz!
- Backplane eliminated by fast, on-chip, core-to-core communication

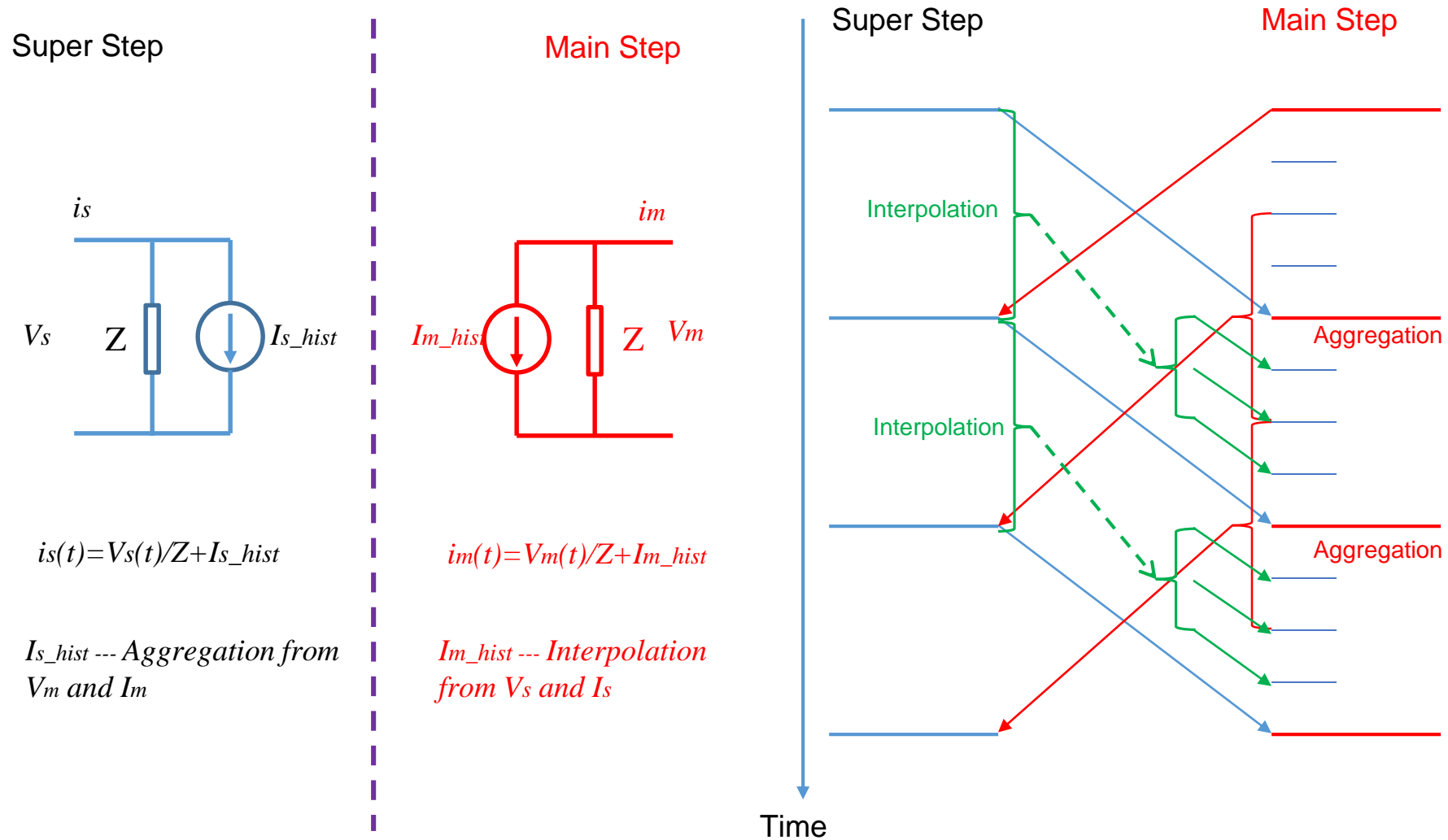
The **custom designed real time simulation hardware** is the only way to fully use the computation power of the available processors

Multirate Simulation

- The current multirate framework that we have with the NovaCor can largely be described by the following diagram:

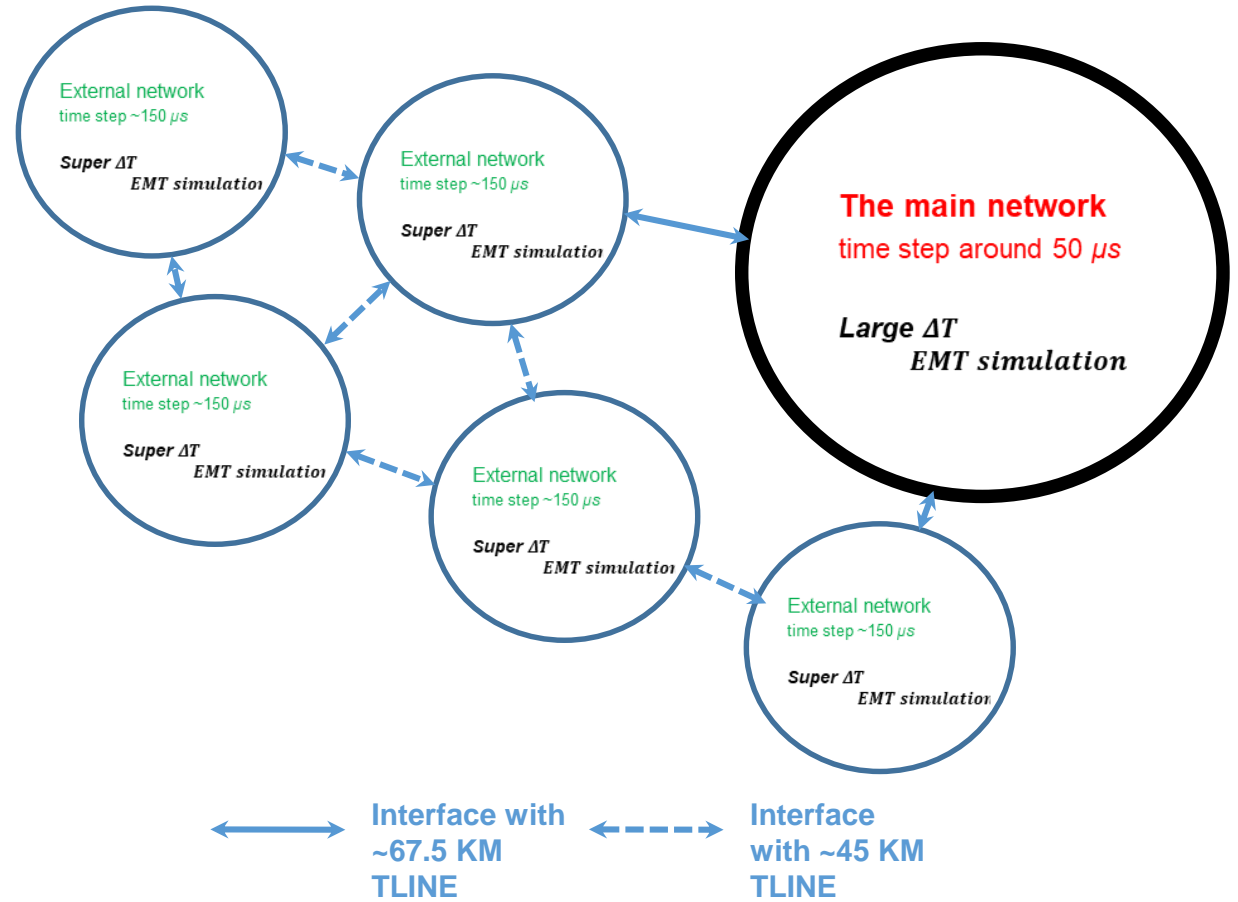
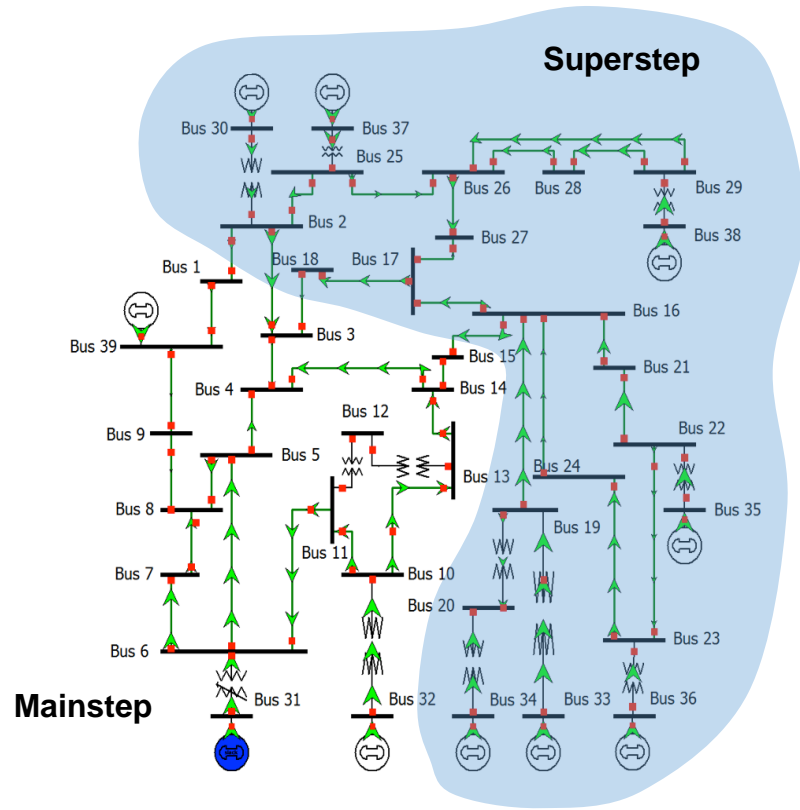


Multirate Transmission Line Solution



Superstep Solution – Modelling External Network

Larger network in less detail, but still EMT



Substep Simulation – An improved small dt solution

- The processing power of our latest hardware has allowed us run the conventional EMTP algorithm in real time using timesteps of 1-10 μ s.
- The solution can compute a matrix inversion and is more flexible.
- **LC switching can be abandoned in many cases.**
- **No interface lines required for use of bridges with resistive switching.**
- **No limit on the number of resistive switching elements**
- **Model developed with Cbuilder – User Defined Small Time Step Model Be Possible**



Predictive Resistive Switching

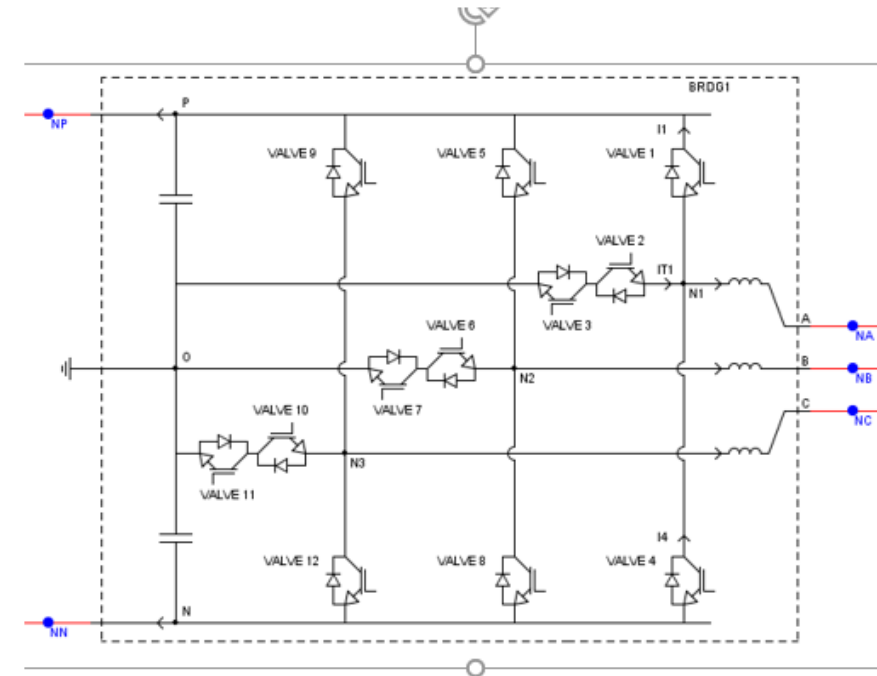
Assumptions:

- Weak electrical interaction between switch devices from different legs
- Strong electrical interaction between switch device within a leg
- As a results, predictive ON/OFF statuses can be predicated separately for each leg

Predictive resistive switching is a method of predicting the ON/OFF statuses of switches in a VSC for the next time step when switched resistances are used

Procedure of predicting the switching status:

1. Solve the circuit and get a preliminary solution of each node voltage
2. Calculate each branch voltage
3. Predicting the switching status according to the branch voltage



New Network Solution

➤ Network solution

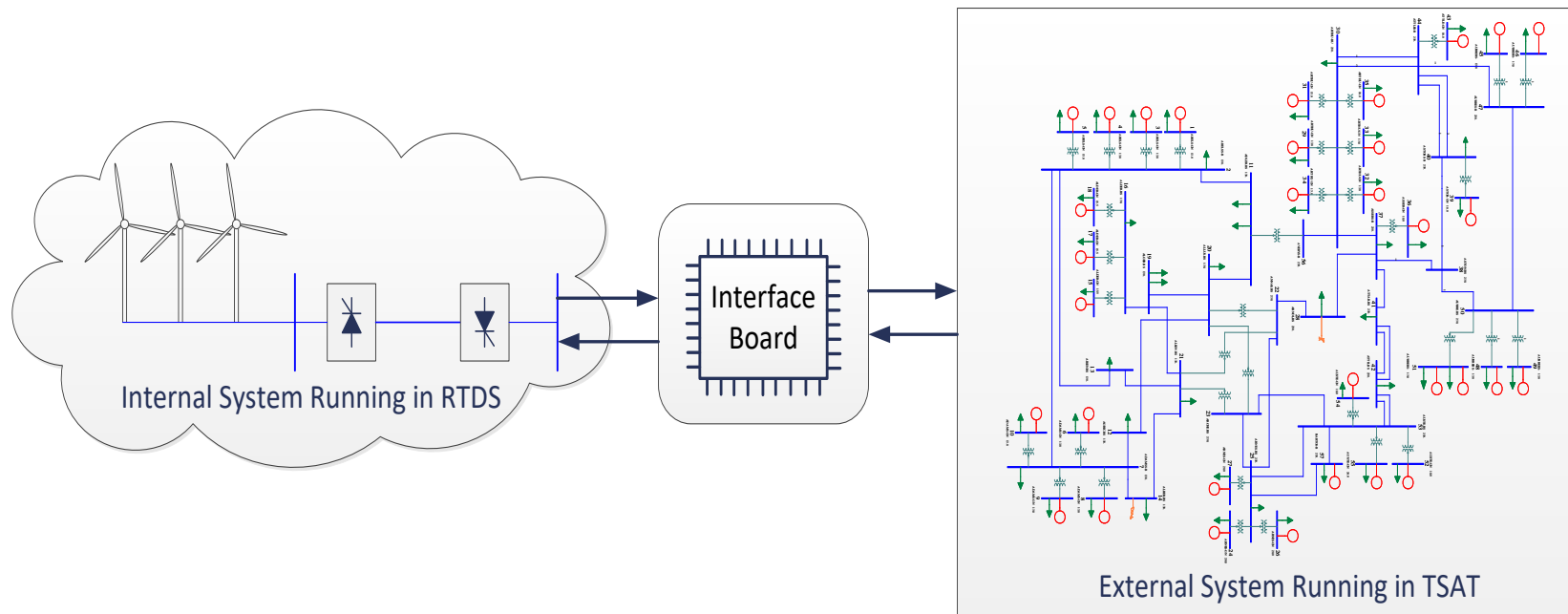
- NovaCor currently allows 2 x 300 nodes per chassis
 - 2 network solutions separated by traveling wave models
 - 2 cores for 2 x 300 nodes
- NovaCor upgrade in development for 1 x 600 nodes per chassis
 - 1 network solution with 600 nodes with no requirement for separation by traveling wave models
 - 2 cores for 600 nodes



Hybrid EMT / RMS Simulation

TRI - TSAT-RTDS Interface

- Combine RTDS® EMT simulation and TSAT™ RMS simulation in real time
- TSAT running on PC at 4-5ms timestep with up to 10000 buses
- Multi-port interface supported



GTFPGA-GPES

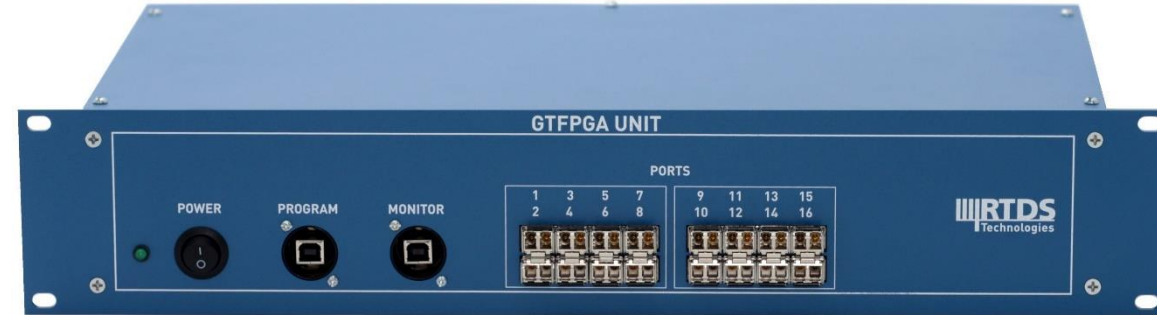
➤ Capability (on VC 707)

- Used for large power electronics circuits
- Freely configurable
- Maximum 128 nodes, 256 branches
- Time-step 230 ns -> 2 us

➤ Components

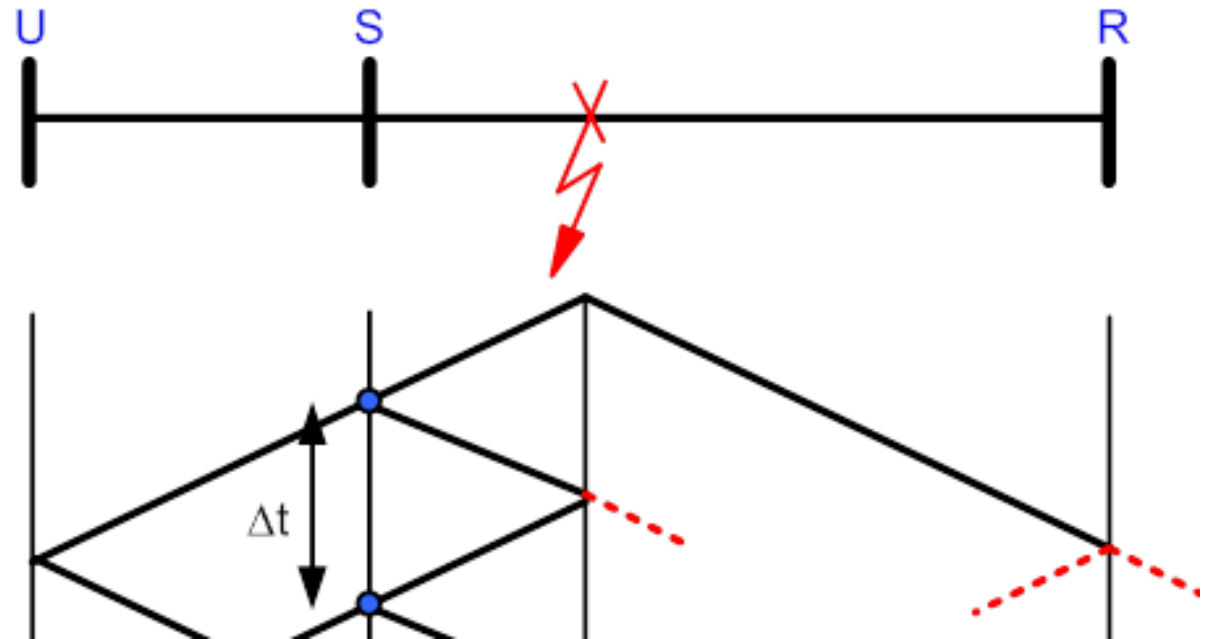
- RLC, switches, single phase transformer, source, Bergeron Interface Tline
- Direct I/O connection for 4 x GTDI and 2 x GTA0
- 2- and 3-phase coupled inductors (chokes) being added

- ## ➤ The Performance Can be Doubled if using Large FPGA (e.g. VCU 118)
- Smaller time step and large Circuit (such as 256 nodes and 512 branches) is possible to achieve



Traveling Wave Relay Testing

- Frequency dependent transmission line models
 - ~2 microsecond timestep
 - NovaCor for flexible topology through Substep
 - GTFPGA (limited configurability)



MMC Based HVDC Simulation

Latest Development

V2 – VC707 FPGA board

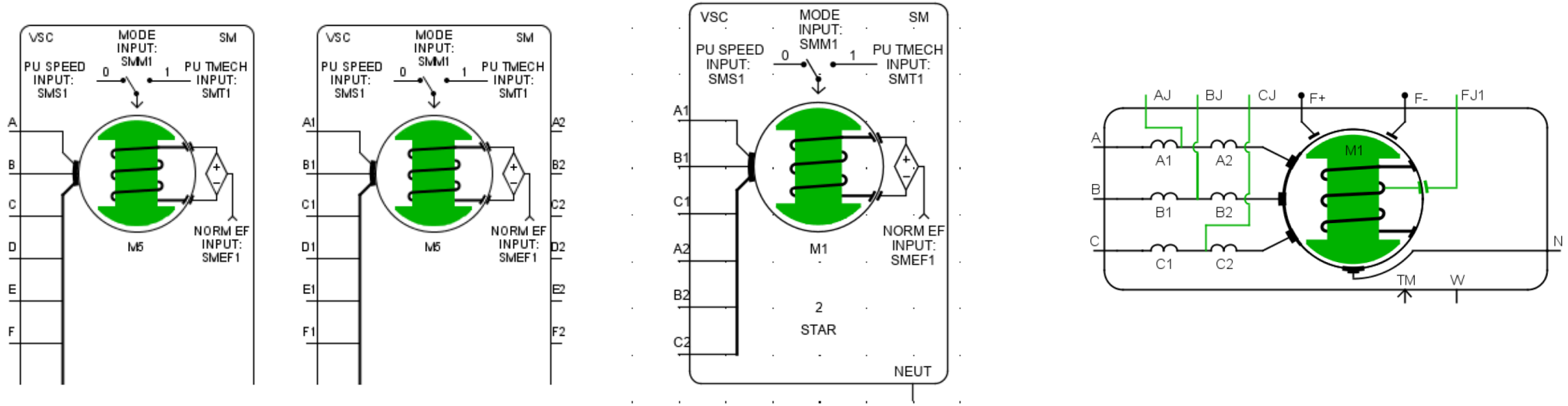
- GM/GMT3 Model with 1024 SM, potentially for MMC UHVDC
- GM/GMT3 with mixed full and half bridge SM
- GMT3 with internal grounding fault
- CDSM – Clamped Diode Sub Module
- Available Internal Faults
 1. Any individual or multiple SM short circuit;
 2. Any individual or multiple SM capacitor partial short circuit;
 3. The arm reactor partial shorts;
 4. The SM parameters (C_{cap} and R_{disch}) are can be individually given;
 5. Grounding faults from any internal point of the valve arm;
 6. Inter-arm faults.



Electrical Machines

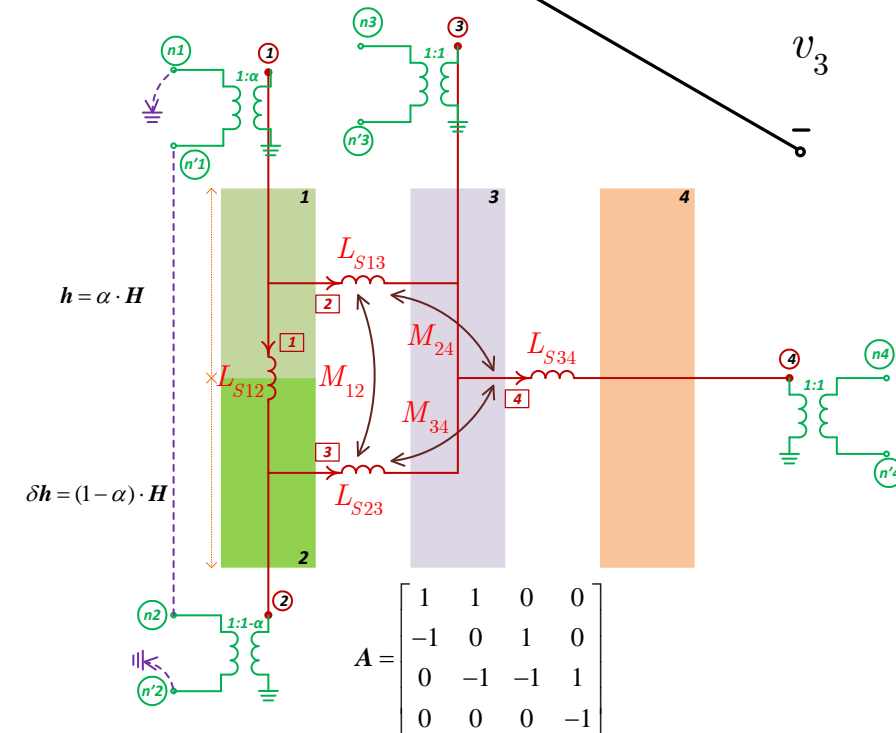
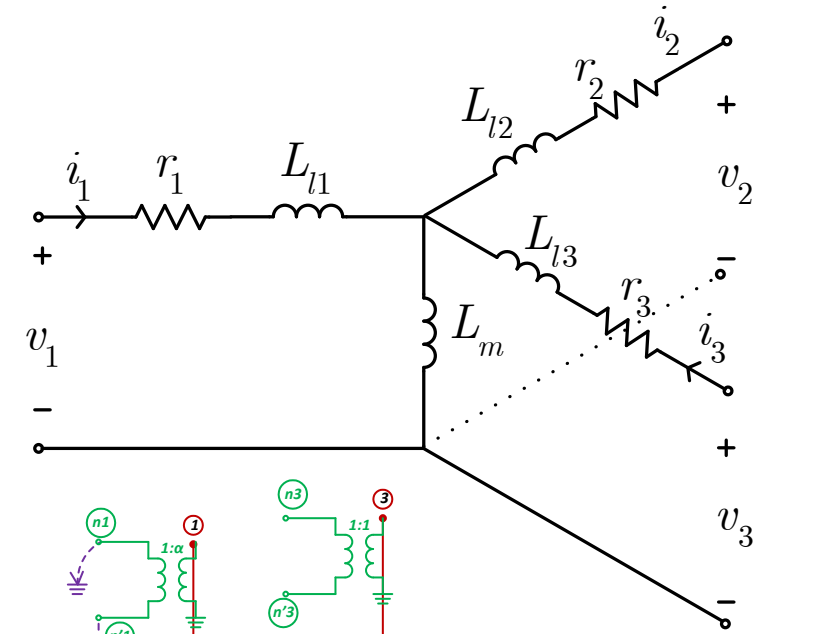
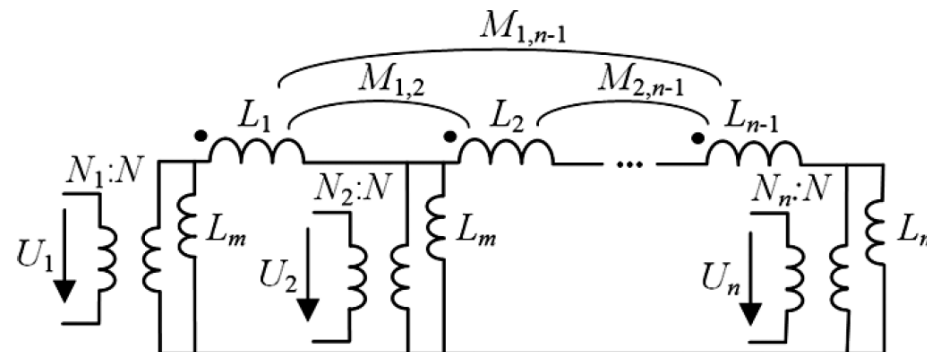
Electrical Machine

- *Multiphase machine models and Synchronous machine model with more faults*
- *Dual stator synchronous machine*
- *Machine model with parallel winding and internal faults*



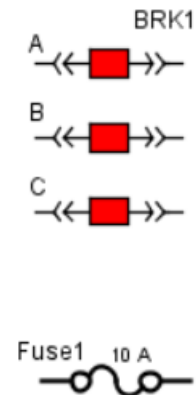
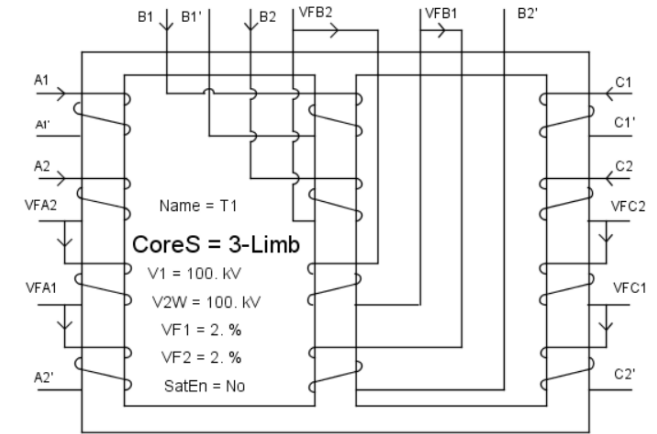
Faulted Transformer

- Currently the faulted transformer is modelled by splitting the fault winding into 2 winding.
- Negative Leakage often happened in the Star Equivalent Circuit of a 3-Winding Transformer.
- If the faults happens on the winding with negative impedance, it causes divergence.
- Terminal-Duality Equivalent Circuit Model is developed to solve the faulted transformer.

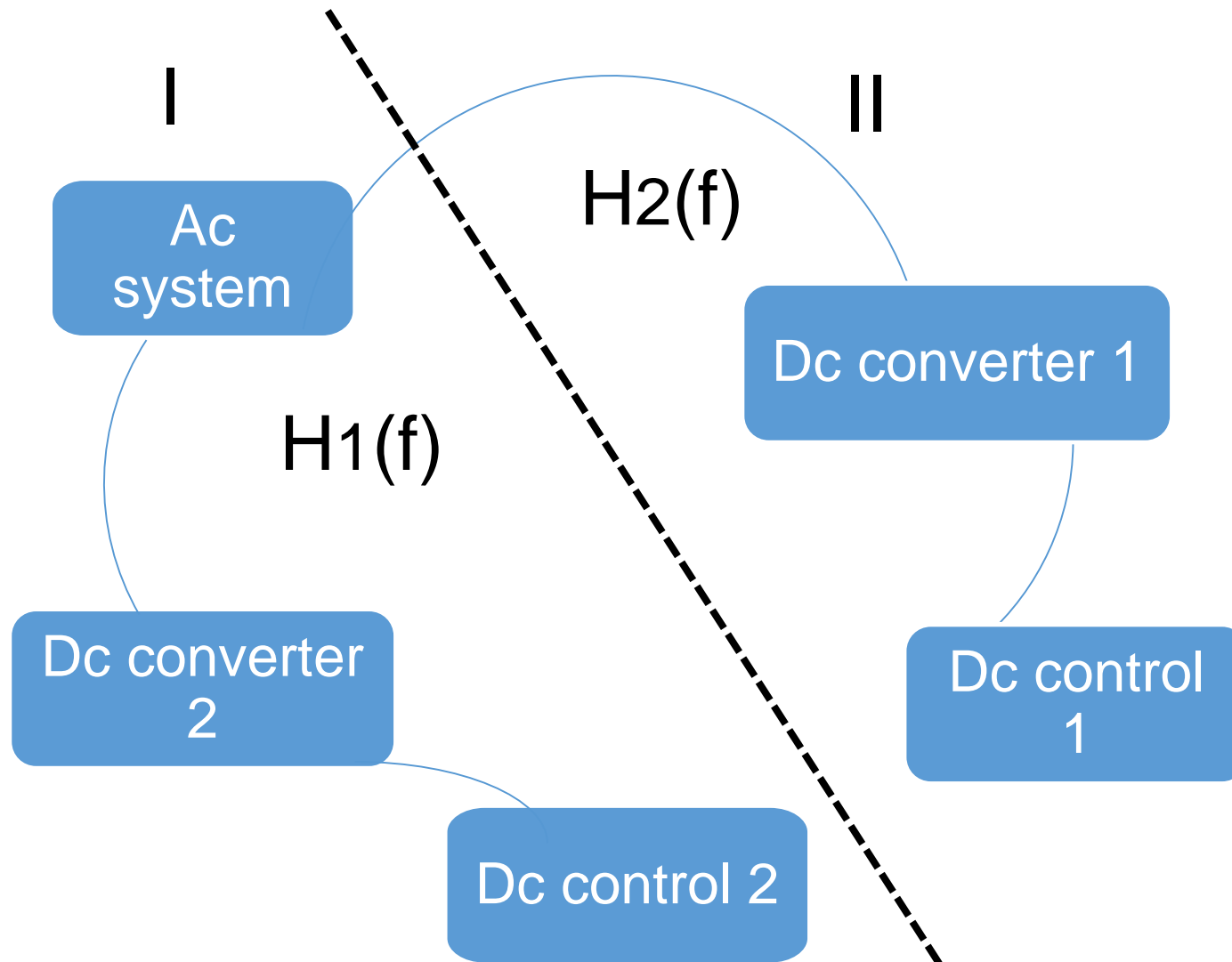


Other New Models in RSCAD

1. 3-phase, 4 winding UMEC model - Configurable as 2 or 3 winding model with fault
2. Fuse model - Medium voltage fuse with 5 different current ratings
3. New breaker model - Embedded disconnects with interlocks, Built in breaker status, Optional pre-insertion resistor
4. Scott transformer for rail systems
5. Improved arrestor model with VI curve input, in large and small time step
6. Improved Zigzag transformer
7. Improved load model with internal frequency measurement
8. Controllable P/Q source
9. Transformer model with saturation branch in middle
10. Multiple PI model with load in between – for distribution network



Frequency Scanning and Stability Analysis



- It is a post-analysis of the simulation results, help to look deep inside by analyzing the simulation results
- Here the system is cut into I and II (for example);
- Conduct frequency scanning and obtain a transfer function
- General Nyquist Method is used to determine the stability boundary and margin

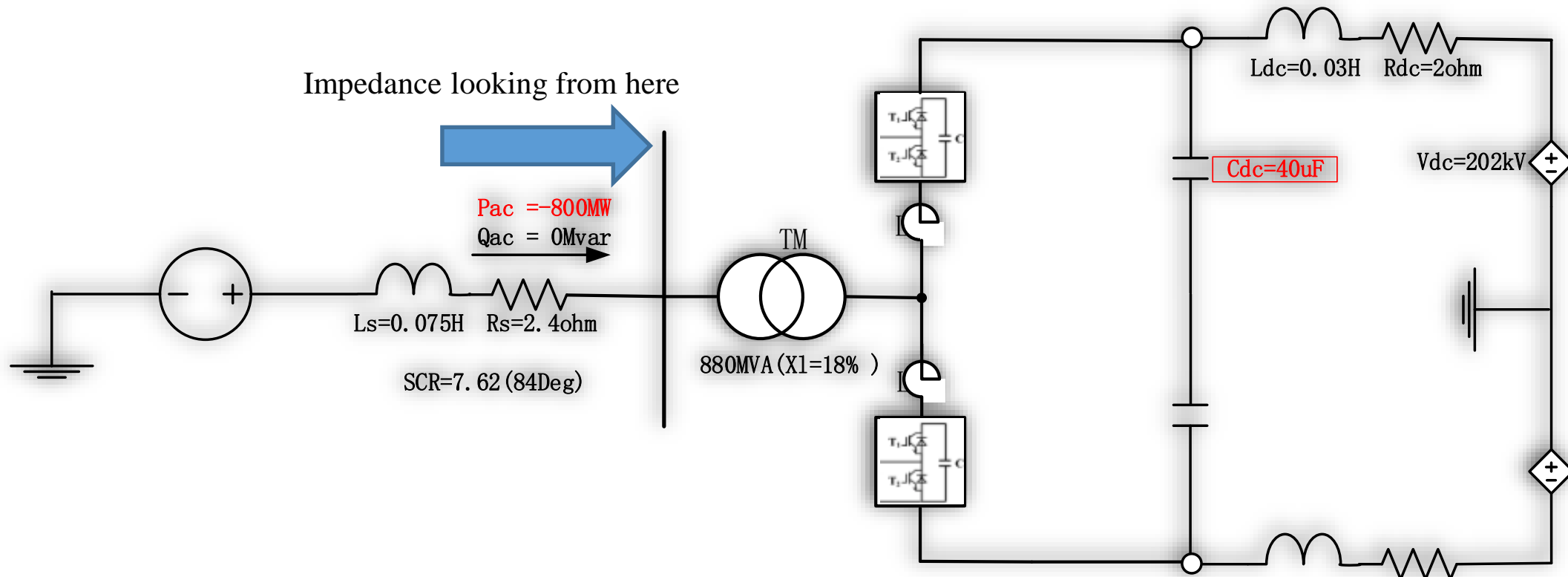
CIGRE DCS1 Stability Analysis

MMC and AC System Interaction

- ❖ (1) Sub-synchronous Interaction
- ❖ (2) High Frequency Interaction

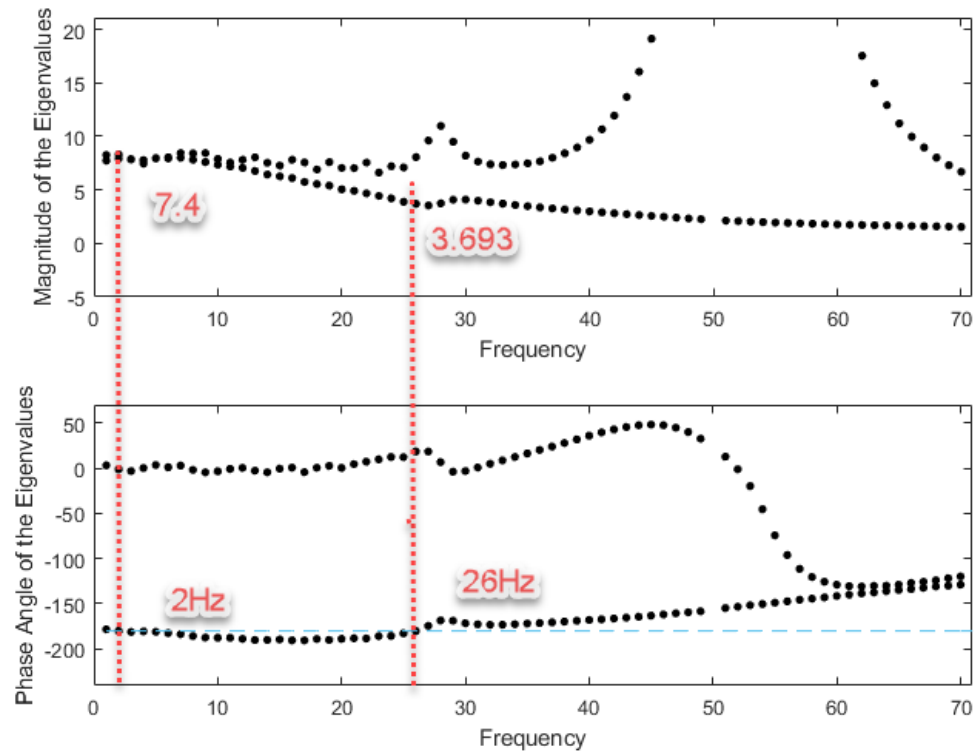
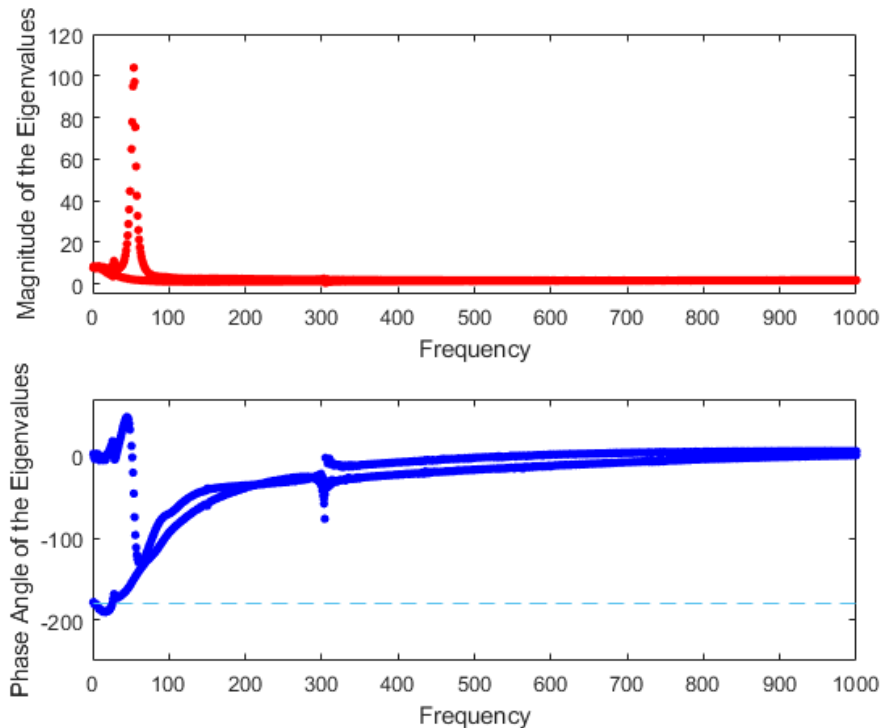
Operation Mode:

- ❖ AC active power and reactive power control
- ❖ $P_{ac_ref} = -800MW$; $Q_{ac_ref} = 0Mvar$



CIGRE DCS1 Stability Analysis (1)

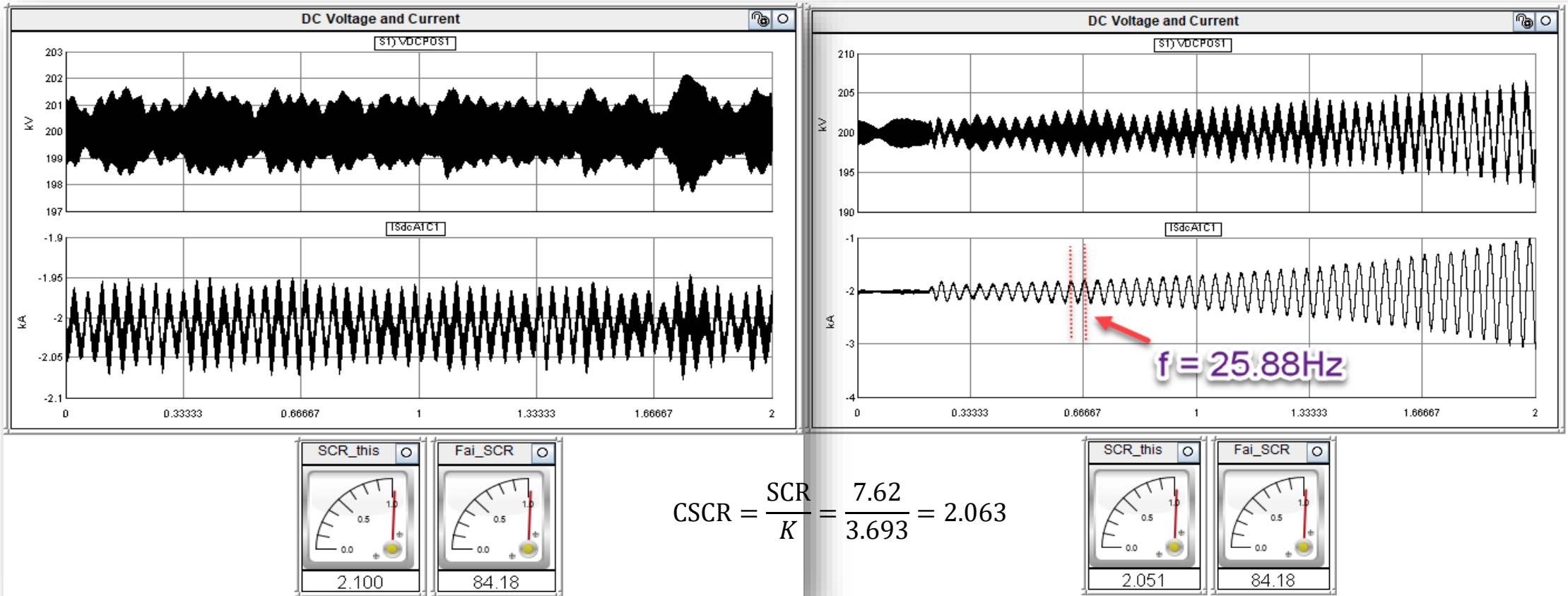
Yac(s)Zmmc(s) Eigenvalue Bode Plot



The magnitude margin: @26 Hz is 3.693; @2 Hz is 7.4

CIGRE DCS1 Stability Analysis (1)

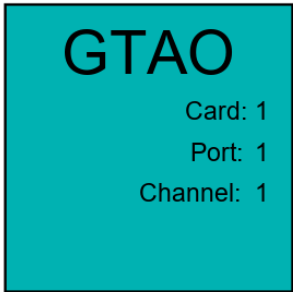
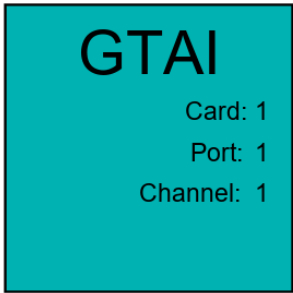
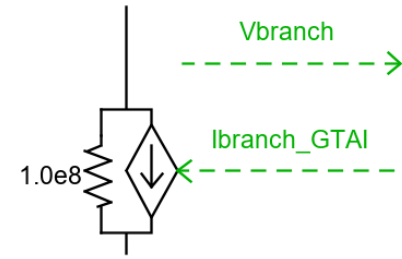
DCS1 Critical SCR (CSCR) and Time Domain Validation



PHIL Simulation

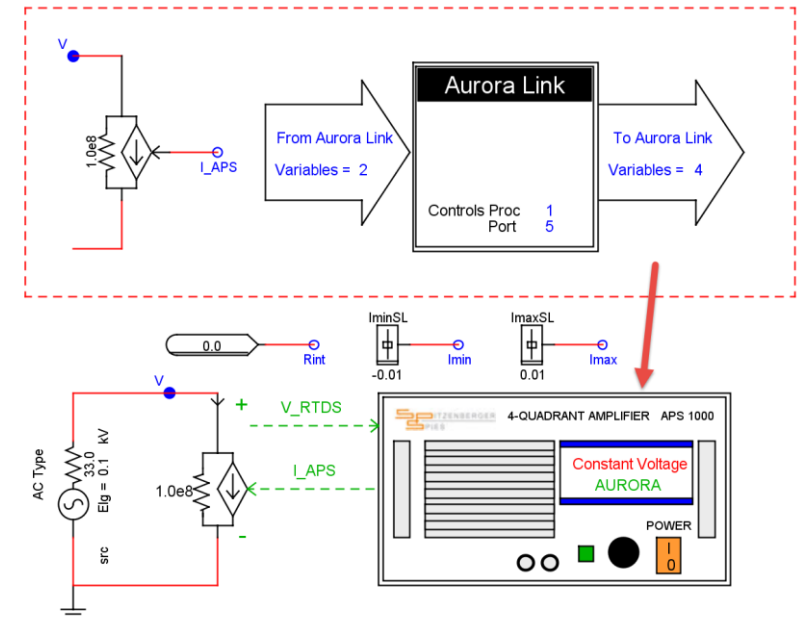
➤ Conventional Interface for PHIL Simulation

- Component with conventional GTA0 and GTAI plus current source embedded
- Optimized timing for data exchanges to further reduce loop delay (loop delay is less than Δt)



➤ Aurora Interface for PHIL Simulation

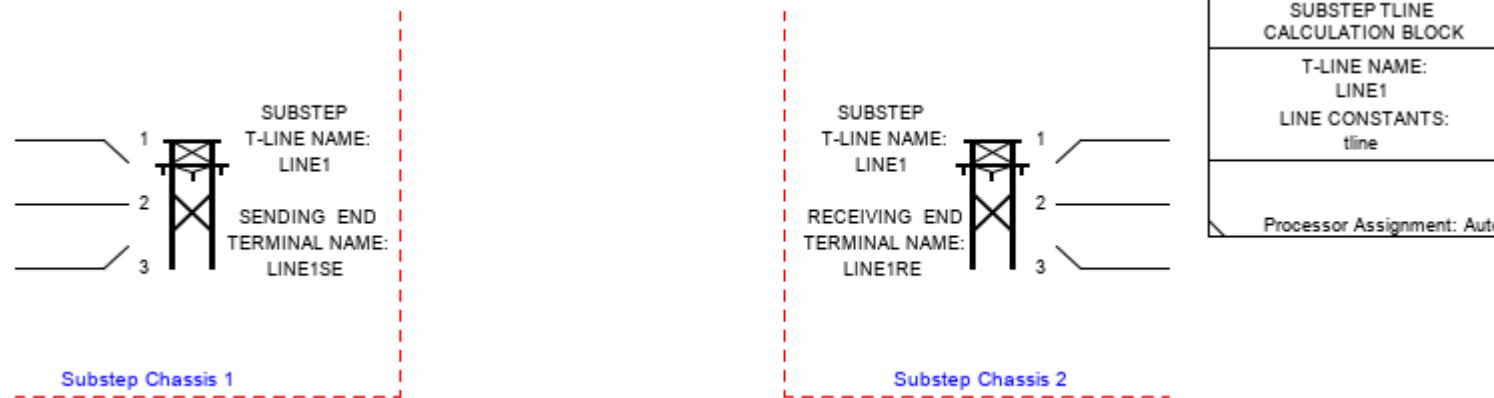
- Component with Aurora link plus voltage/current source embedded
- Optimized timing for data exchanges to further reduce loop delay (loop delay is less than Δt)



New Features in RSCAD

➤ Cross chassis connections enhanced

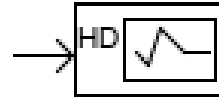
- Cross chassis substep connections



- Cross chassis Superstep connections

New Features in RSCAD

- Substep and small time-step high resolution plotting

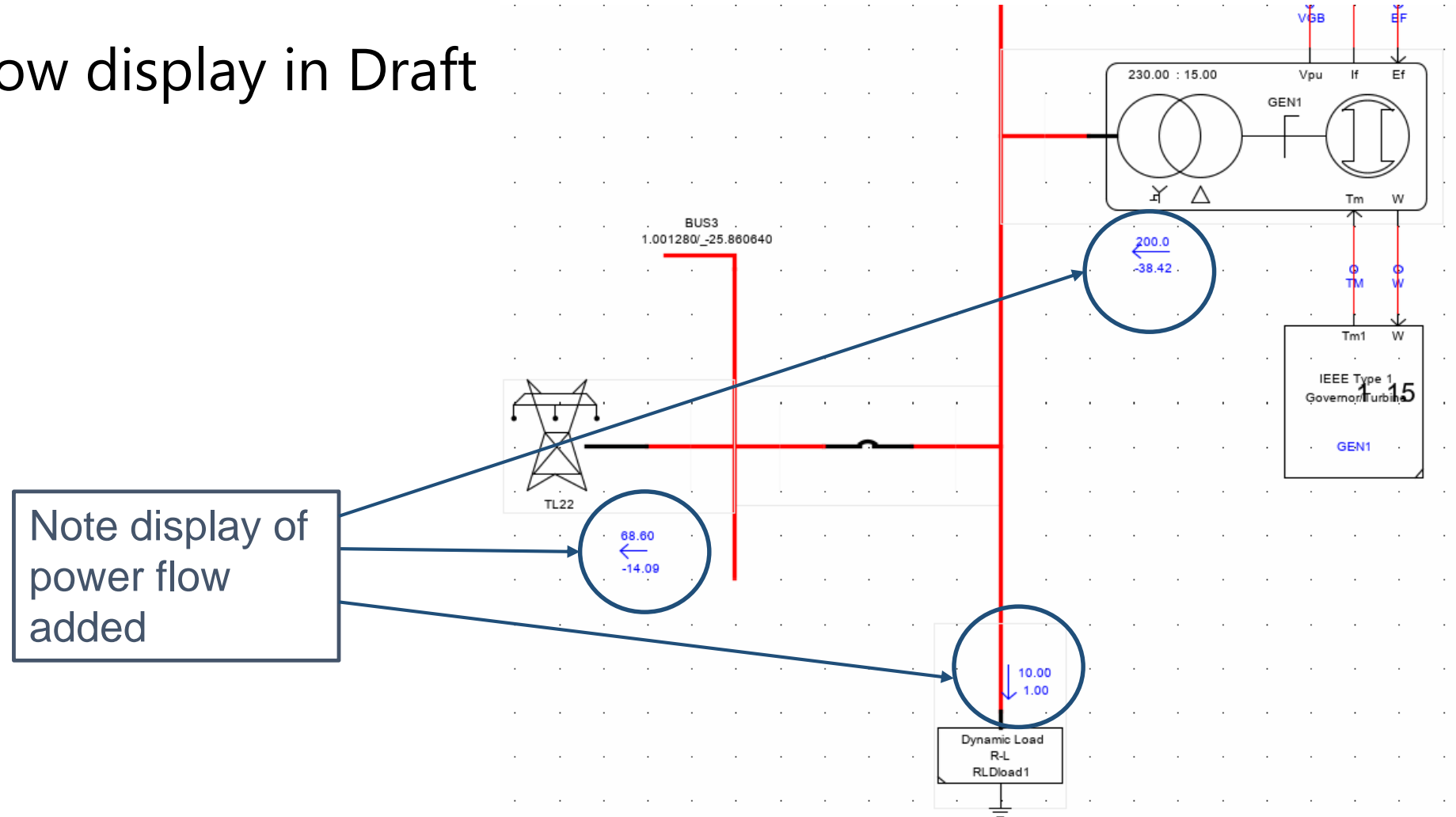


SUBSTEP HIGH RESOLUTION
PLOT COMPONENT

- Increased the number of signals that can be plotted in RunTime

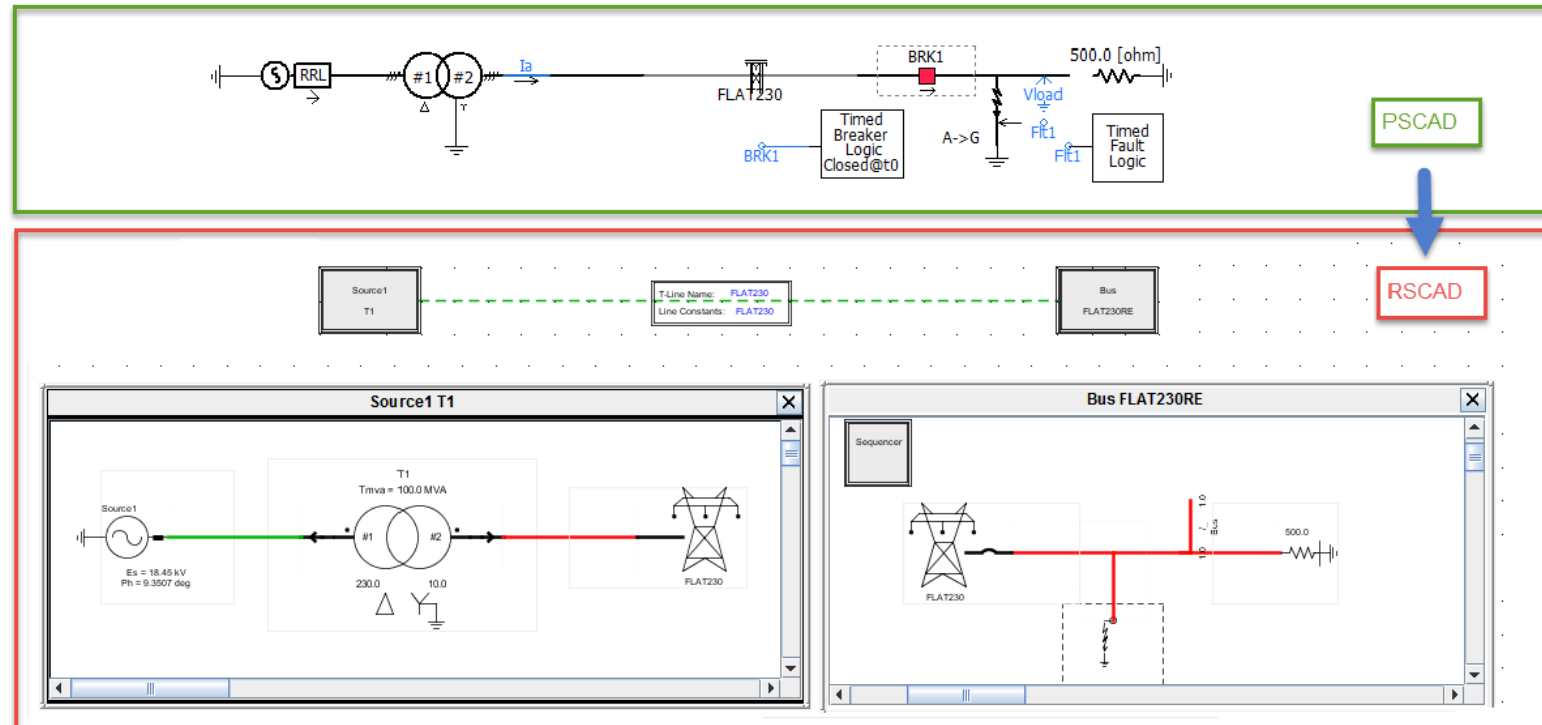
New Features in RSCAD

- P & Q load flow display in Draft



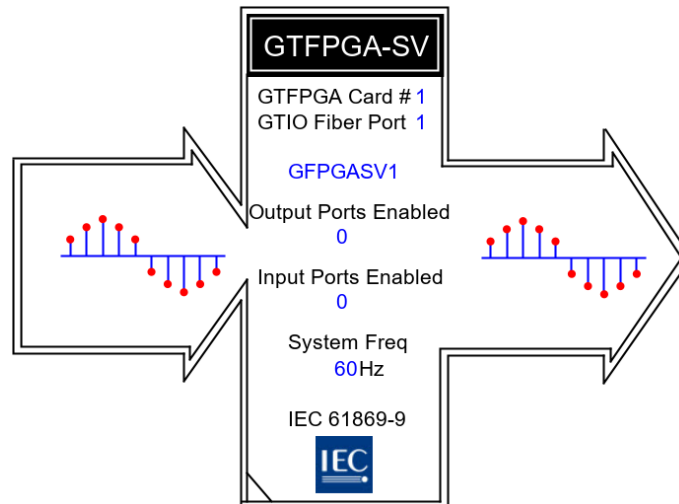
PSCAD to RSCAD Conversion

- Hierarchy boxes used to organize components
- In addition to built-in conversion scripts, user can specify (or override) how components are translated



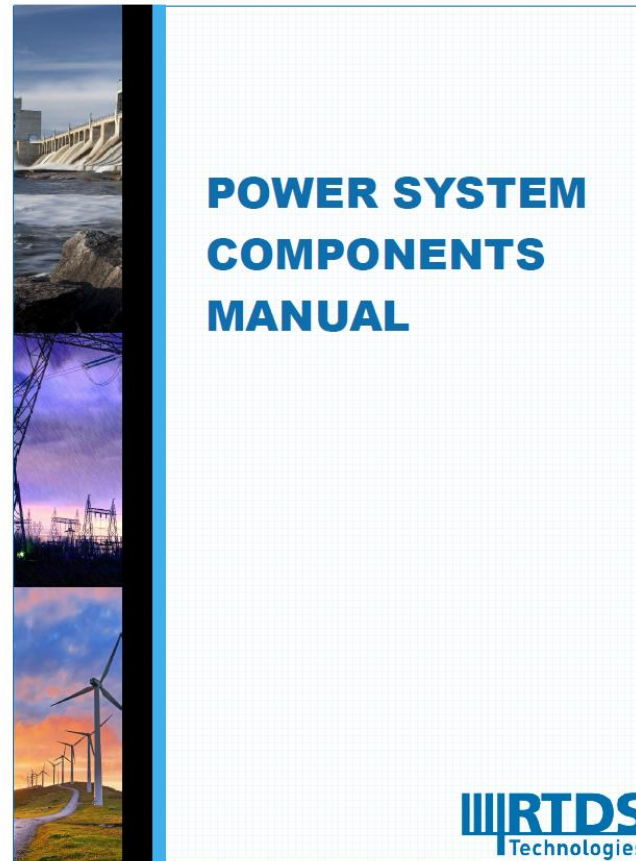
Protection and Automation Updates

- P&A Suite
- PMU Utility Enhancement
- GTNETx2 Development – MODBUS, 104 and SKT
- GTNET SV v1 - 16 streams 24 channels at sampling rate of 80, 96 s/c and 4800Hz
- GTNET SV v2 - 1 streams 24 channels at sampling rate of 96kHz
- GTNET SV v2 – Small DT/Substep for 96kHz and 250kHz



New Customer Support Features

- Improving documentation and release notes



New Customer Support Features

➤ New Client Area

RTDS Technologies Customer Support Web Site (Release 4.41)

Navigation

- Introduction
- Downloads
- Uploads
- Release Notes
- Get RSCAD Keys
- Get NovaCor Certificates
- Support Requests
- RMA Requests
- Web Site Settings
- Change Password
- Installation Instructions
- System Requirements
- Technical Publications
- Log Out

Introduction

Log-In Information

Email Address: paf@rtds.com
Company Name: RTDS Technologies Inc.
Logged in since: 2019 10 02 05:05:50 PM CDT

Notice History | Log-In History (Admin Only) | Company Actions (Admin Only) | Unconfirmed E-Mail Logins (Admin Only) | Notice Maintenance (Admin Only)

Email Notification Maintenance (Admin Only) | Event Log (Admin Only)

Date	Notice
2019 03 08 08:04 PM CST	<p>Version 5.007.2 was released on March 1, 2019.</p> <p>Some people may have noticed that our support website seems a bit different. We've ported it to a new application server and re-done the user administration.</p> <p>Here are the main new features:</p> <ul style="list-style-type: none">The old "Company" accounts are no longer available. Instead, each company will have one or more email-based accounts that will serve as Company Administrators. If you have been trying to login using your company name instead of an email address, this will now fail. Although this may be annoying in the short term, it improves our security by letting us see, and the Company Administrators see, who can log-in to the administrative accounts.The new Company Admin users will be able to add or remove email addresses, enable/disable email addresses and send invitations to new users (as the old Company admins could do before). They will also be able to designate additional Company Admin users if desired.

The **All-in-One** Real Time Simulator

The Goal of RTDS Technologies is to provide:

An All-in-One Real Time Simulator for Power System and Power Electronics.

- Largest system possible
- Smallest time step and details of switching
- Most detailed modelling
- **All-in-One** simulator covers from small to large scale circuits
- Continual Innovation and Research & Development
- Interacting and collaborating with users of simulation practice and applications.

Covers from nanosecond to hundred microsecond time scale

What is RTDS? Not only a simulator but also a team.

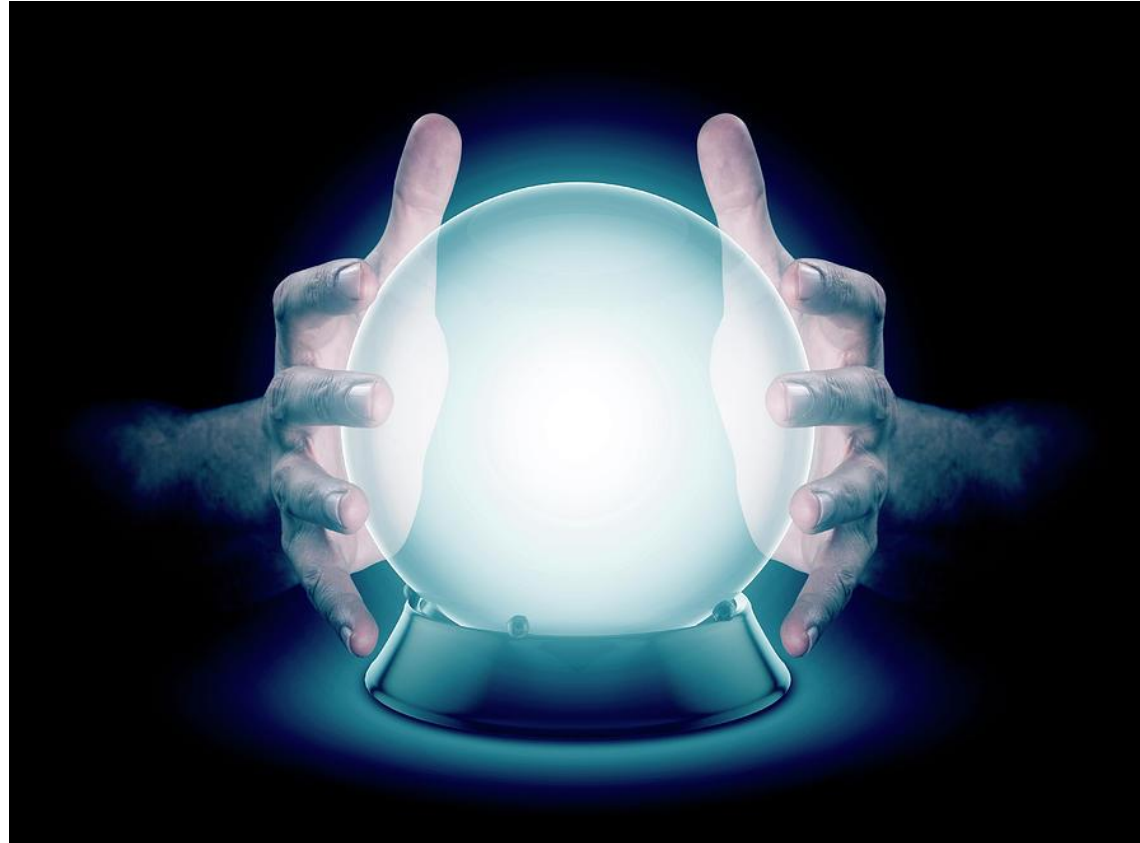


We Are Team RTDS...



Team RTDS is with you and ready to serve you !

LOOKING TO THE FUTURE





**THANK YOU!
QUESTIONS?**



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