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SUBSTEP SIMULATION

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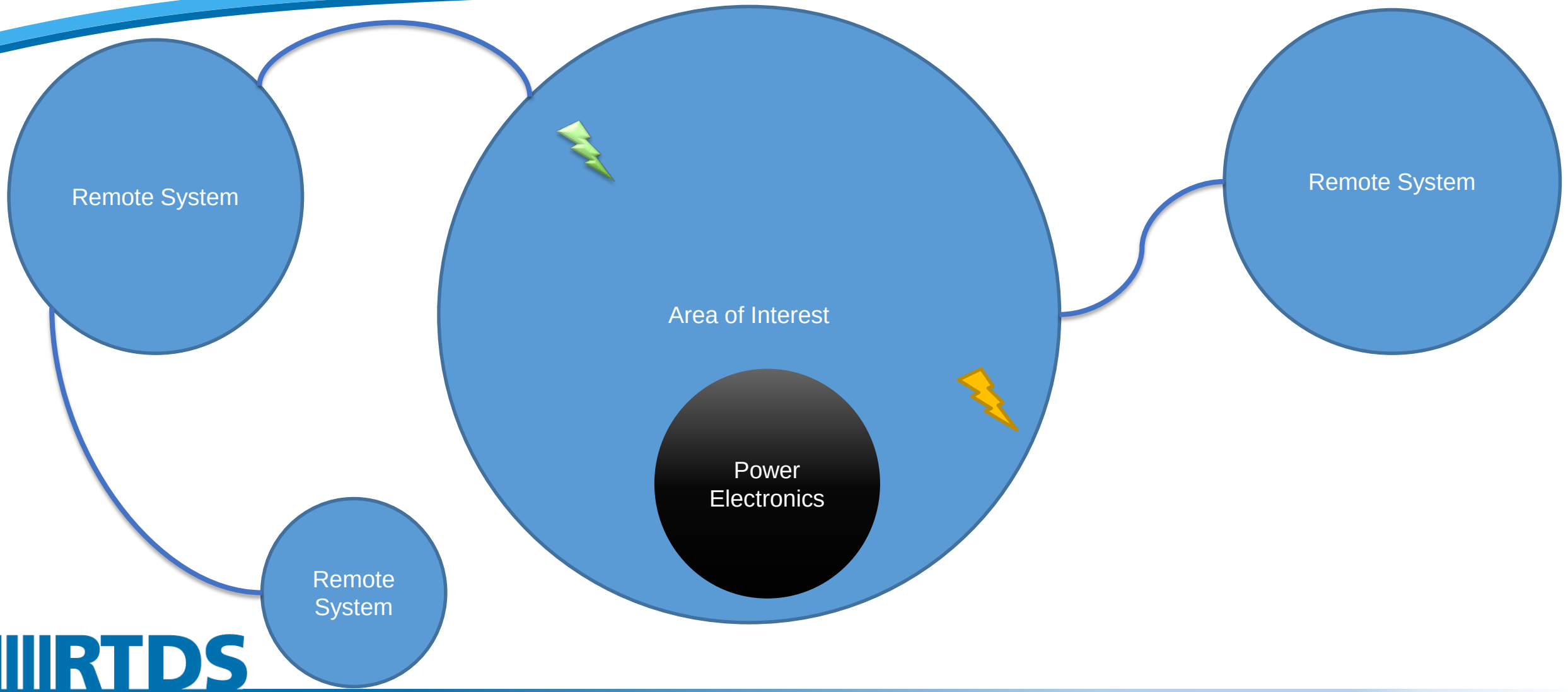
Outline

- Introducing Substep
- Multirate Simulation
- Substep and Small Timestep
- Substep Feature
- Examples and Test Results
- Summary

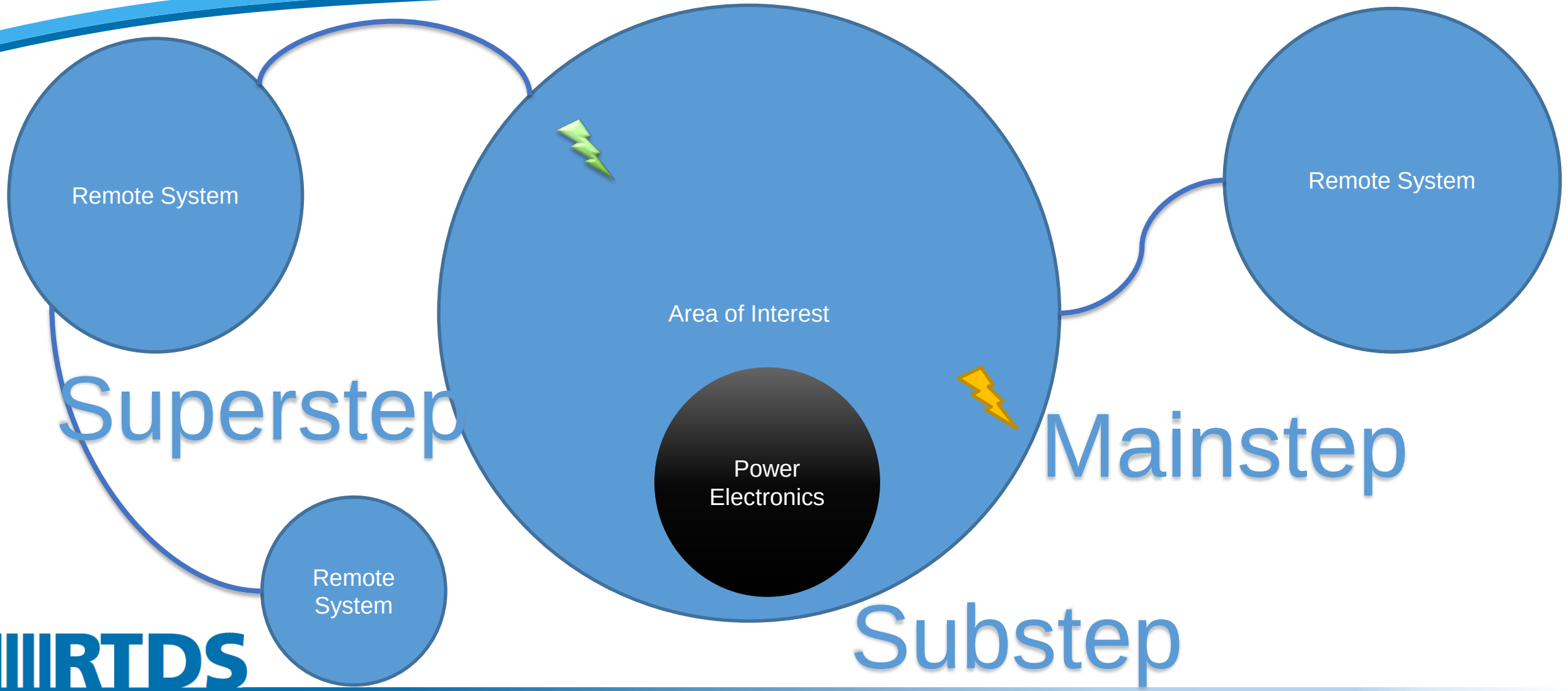
Introducing Substep

- NovaCor platform provides a lot of computation power which can be used to develop new features
- Prior to NovaCor, simulating high-frequency switching power electronic converters required using small time step library
- Converters in small time simulation uses LC switching or resistive switching with interface t-lines due to constant admittance matrix approach from the small time step simulation environment.
- The processing power of NovaCor has made it possible to perform matrix re-factorization at time steps as low as ~1 µsec.
- This has created a new simulation environment, Substep, which will simulate control and/or power system circuits multiple times for each Mainstep but perform a matrix re-factorization for each Substep.
- This will support modelling switches are pure resistive switches
- Losses will be low, signals will be cleaner and the time step size will be small to support high frequency switching.

Multirate Simulation

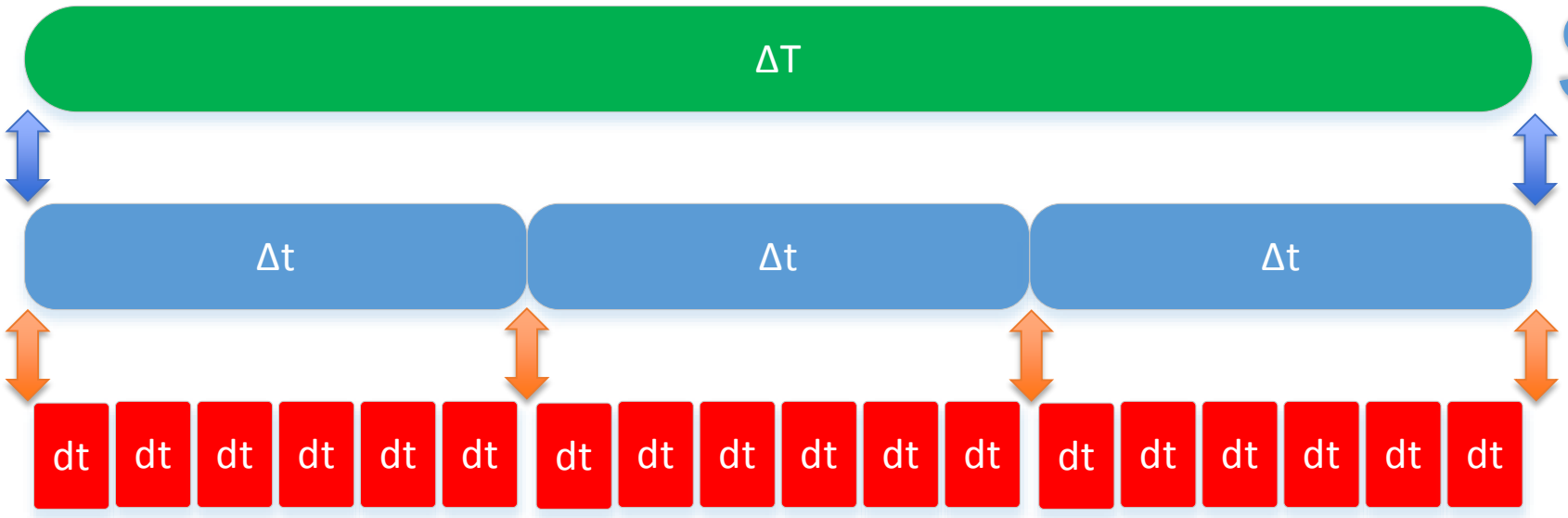


Multirate Simulation



Substep

Multirate Simulation

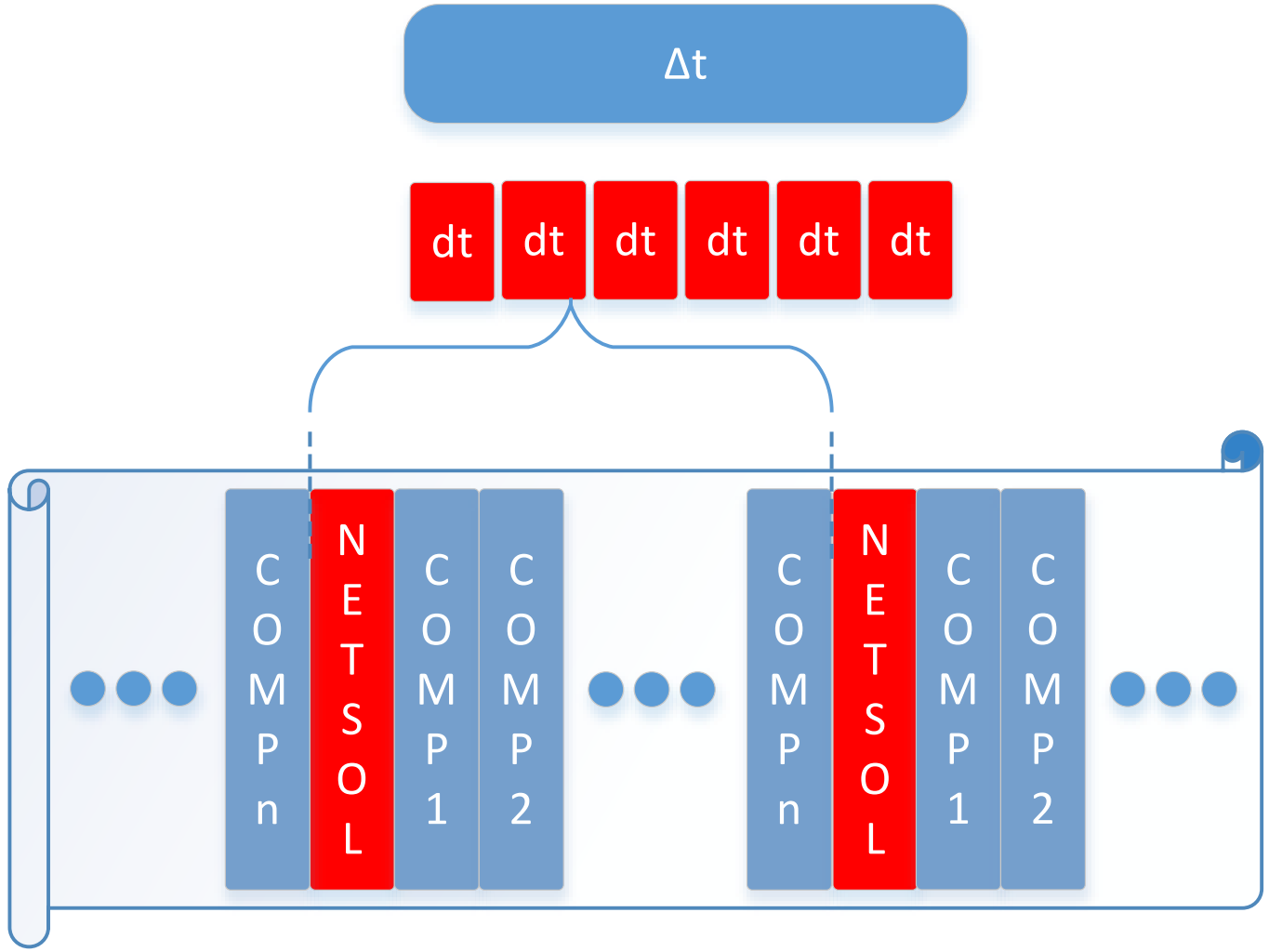


Superstep

Mainstep

Substep

Substep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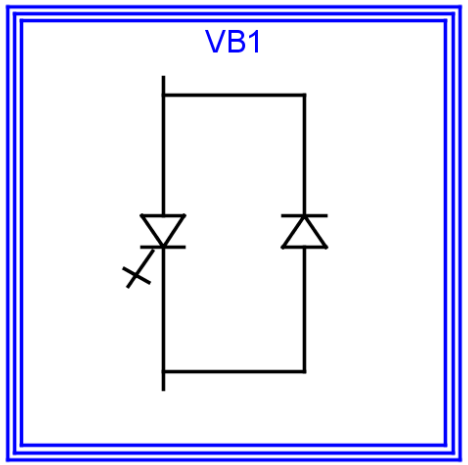
COMP2

Substep or Small Timestep

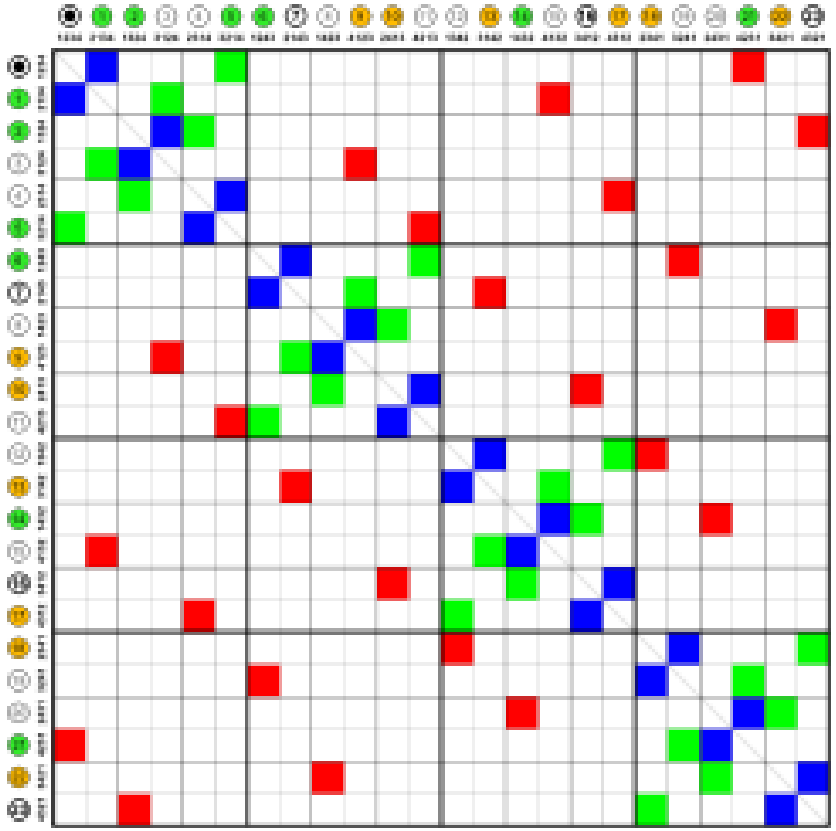
- Substep is designed based on Power8 processor and NovaCor simulator
- It allows using the power of NovaCor to develop new features and component for power electronics simulation
- Substep is available in RSCAD 5.007



Advantages over small timestep

- **Full decomposition Network Solution**
  - No hard limit on resistive breakers/switches
  - More accurate models (saturation, non linear elements)
  - Resistive switching converters with no interface Bergeron lines

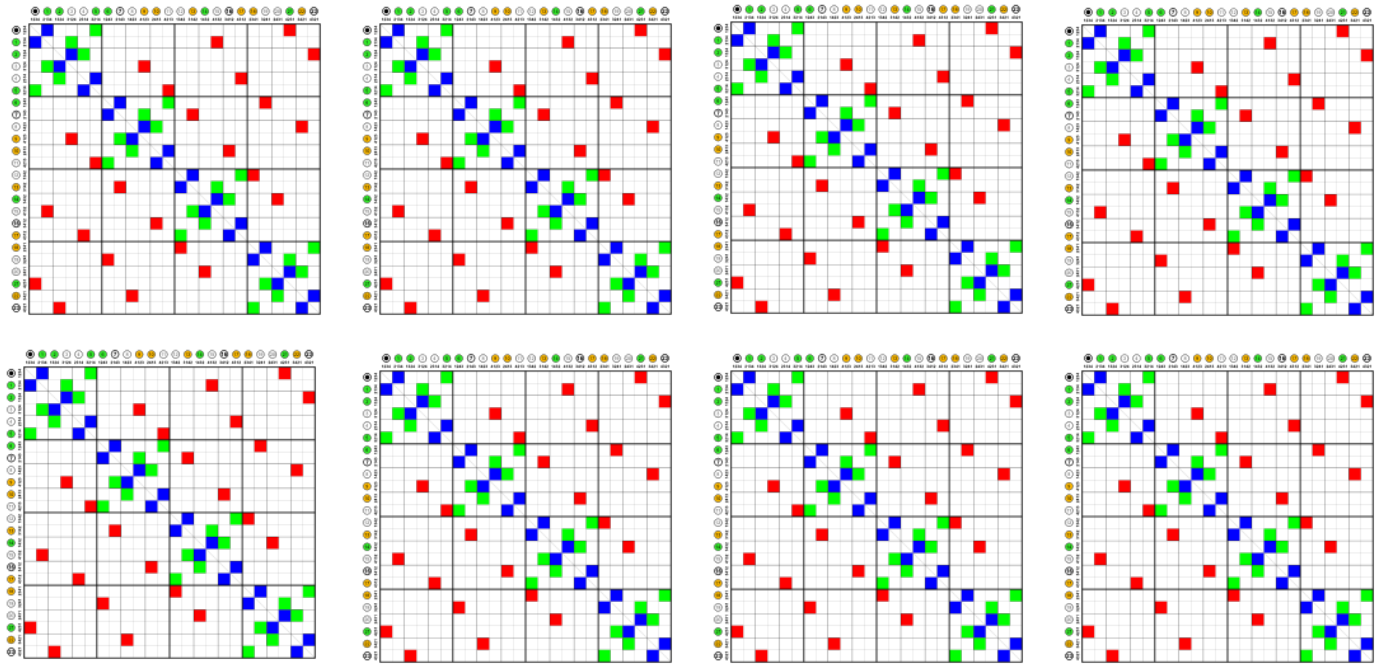
Small timestep network solution



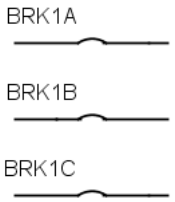
- In small timestep pre-calculated matrices are stored in the simulator
- In every small timestep pre-calculated matrix is multiplied by the injection vector to calculate node voltages

$$V = Y^{-1} \times I$$

Small timestep network solution



- To model resistive switches, all permutations must be stored. (2^n for n switches)
- All matrices must be stored in the processor cache
- A limited number of switches can be modeled

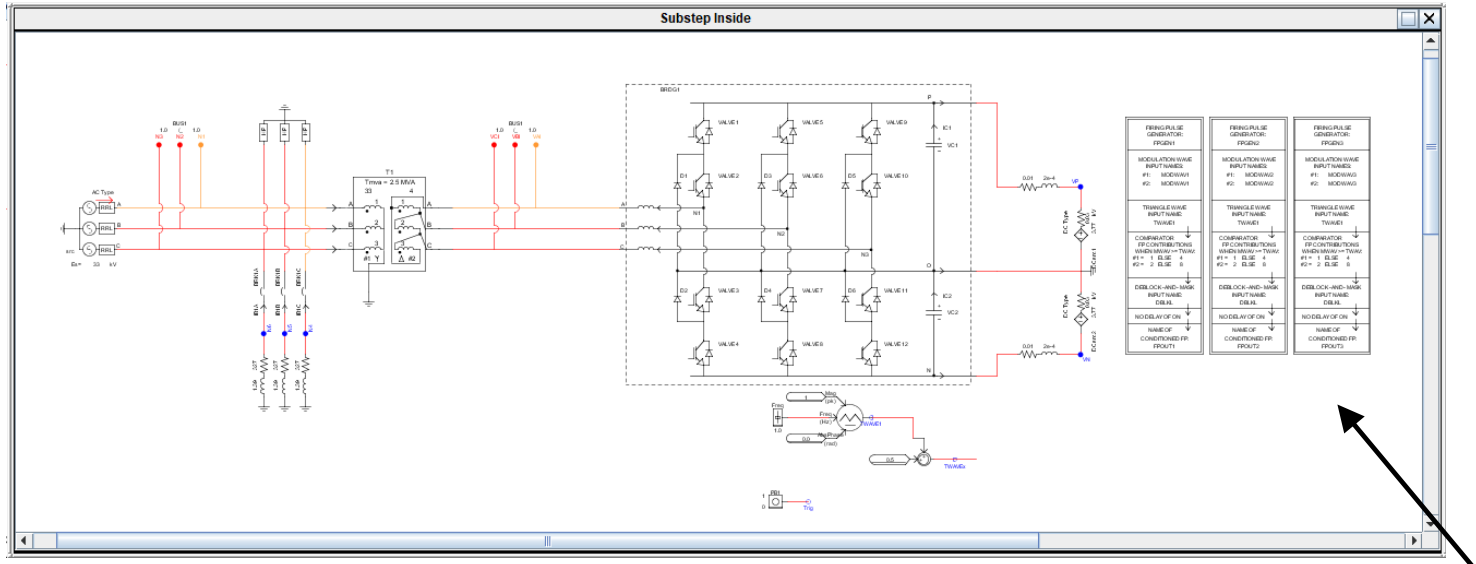


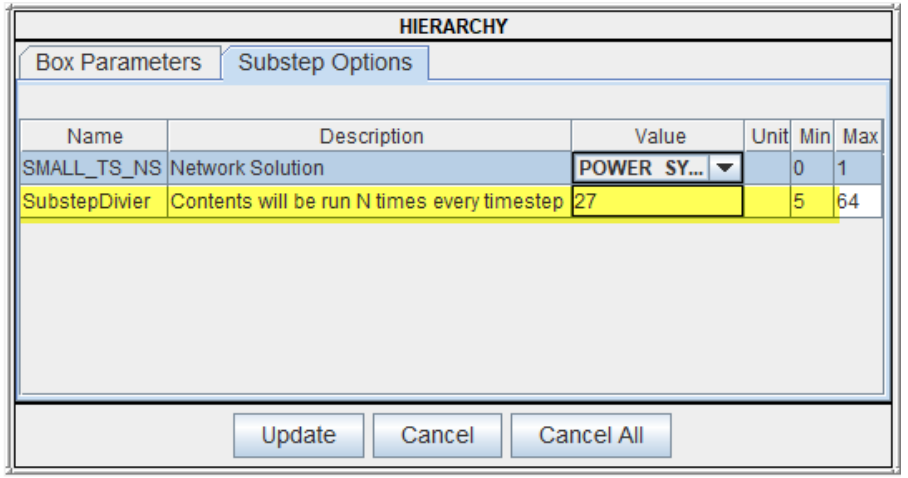
Substep network solution

- Substep network solution solves the nodal equation every Substep
- This allows using more resistive breakers and more accurate models

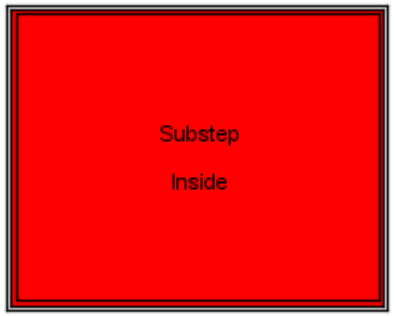
$$\begin{pmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{pmatrix} = \begin{pmatrix} L_{11} & & \\ L_{21} & L_{22} & \\ L_{31} & L_{32} & L_{33} \end{pmatrix} \begin{pmatrix} U_{11} & U_{12} & U_{13} \\ & U_{22} & U_{23} \\ & & U_{33} \end{pmatrix}$$

Substep



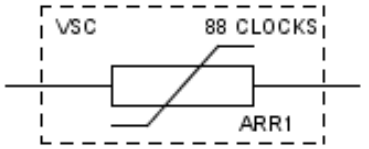


- Mainstep = 30 µsec
- Substep divider = 27
- Substep time step = 30/27= **1.11 µsec**

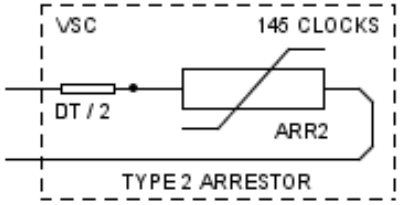


More Accurate Models

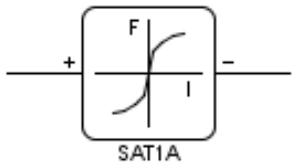
- Full decomposition allows accurate representation of nonlinear elements such as surge arrestors and transformers and machines with saturation.



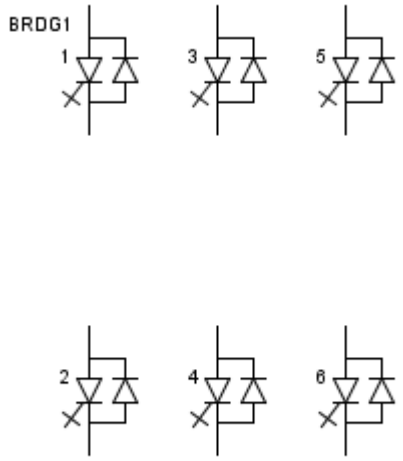
ARR1 less accurate than ARR2, but number of clocks used is less than ARR2



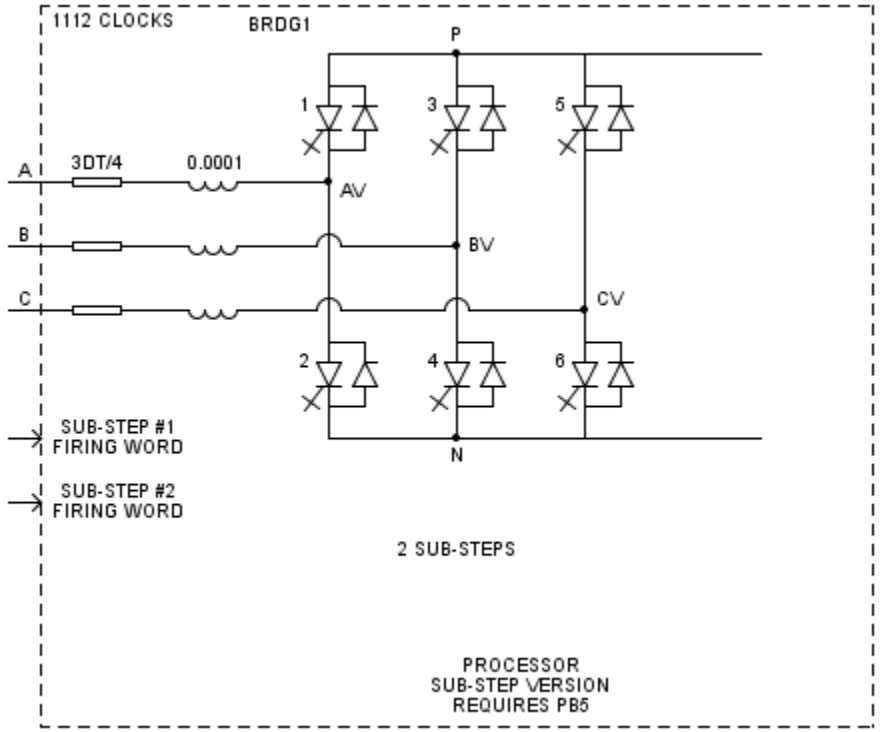
ARR2 is an accurate model of an arrestor Modeled just like the large time-step arrestor model, but requires more clocks



Allows Elimination of Interface Lines



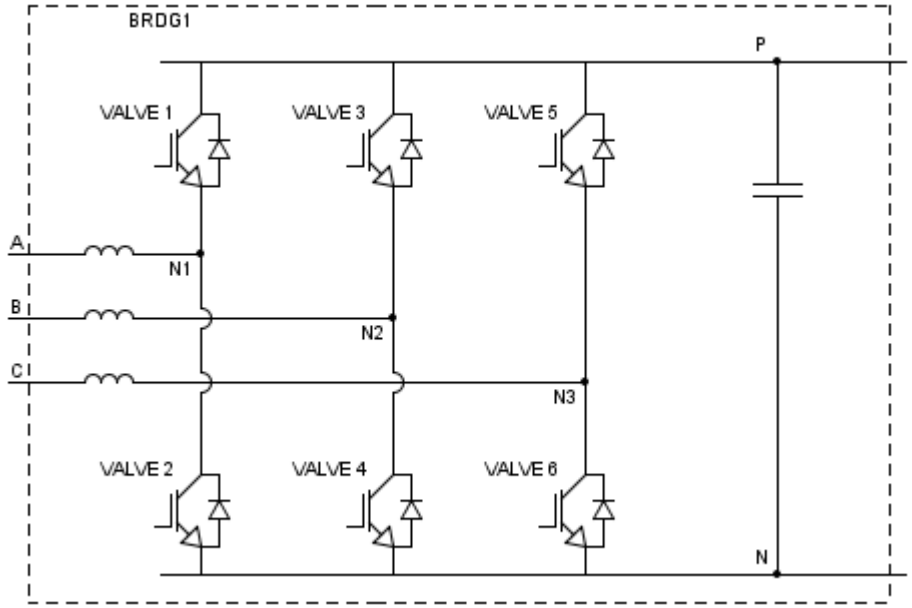
LC Switching
No Interface



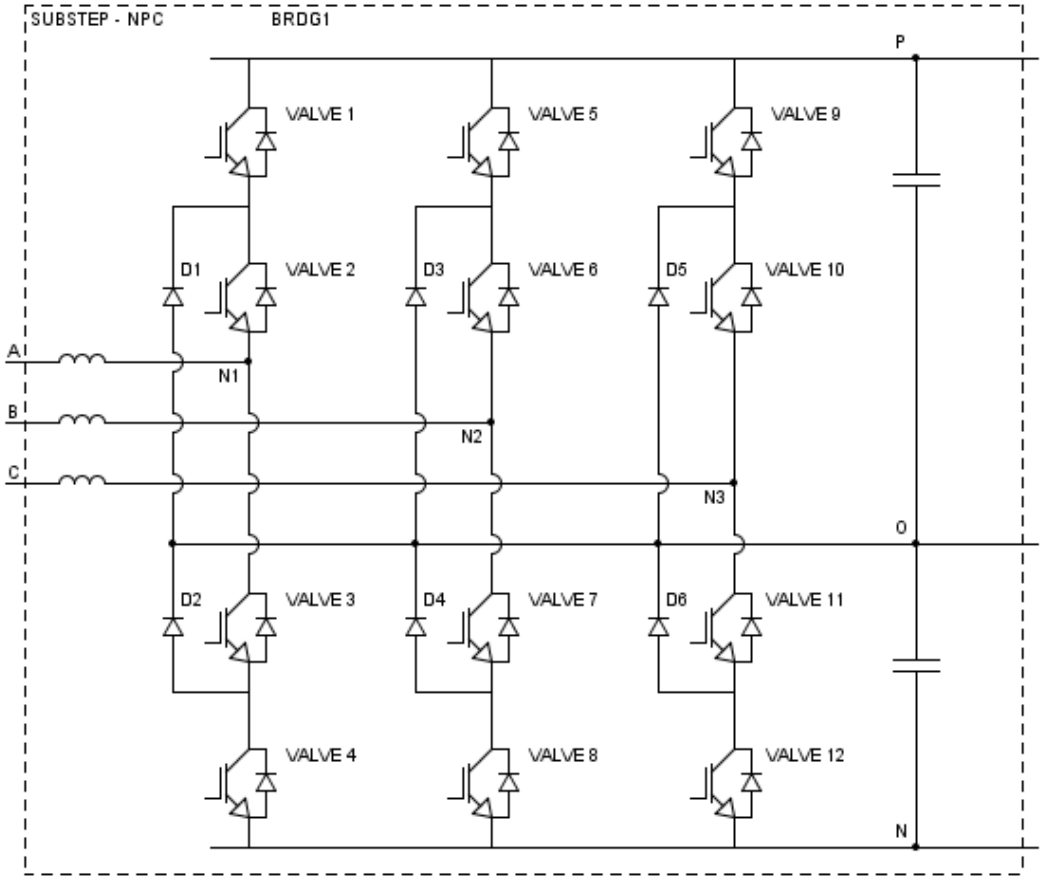
Resistive Switching
Bergeron Interface

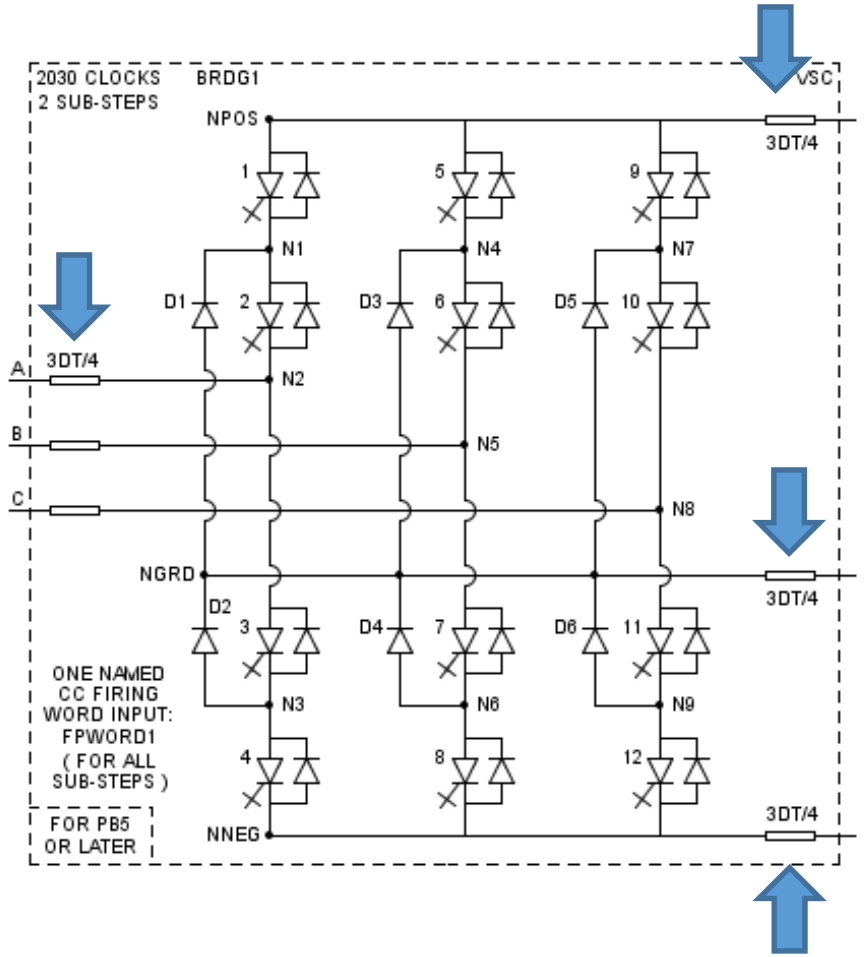
Allows Elimination of Interface Lines

- Full decomposition allows modeling converters with resistive switches without the need for Bergeron interface t-lines.

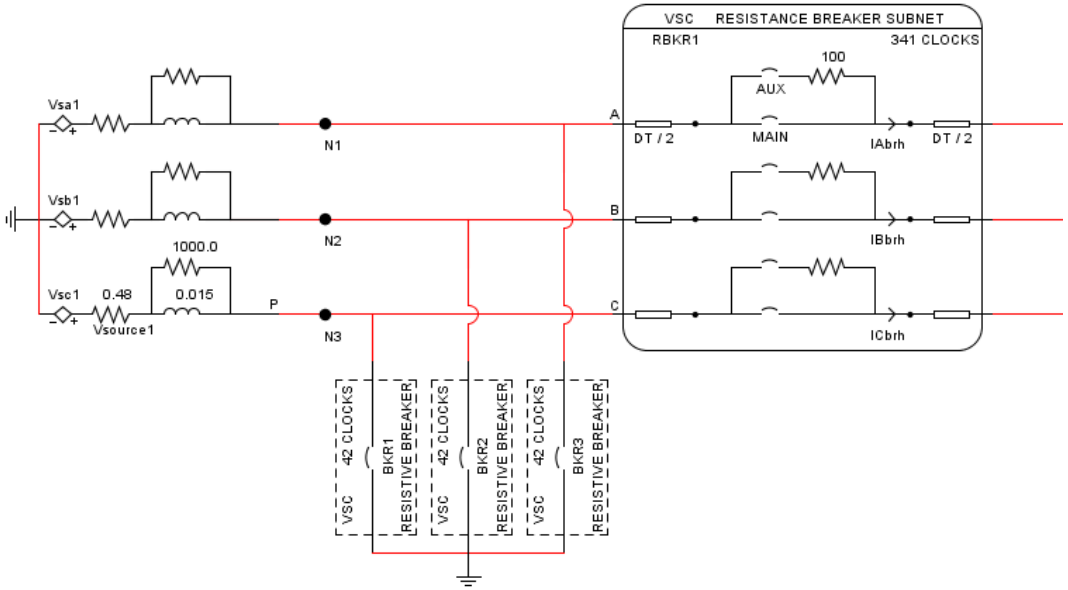


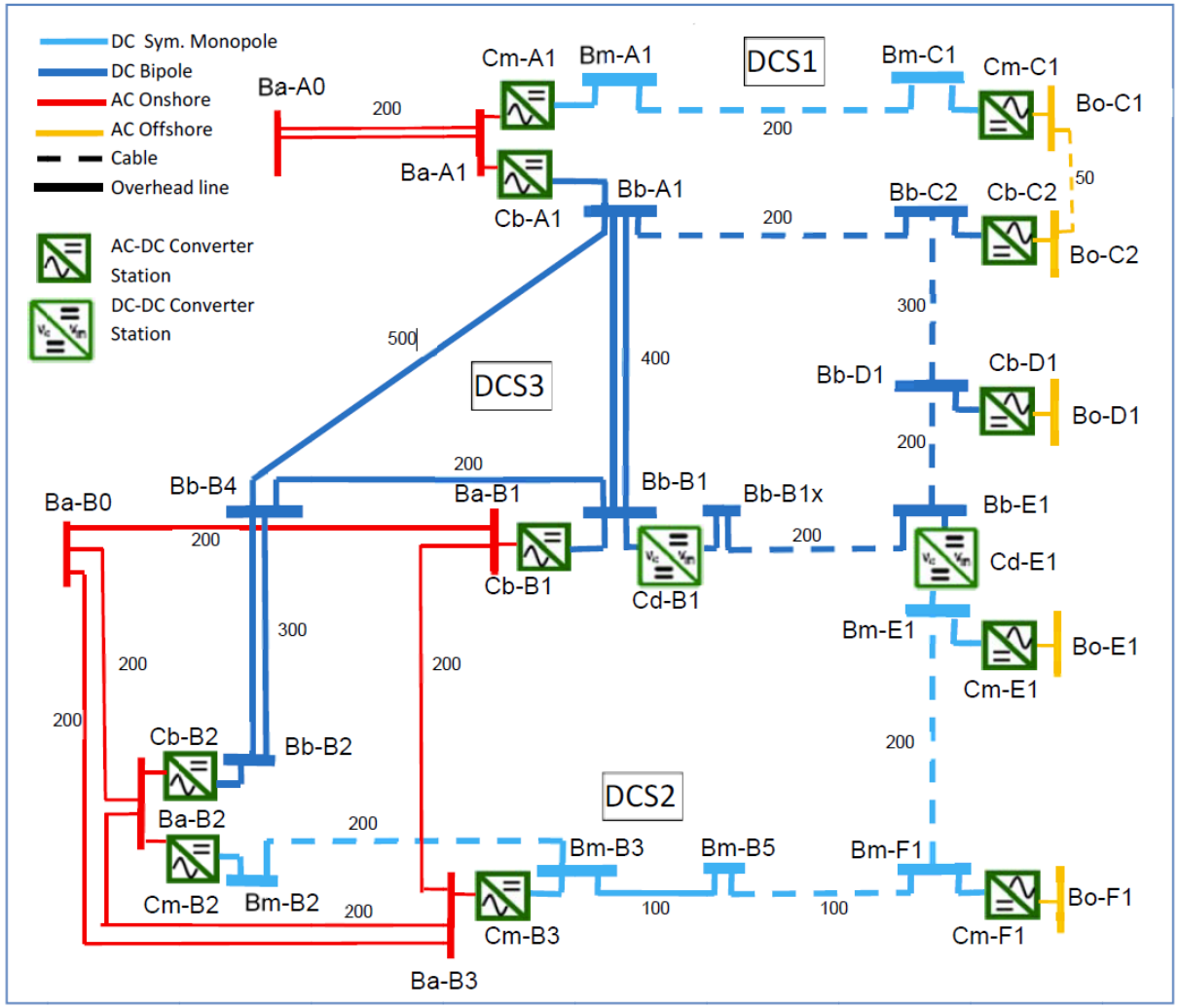
3 Level Converter





More Resistive Breakers





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Introducing NovaCor™ – the new world standard for real time digital power system simulation

Substep vs Samll-dt

	Small time Step	Substep
Hardware	Available GPC, PB5, NovaCor	Available for NovaCor only
Processor Assignment	One or two cores Or 1-2 PB5/GPC processors	One full core
Node limit	Node limit = 30 (PB5/GPC) Node limit = 45 (NovaCor)	Node Limit = 60
Time-step	Small time-step range: 1.4 – 3.75µs	Substep range: no minimum – 10us Range if LC switching included: no minimum – 3.75us
	Time-step *is not* user selectable. Time-step is chosen by RSCAD based on requested time-step by user	Time-step *is* user selectable Substep time-step = 1/N * main time-step, where 5≤N≤64
Switch model	Most Models: RLC Switching Resistive switching with artificial interface tlines *(for 2 level converter)*	Most models: Resistive switching ***without*** artificial interface tlines RLC switching *(typically for individual switches/custom topologies)*
Solution Process	Constant conductance matrix. No matrix inversion required each time step. If tline decoupled models used, then the conductance	Full decomposition of Network Solution
Resistive Limits	10 resistive breakers	No resistive breaker limit
I/O	Specific process. *See Small time-step tutorial.* GTNET not supported	Same straightforward process as mainstep I/O. GTNET not supported
Components	Only small time-step components	Substep, Controls, Power system components

Substep Features

- Substep is only available on NovaCor hardware platform
- Each Substep network requires a full core
- Substep time step = 1/N * main step time step
- Substep library is developed which has models optimized for a smaller time step
- Components from the Mainstep library are supported *
- No limit on the number of resistive switching elements*
- No fictitious losses
- Full decomposition allows accurate representation of non linear elements (surge arrestors, transformer and machine saturation)
- No interface lines required for use of resistive switching
- Multiple Substep networks allowed
- IO cards supported (excluding GTNET)

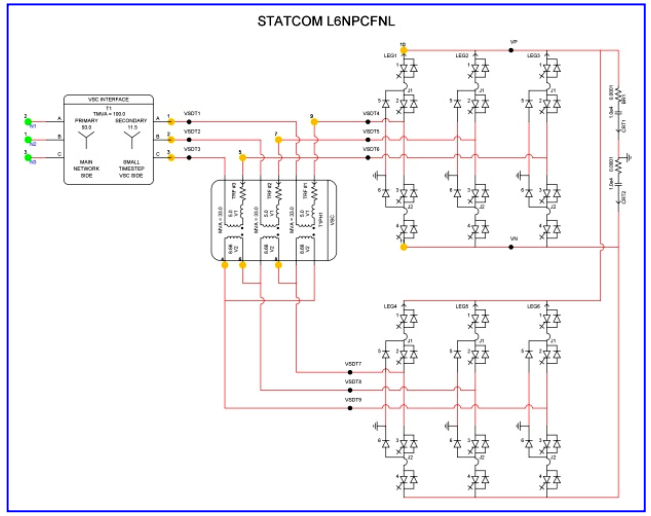
Difficulties of Resistive Switching

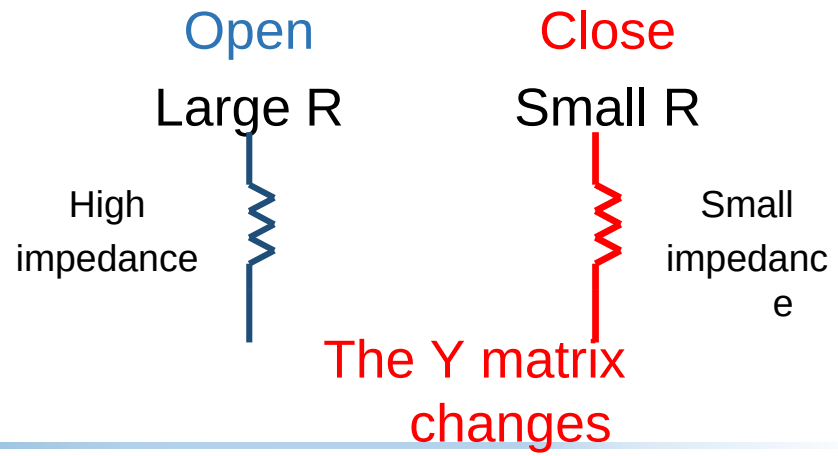
- **EMT programs**

  Switched resistive representation

- **Challenge**

- to simulate the high switching frequency. Requires low time step (~1-3 µsec)
- The topology change causes the frequent re-factorization of system conductance matrix.
- Real time simulation is challenging for higher switching frequency. For instance, if the time step is 2 µs, the g matrix need to re-factorize every 2 µs. No exceptions.

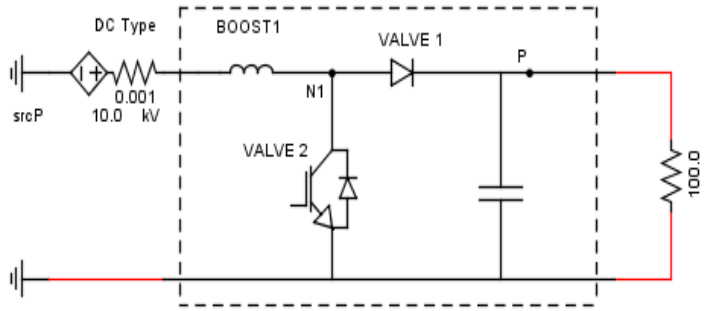




Difficulties of Resistive Switching

Simple Voltage Boost Converter example

- When IGBT Valve 2 is fired on, the diode V1 should change from ON state to OFF state for the next timestep.
- If not properly predicted, both IGBT and Diode will be ON for 1 time step
- Results in a large erroneous spike in current



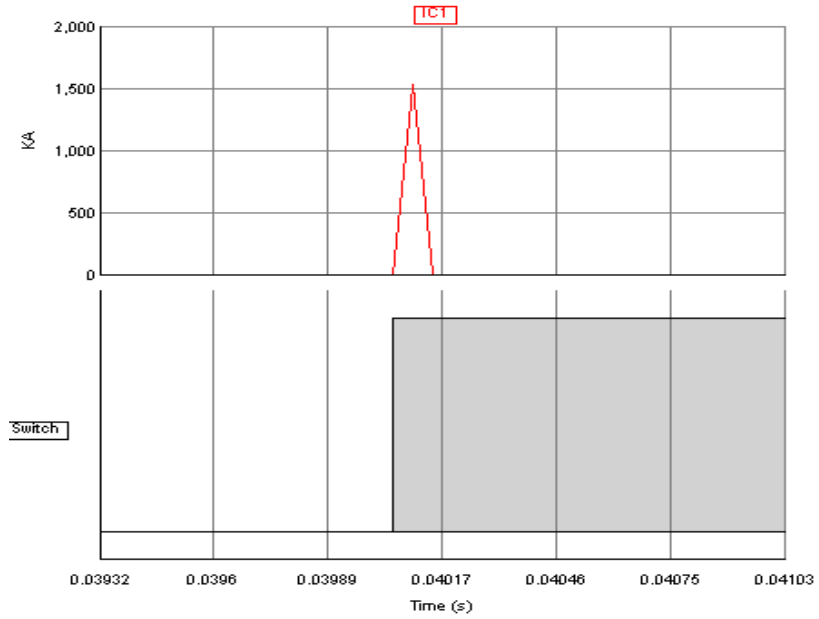
Offline simulation tools

- It employs interpolation techniques to eliminate numerical inaccuracies

Real time simulation

- Interpolation cannot be used

Do we know the switching statues of switches in next time step?



Predictive Resistive Switching

Predictive resistive switching is a method of predicting the ON/OFF statuses of switches in a VSC for the next time step when switched resistances are used

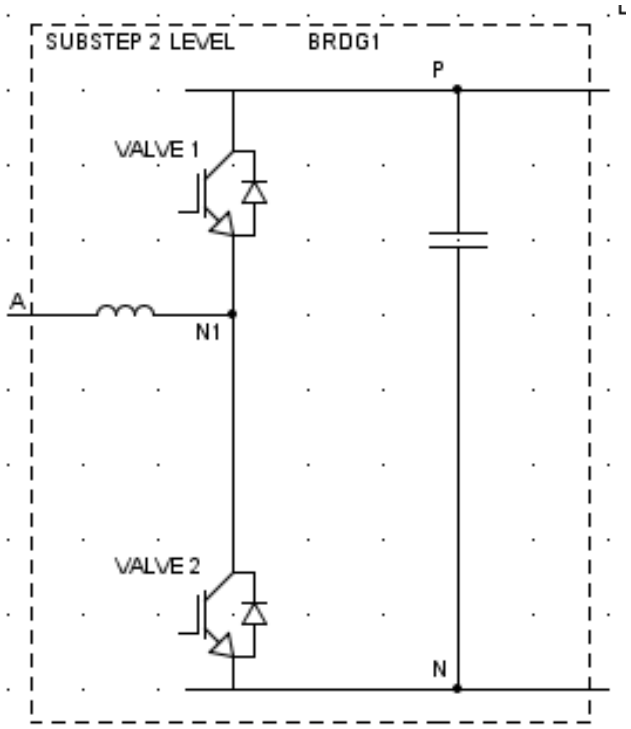
Procedure of predicting the switching status:

- Solve the circuit and get a preliminary solution of each node voltage
- Calculate each branch voltage
- Predicting the switching status according to the branch voltage

Predictive Resistive Switching

- Strong electrical interaction between switch device within a leg
- Weak electrical interaction between switch devices from different legs

As a results, predictive ON/OFF statuses are predicated separately for each leg



2 level VSC leg

Predictive Resistive Switching

Each switch behave as a **ON branch, OFF branch or Diode branch**

Example: 3 level T-type Leg

Valve 1 - **ON branch** when fired

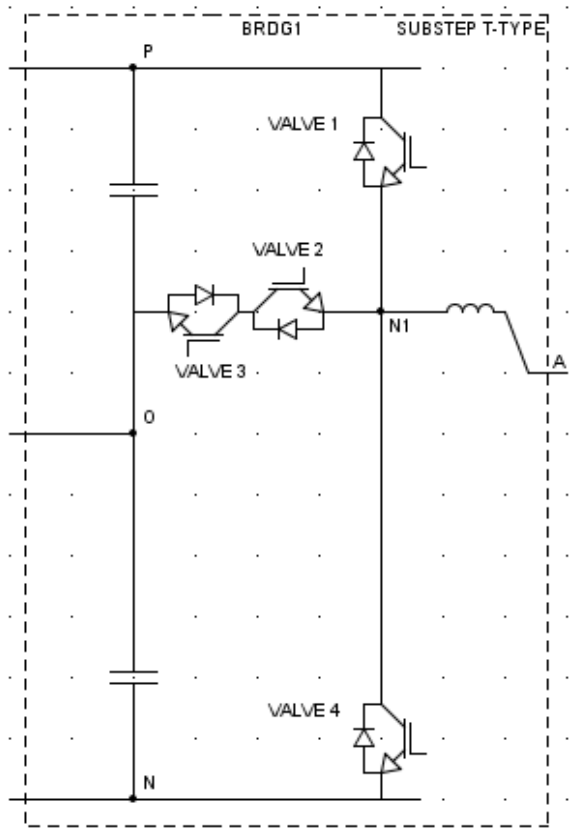
- **Upward directed diode** when NOT fired

Valve 4 - **ON branch** when fired

- **Upward directed diode** when NOT fired

Valve 2 and 3 are combined as one single switch

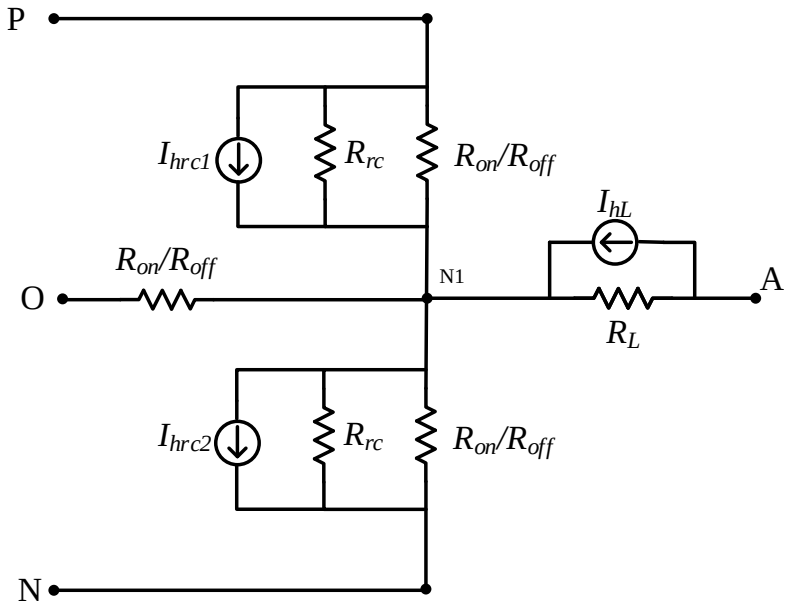
- **ON branch** (V2 and V3 is fired)
- **OFF branch** (V2 and V3 NOT fired)
- **Diode directed toward node N1** (V2 is fired and V3 is NOT fired
- **Diode directed toward node 0** (V2 is NOT fired and V3 is fired)



Predictive Resistive Switching

Example: 3 level T-type leg

- 4 switches per leg in real circuit
- 2 switches connected in series with neutral path can be combined to one switch for EMT model (test circuit will have 3 switched resistance)
- 8 possible switching combination
- Test circuit will go through each combination to find valid combination based on latest firing pulses, history currents, peripheral nodes voltages
- Will apply valid switching combination for the next time step to actual T-type bridge



T-type test circuit model

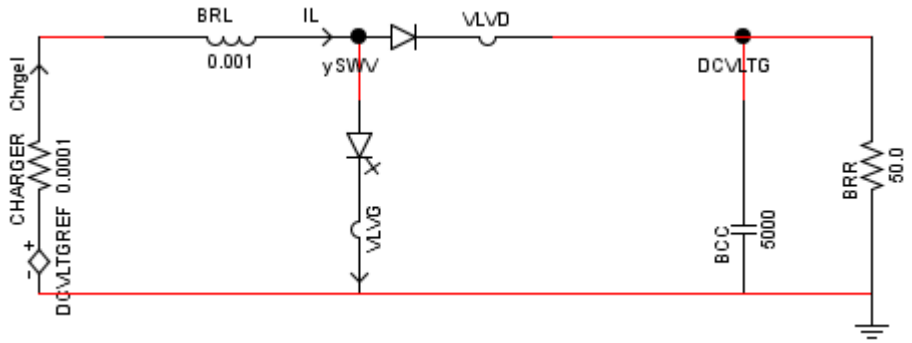
Substep Example

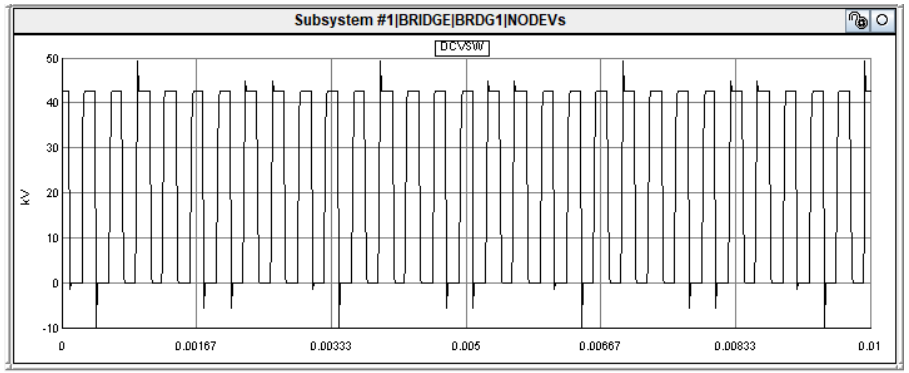
Test Platform

- NovaCor simulator with Power 8 Processor
- Processor operate at 3.5 GHz

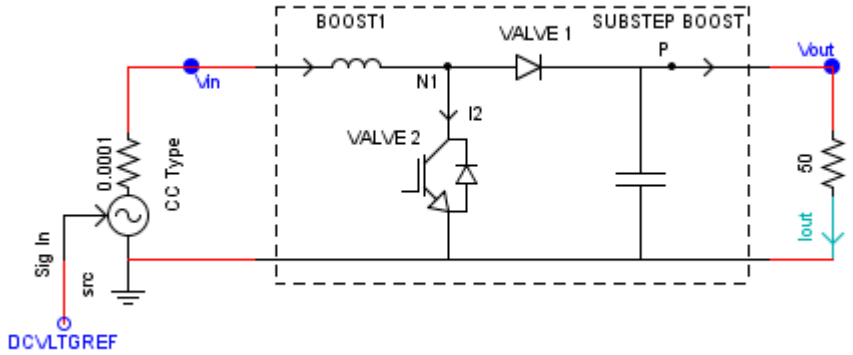
Simulation Results

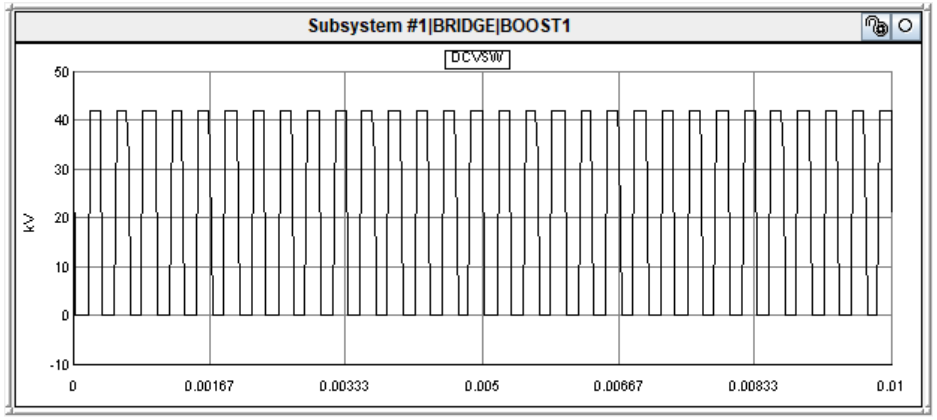
Case 1 : Boost Converter





Small time step



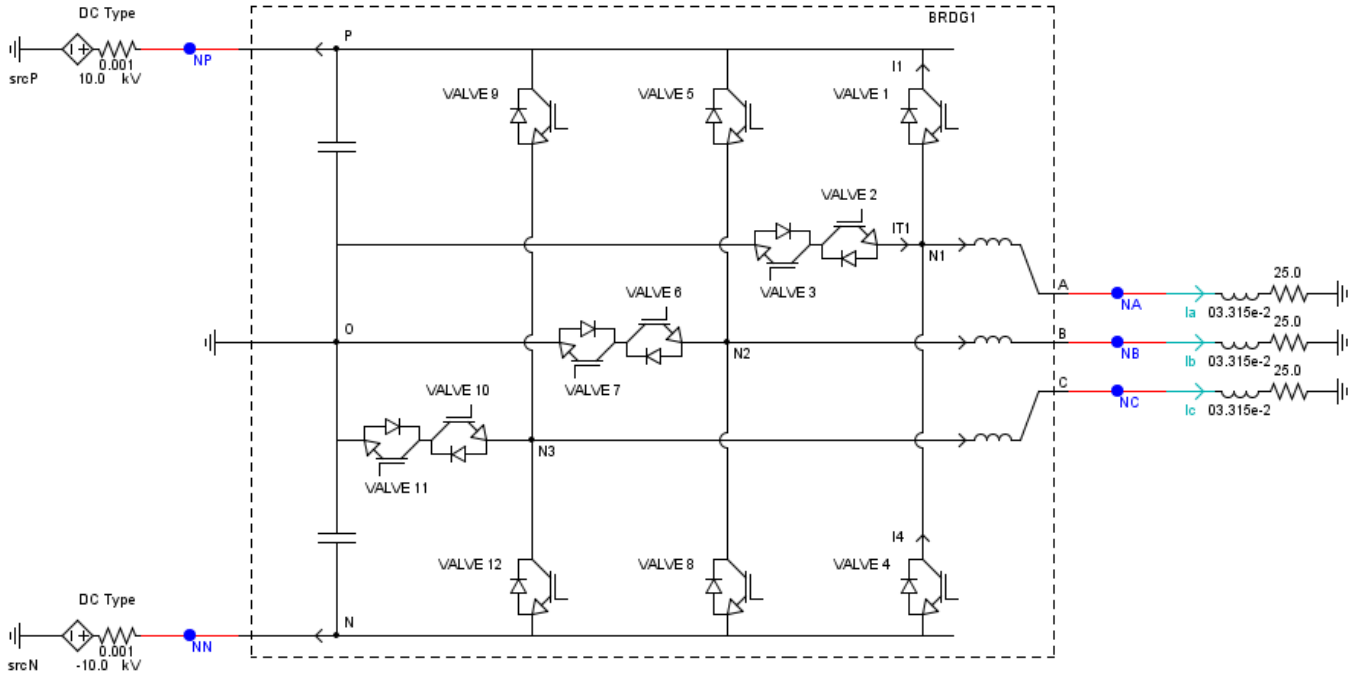


Substep

* The boost converter can run in substep at ~500 nanoseconds

Simulation Results

Case 2: 3 phase 3-level T-type VSC bridge



- 8 Nodes and 9 switches
- The power system components are running at 0.96 µsec time step
- Some controls (Firing pulse generators) are also running at 0.96 µsec
- High level controls are running at 25 µsec.

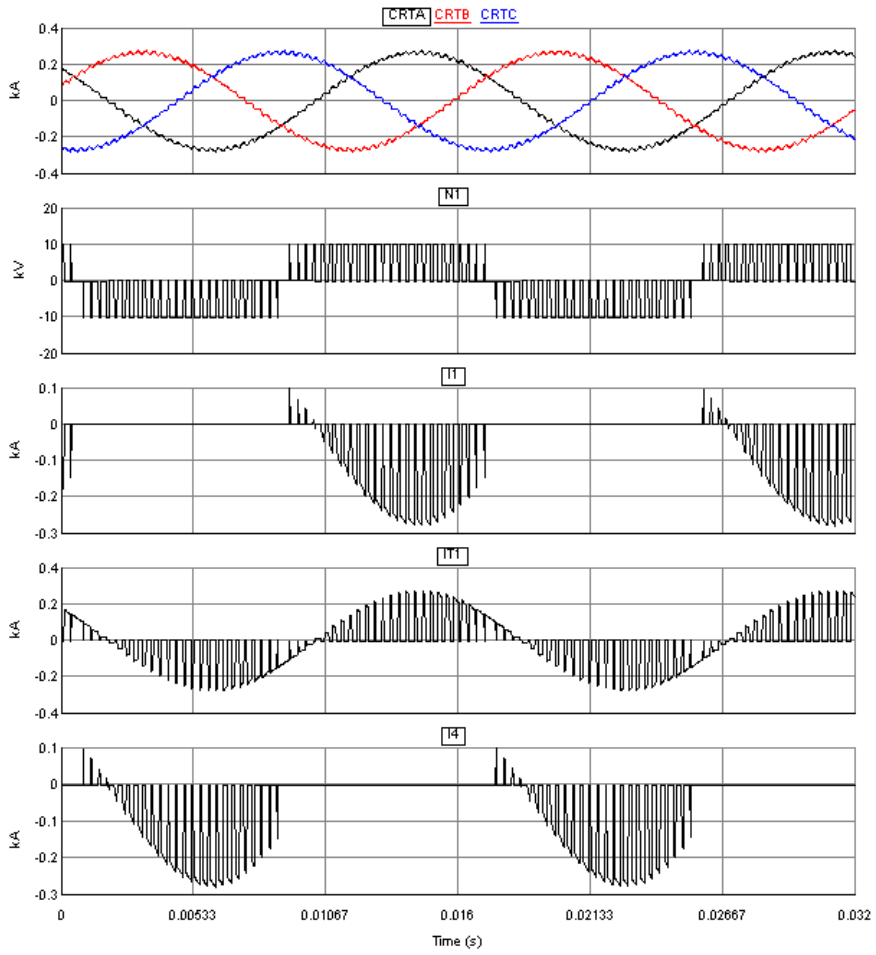
Simulation Results

Switching Frequency (Hz)	Losses (%)
3060	0.259
9900	0.333

- Losses likely lower then in real physical t-type converter
- Losses can be increased by modifying the ON and OFF resistances – **User configurable losses.**

Plots

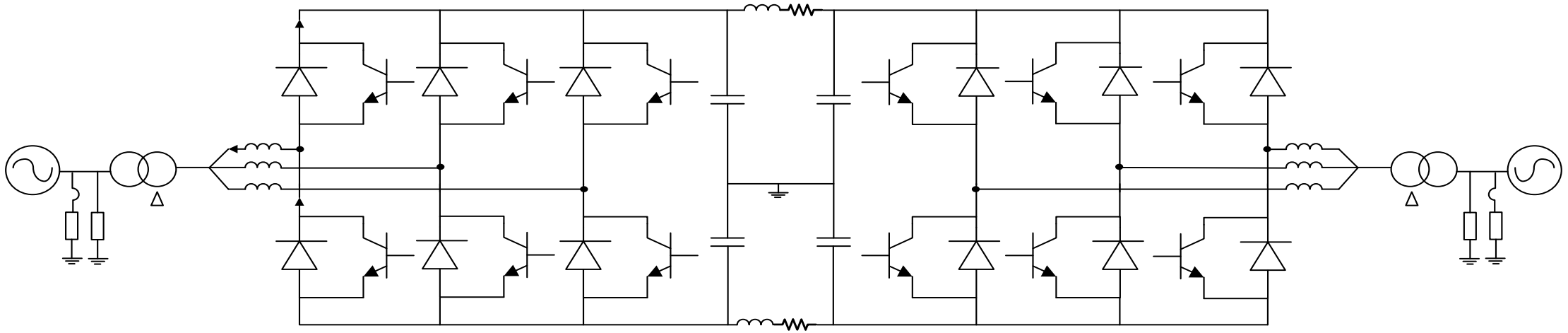
1) AC side load currents
2) Voltage of internal phase A node N1
3) Upward current through Valve 1
4) Current through Valve 2 and Valve 3 directed to the load
5) Upward current through valve 4.



3060 Hz switching frequency

Simulation Results

Case 2: Back to Back 3 phase 2 level VSC



- 28 nodes system
- 18 conductance values (12 IGBTs and 6 breakers)
- 22 nodes are connected to a switch resistive branch
- The entire circuit runs on a single core
- The entire circuit runs at **2.0** µsec times
- High level controls are at 35 µsec

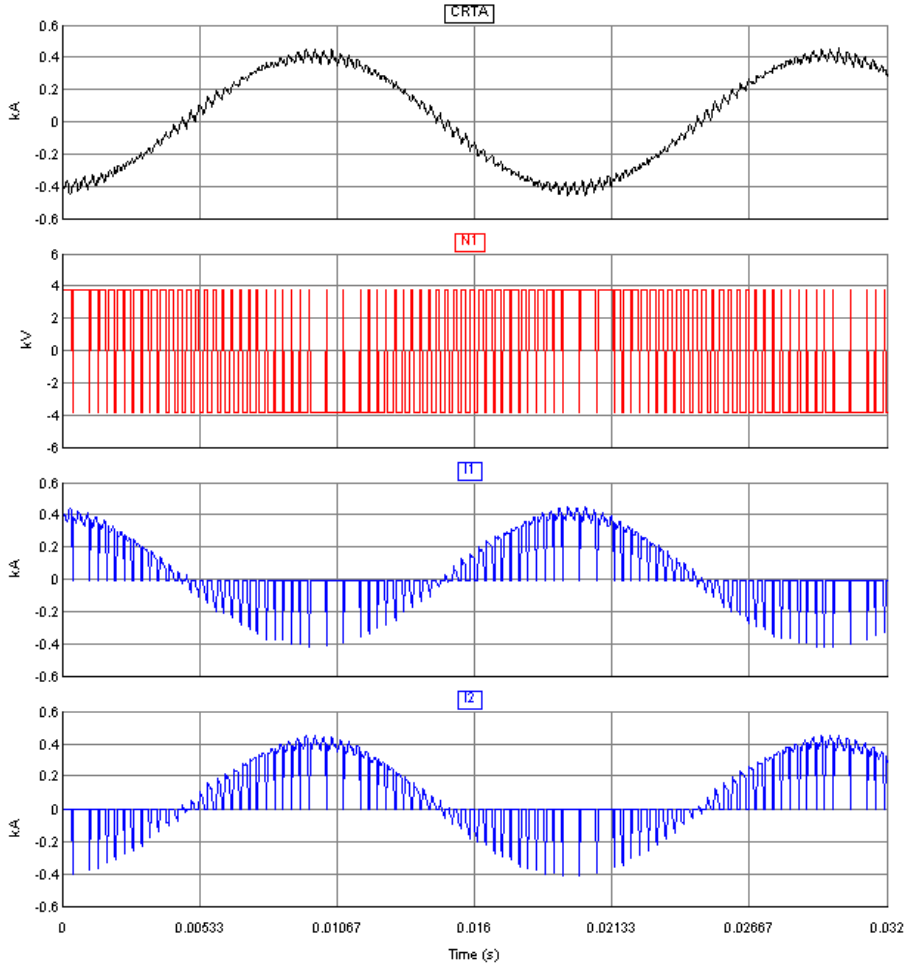
Simulation Results

Switching Frequency (Hz)	Losses (%)
3000	0.5
5000	0.51
10000	1.0

Losses can be increased by modifying the ON and OFF resistances – **User configurable losses**

Plots (left end of back to back)

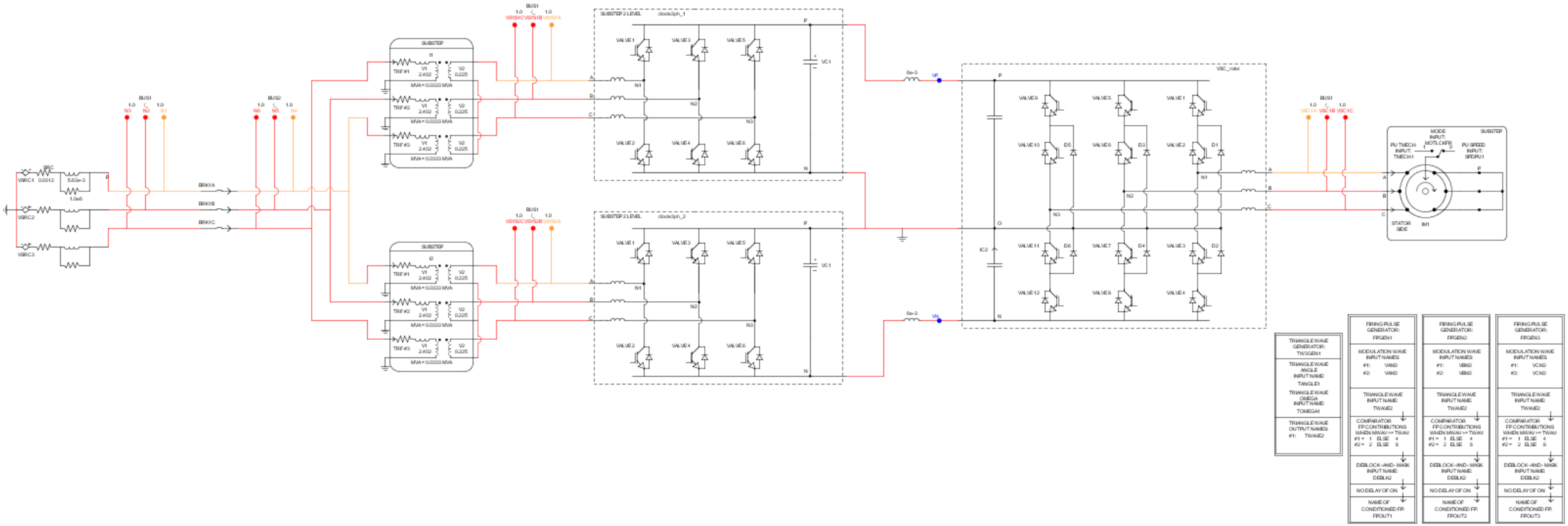
1) AC side phase A load current
2) Voltage of internal phase A node N1
3) Upper phase A valve current
4) Lower phase A valve current



3000 Hz switching frequency

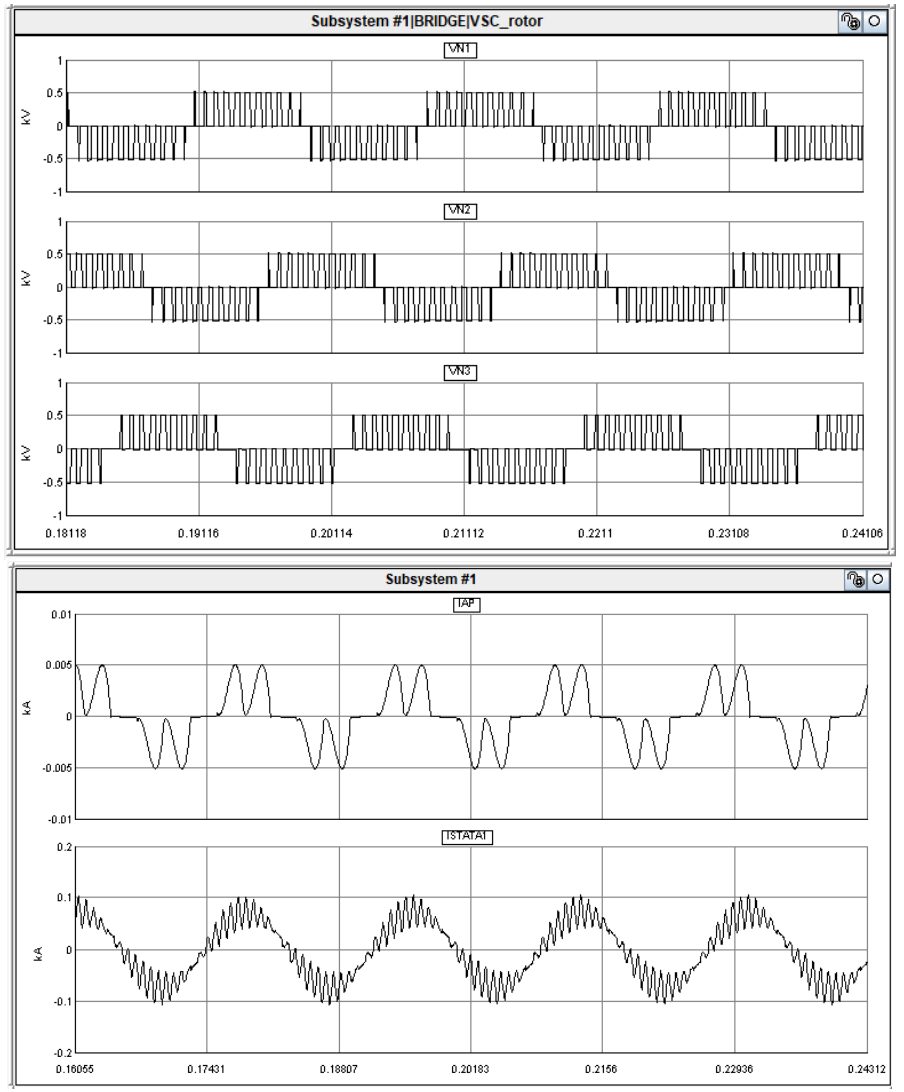
Simulation Results

Case 3: Induction Motor Drive



Simulation Results

- 26 Node system
- 24 switching devices
- 22 nodes connected to a switching branch
- Two 2-level 3 phase converter bridge
- One 3-level 3 phase NPC bridge
- Induction machine model
- The system can run in Substep at **2 µsec**



Summary

- There are several platforms to model power electronics circuits with the RTDS Simulator
  - Mainstep for LCC based converters (~30-60 µsec)
  - Small time step (1.4-3.75 µsec)
  - GPES for investigating new converters topologies (as lows ~400 nsec)
  - **Substep** for modelling networks with pure resistive switching (0.5 - 10 µsec)

- **Substep** offer the best environment to model power electronics circuits
  - Low losses that are user configurable
  - Clean waveforms
  - Time step size supports modelling of high frequency switching
  - Supports model from the Mainstep library

THANK YOU!
QUESTIONS?

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