DC Transformer Modelling & Simulation in RTDS Simulator

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AGENDA

- Background
- Operation and Control of DC Transformer
- DC Transformer Simulation in SUBSTEP
- DC Transformer Simulation in GPES
- Conclusions & Future Plan

Background

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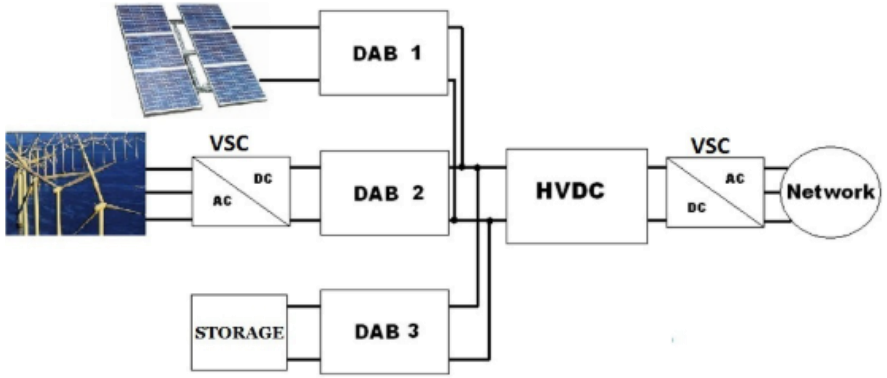
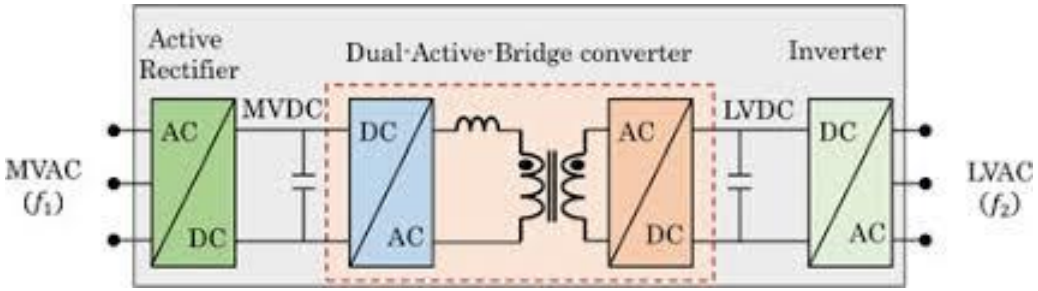
DC Transformer

- Power electronic transformer (PET)
- Isolation for input and output sides
- Bidirectional power flow if using fully-controllable switching devices
- High switching frequency → Reducing transformer's cost, volume and weight
- DC Transformer in series/parallel → Large system



Applications:

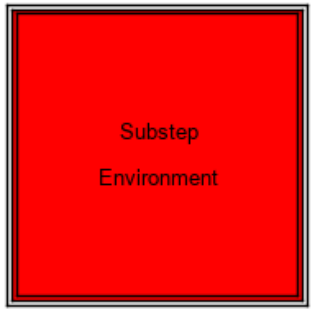
- Automotive
- DC grids
- Renewable energy conversion systems
- Integrating battery energy storage systems
- Medium-voltage or –power systems



Power Electronics Simulation Capability in RTDS

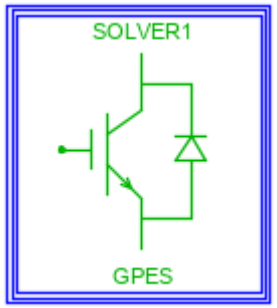
SubStep Simulation Environment

- Only available on NovaCor hardware platform
- No limit on the number of resistive switching elements*
- No fictitious losses*
- Full decomposition allows accurate calculations



GPES Simulation Environment

- A generic PE solver platform on GTFPGA
- Uses powerful parallel processing power of FPGA
- Can model power circuits with arbitrary circuit configurations
- Larger network (128 nodes and 256 branches) and smaller time step (400^{+} ns), e.g., dc breaker needs 110+ nodes and 200+ switches



Operation and Control of DC Transformer

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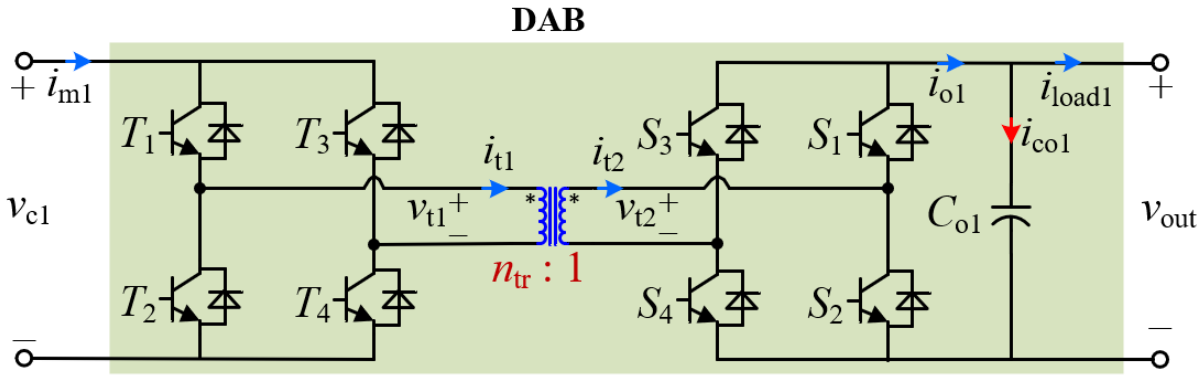
Dual-Active Bridge (DAB) Converter

Operation:

- Considering square-wave operation at both transformer's sides

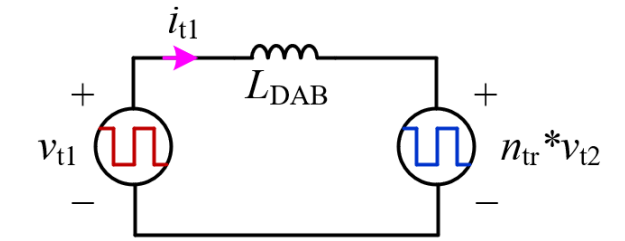


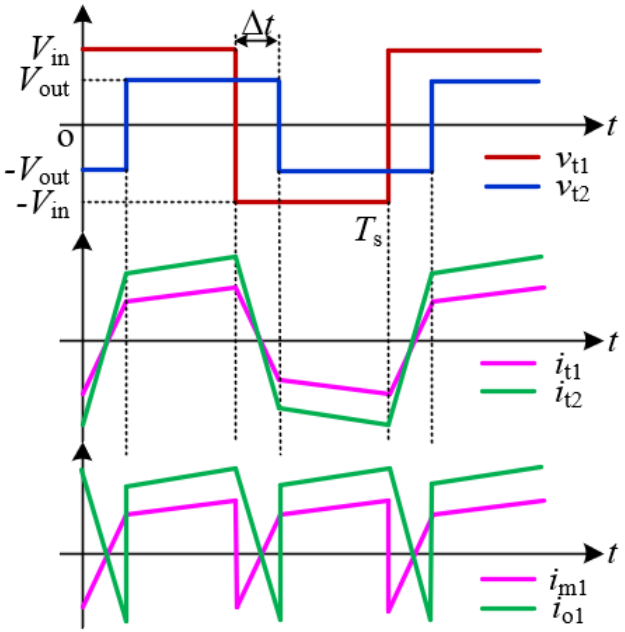
$$P_{DAB1} = \frac{V_{in} \cdot V_{out} \cdot n_{tr}}{2\,\pi \cdot f_{sw} \cdot L_{DAB}} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right)$$

$0 < \varphi < \pi$, $P_{DAB1} > 0$: power delivered from v_{t1} side to v_{t2} side

$-\pi < \varphi < 0$, $P_{DAB1} < 0$: power delivered from v_{t2} side to v_{t1} side

→ Overall, the power is delivered from leading phase side to lagging phase side.





Phase shift angle: $\varphi = 2\pi f_{sw}\Delta t$

$\varphi > 0$ → v_{t1} leading v_{t2}

$\varphi < 0$ → v_{t1} lagging v_{t2}

$I_{m1\_avg} = I_{o1\_avg}/n_{tr}$

Leakage Inductance of Transformer

Design consideration of leakage inductance:

- Considering all the inductance provided by transformer's leakage inductance
- DAB real power < transformer's MVA to avoid overload for transformer
- $V_{in} = k_1 * V_{tr1}$, and $V_{out} = k_2 * V_{tr2}$

DAB real power:

$$P_{DAB1} = \frac{V_{in} \cdot V_{out} \cdot n_{tr}}{2\ \pi \cdot f_{sw} \cdot L_{lk}} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right) < S_{tr}$$

$$\Rightarrow \quad \frac{V_{in} \cdot V_{out}}{V_{tr2}^{\ 2}} \cdot \frac{1}{X_{lk} \cdot n_{tr}} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right) < 1$$

- Typically, in rated operation, $V_{in} = V_{tr1}$, and $V_{out} = V_{tr2}$, i.e., $k_1 = 1$, $k_2 = 1$, $n_{tr} = V_{in}/V_{out}$

TR's turns ratio:

$$\frac{V_{tr1}}{V_{tr2}} = n_{tr}$$

TR's leakage inductance:

$$X_{lk} = 2\ \pi \cdot f_{sw} \cdot L_{lk} = \frac{X_{tr} \cdot V_{tr1}^{\ 2}}{S_{tr}}$$

$$\Rightarrow \quad X_{tr} > \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right)$$

Input and output voltage:

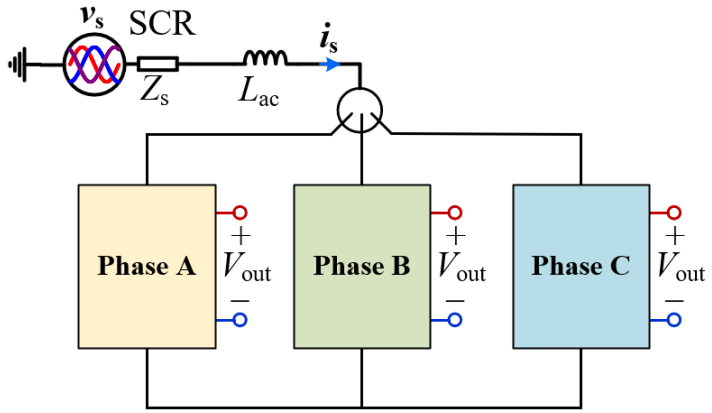
$$V_{in} = k_1 \cdot V_{tr1} \qquad V_{out} = k_2 \cdot V_{tr2}$$

$$If \qquad \varphi_{sel} := 25\ deg \qquad \varphi_{sel} \cdot \left(1 - \frac{|\varphi_{sel}|}{\pi}\right) = 0.376$$

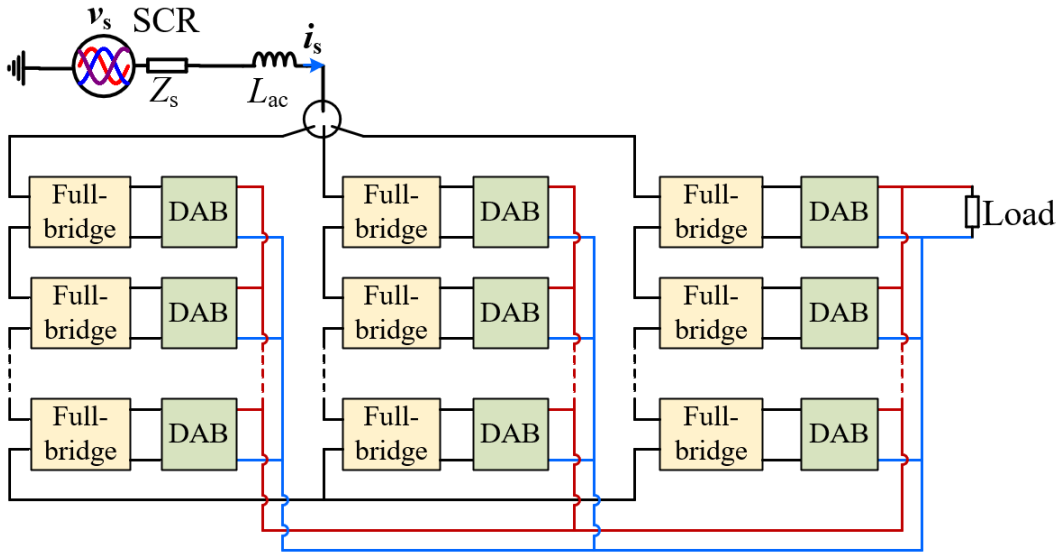
$$X_{tr} > 0.376\ pu$$

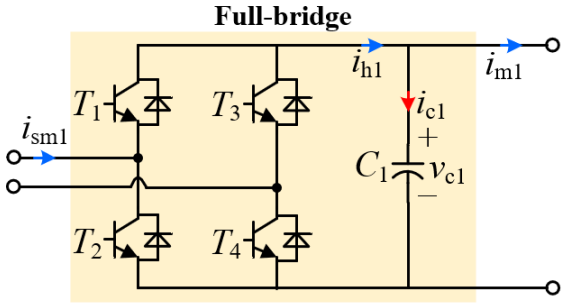
X_{tr}: transformer's leakage inductance in p.u.

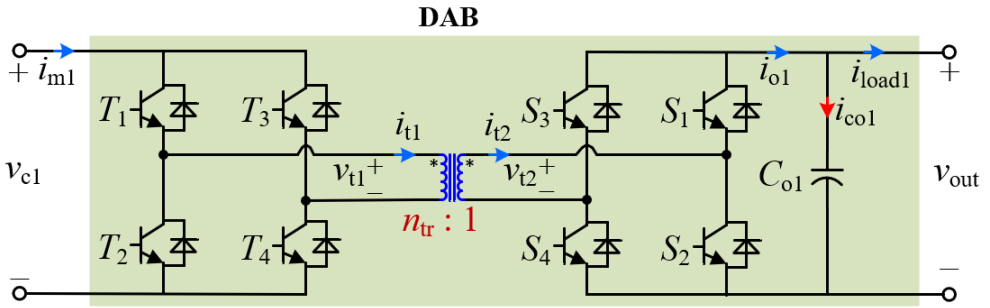
Application: AC Grid → MMC → DAB → Load



Full-bridge + DAB







H-bridge AC-DC stage:

- **Similar to control requirements of conventional MMC**
  - **Real power or capacitor voltage controls**
  - **Capacitor voltage balancing control**

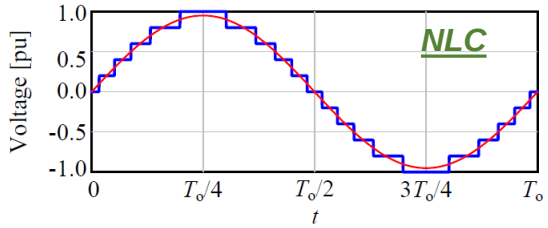
DAB power/voltage control:

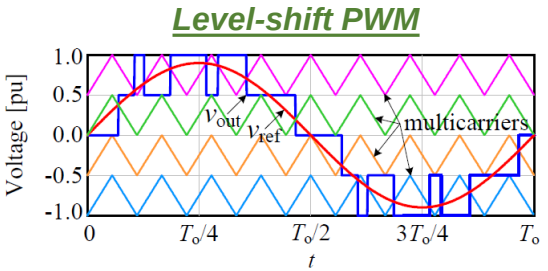
- **It adjusts phase shift between v_{t1} and v_{t2}**

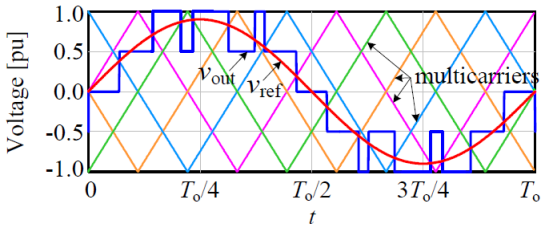
Capacitor Voltage Balancing Control

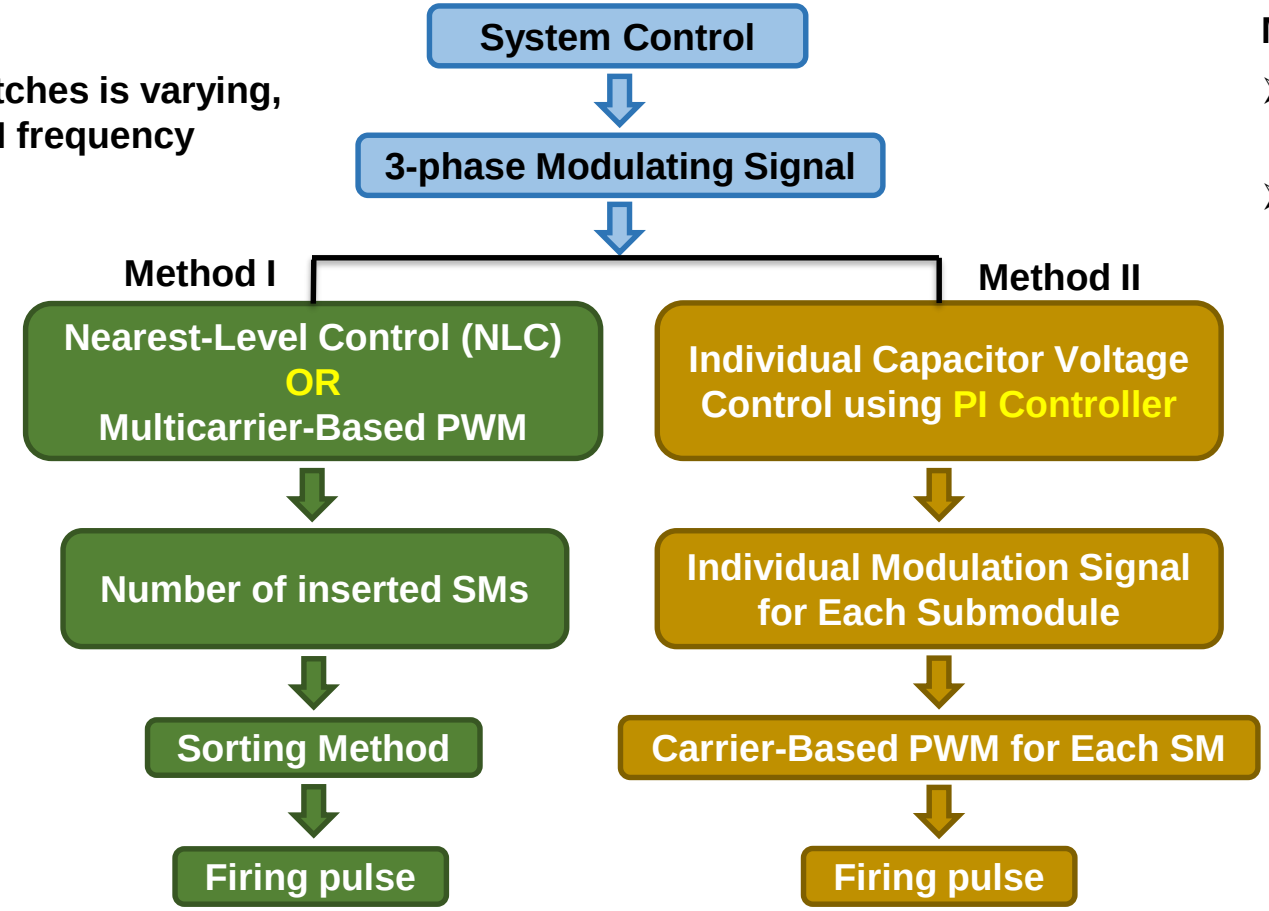
Method I:

- Switching frequency for Switches is varying, maximum at equivalent PWM frequency
- No needs of PI parameters



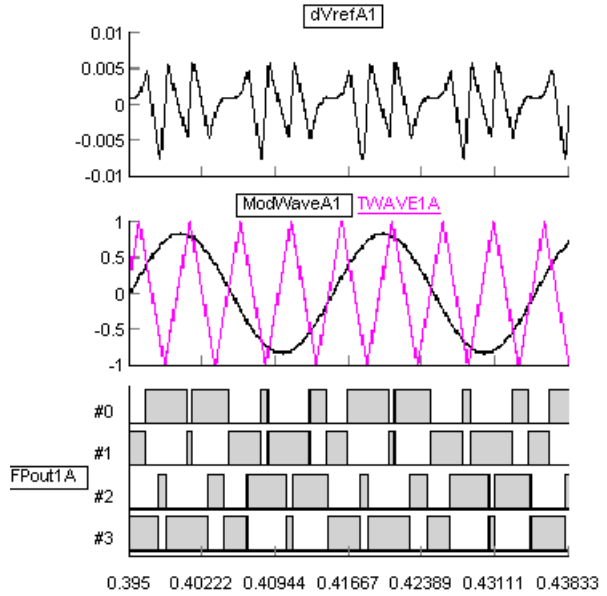






Method II:

- Switching frequency for Switches is fixed at carrier frequency
- It needs to design PI parameters

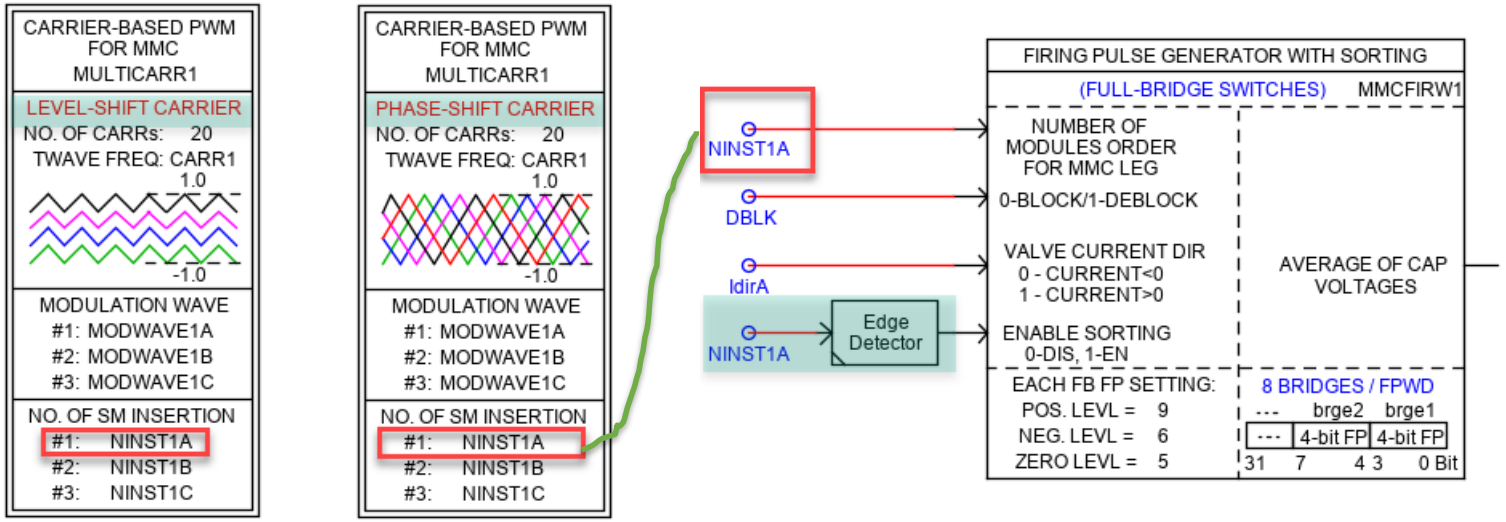


NLC: **mainly used for a large number of submodules**
Multicarrier-based PWM: **can be used for either a large or small number of submodules**

NEW Control Component Development for Capacitor Voltage Balancing – (SORTING METHOD)

- **Multicarrier-based PWM**
- **Firing Pulse Generator with Sorting**

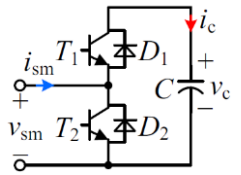
- It supports up to 32 submodules in series
- It supports Level- or Phase-shift PWM
- Firing pulse arrangement in a word supports customer-specified
- It supports firing pulses for Half- or Full-bridge submodule switches and CHAINV5 MMC Model



For Half-bridge with switches

Name	Description	Value	Unit	Min	Max
poslevlhb	FP Value for Positive Voltage Level Output:	1		0	3
zerolevlhb	FP Value for Zero Voltage Level Output:	2		0	3

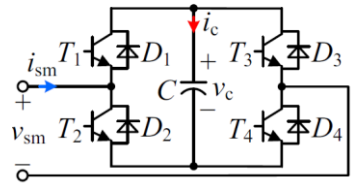
Level	T2	T1	Value
Pso	0	1	1
Zero	1	0	2



For Full-bridge with switches

Name	Description	Value	Unit	Min	Max
poslevlfb	FP Value for Positive Voltage Level Output:	9		0	15
neglevlfb	FP Value for Negative Voltage Level Output:	6		0	15
zerolevlfb	FP Value for Zero Voltage Level Output:	5		0	15

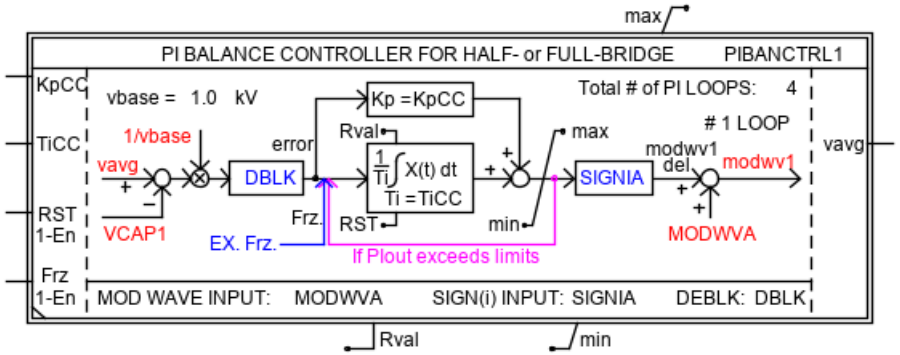
Level	T4	T3	T2	T1	Value
Pso	1	0	0	1	9
Neg	0	1	1	0	6
Zero	0	1	0	1	5
	1	0	1	0	10



NEW Control Component Development for Capacitor Voltage Balancing – (PI CONTROL METHOD)

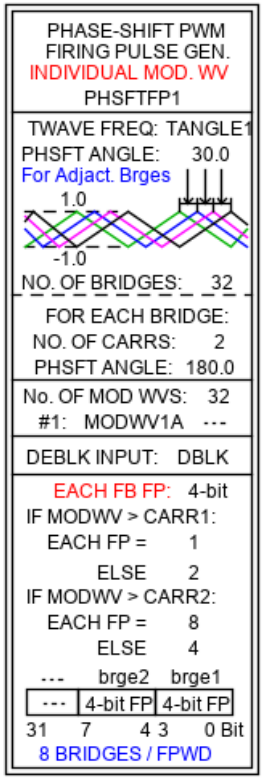
➢ Multiple PI Controller

- It supports up to 32 PI control loops
- PI controller configuration supports RESET, FROZEN, and LIMITS
- It outputs individual modulation signal for each submodule



➢ Flexible Phase-Shift PWM Firing Pulse Generator

- It supports various PWM pattern:
  - ONE modulation signal with multiple carriers
  - Individual modulation signal with each carrier
  - One or Two carriers for each modulation signal
- Firing pulse arrangement in a word supports customer-specified
- It supports firing pulses for Half- or Full-bridge submodule switches and CHAINV5 MMC Model



Name	Description	Value	Unit	Min	Max
Name	PHASE-SHIFT PWM FP GENERATOR NAME:	PHSFTFP1v2			
brgetype	Firing Pulse to Drive Half or Full Bridge?	Full		0	1
numbrge	No. of Bridges:	32		0	32
modeltype	Bridge Model: Separate Switches or CHAINV5?	Separate Switches		0	1
modwvtype	No. of Modulation Waves to All Bridges:	One		0	1
numcarr1	No. of Carriers for Each Bridge:	One / Individual		1	2
phsft1	-- IF 2 Carriers, Phase Shift (>0 lead, <0 lag):		Degrees	-360.0	360.0
ndeblk	Overall De-block Signal (0-blk,1-deblk) Name:	DBLK			

DC Transformer Simulation in SubStep

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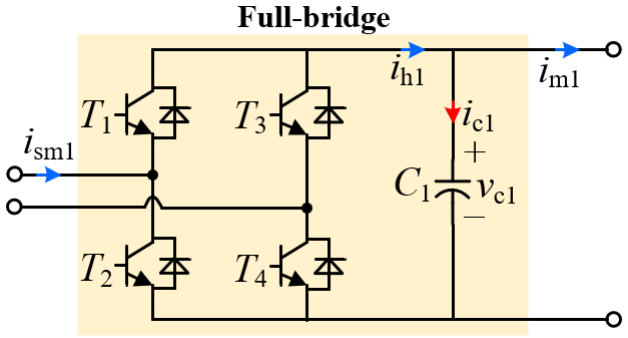
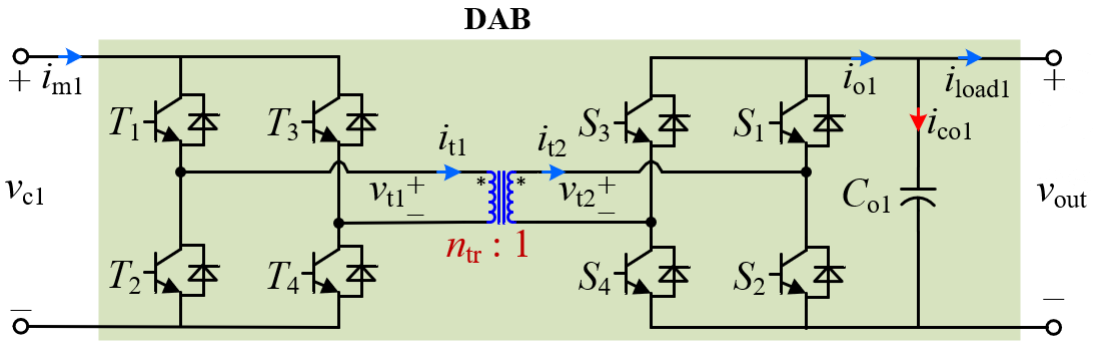
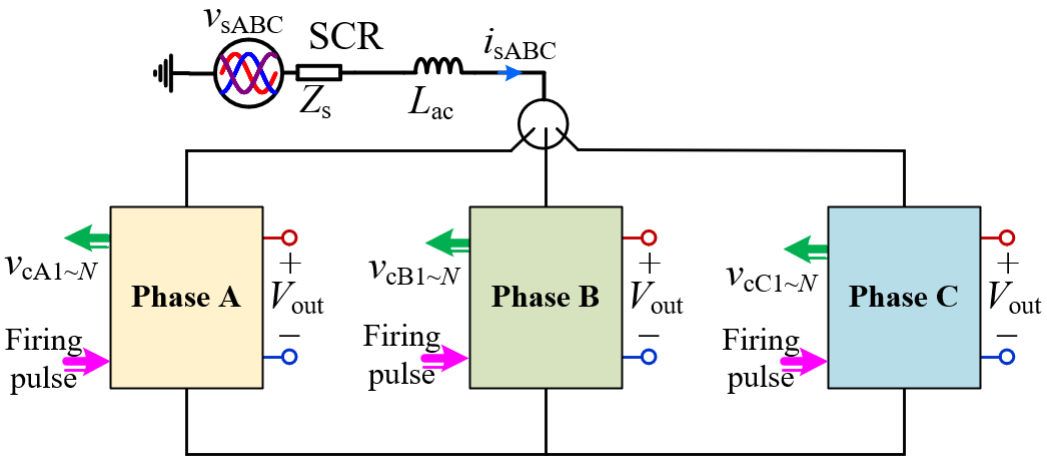
System Parameters

Parameter	AC-DC Stage	DC Transformer (DAB)
# of modules	6 Full-bridge SMs in series	6 DABs in parallel
AC grid	10 kV (LL, rms), 50 Hz, Z_s = 3.5 Ω + $j\omega_0$*0.1 mH	N/A
DC output	1.5 kV, 4700 uF / Full-bridge	1.5kV, 50 uF / DAB
PWM modulation	Unipolar dual-frequency SPWM	Phase-shift PWM with duty = 0.5 (square-wave)
Carrier frequency	200 Hz	1.0 kHz
Transformer	N/A	1.5 kV:1.5 KV, 0.125 MW, 1.0 kHz, 36.7% leakage
Cap Voltage Balancing	**PI control balancing method**	N/A
Real power	2.25 MW	



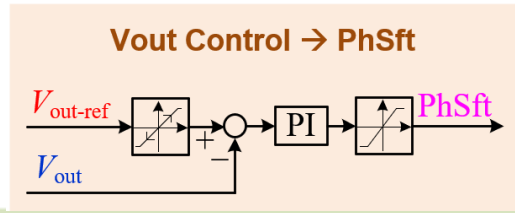


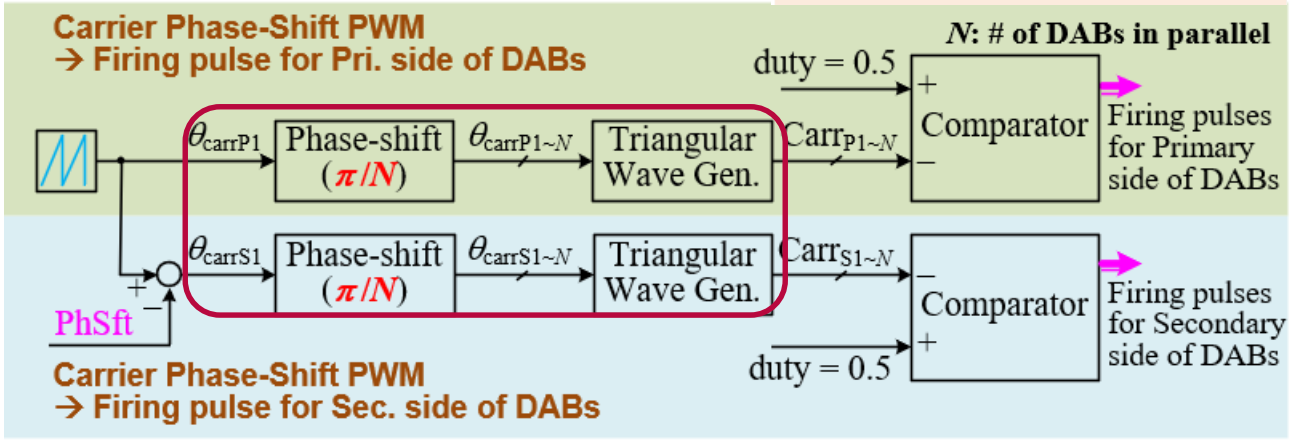
System Control



DABs:

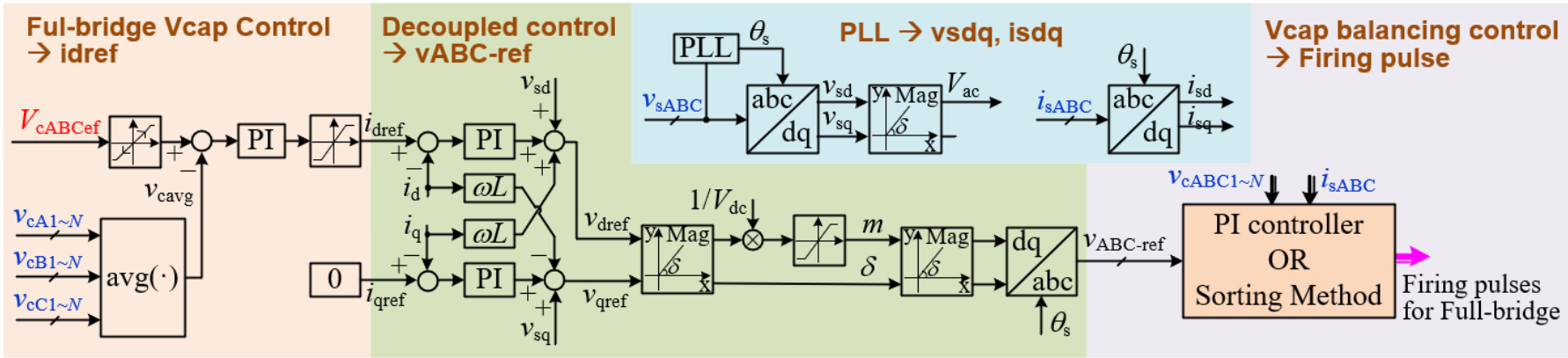
- **Output voltage control**: generate Phase Shift for two sides of one DAB
- **Parallel operation**: use phase-shift PWM to increase harmonic frequency
- **Square-wave operation**: duty = 0.5



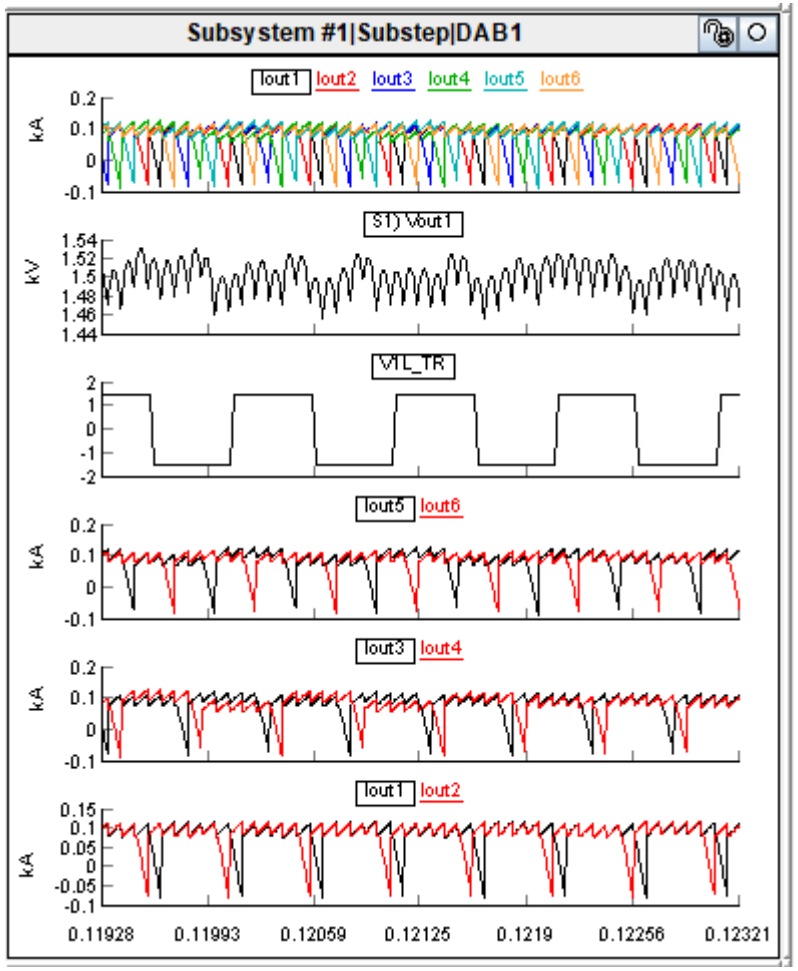


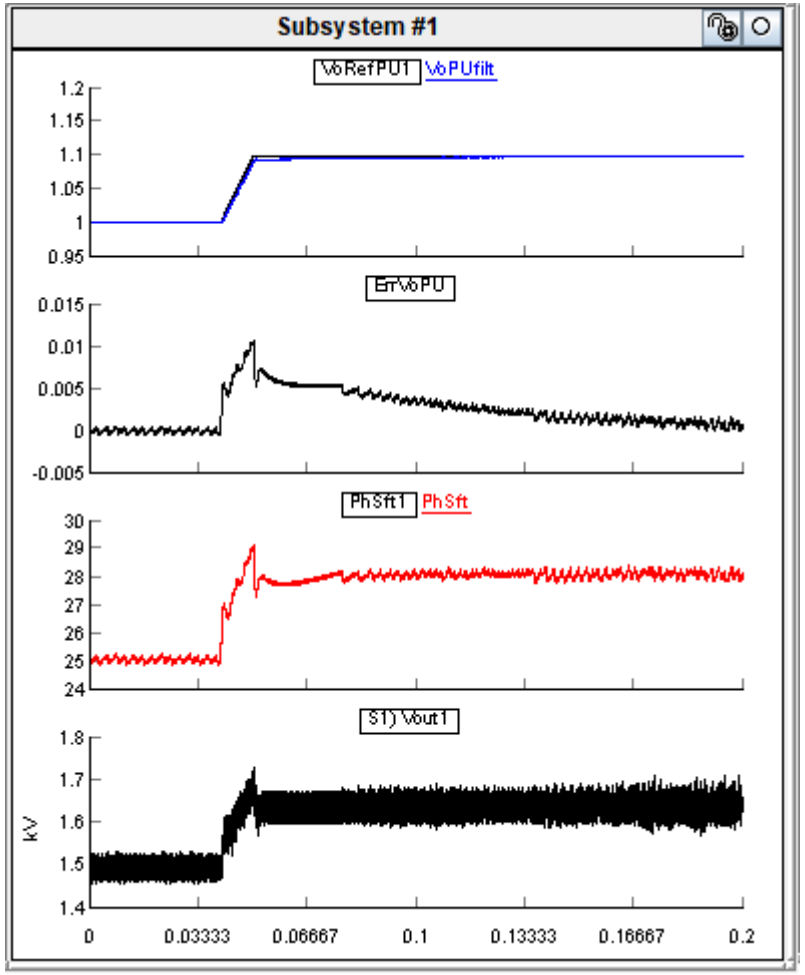
AC-DC stage:

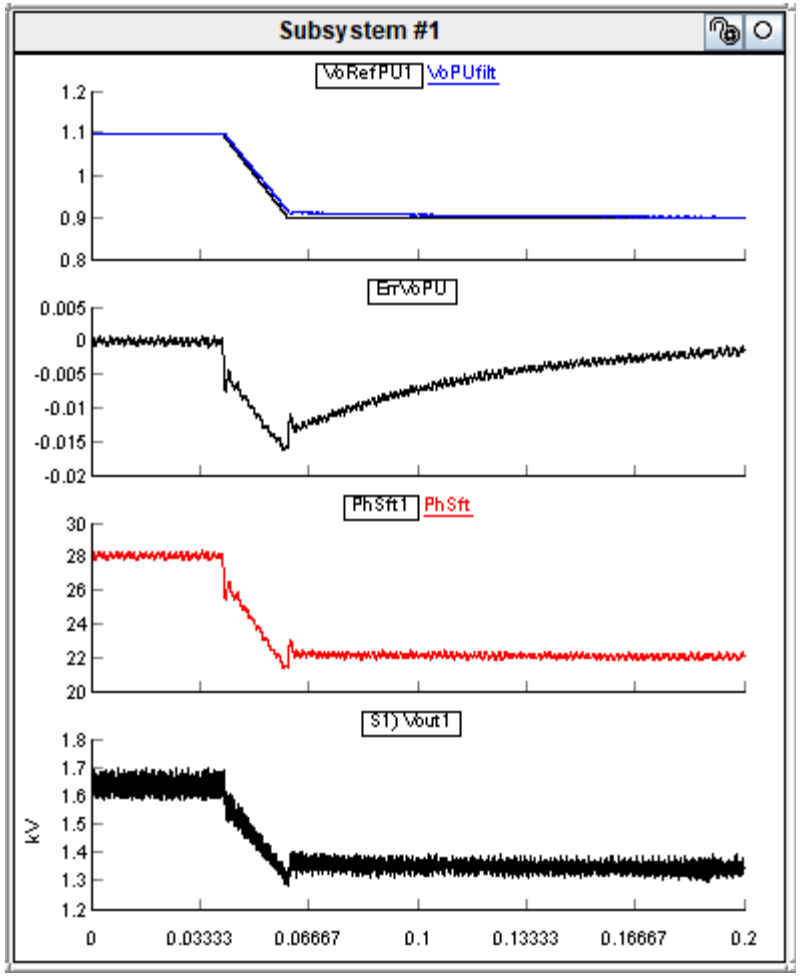
- **Vcap control + current decoupled control**: generate 3-phase references
- **Vap balancing**
- **PWM method**: Unipolar dual-frequency SPWM



Phase-Shift PWM for DABs in Parallel Operation



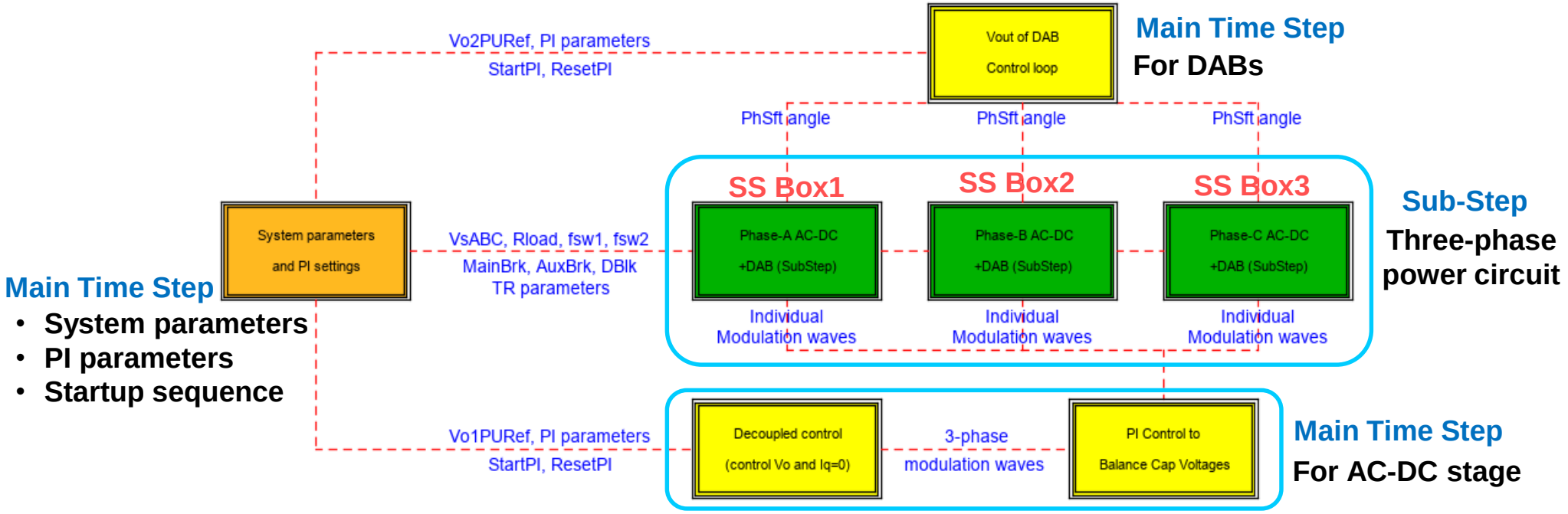




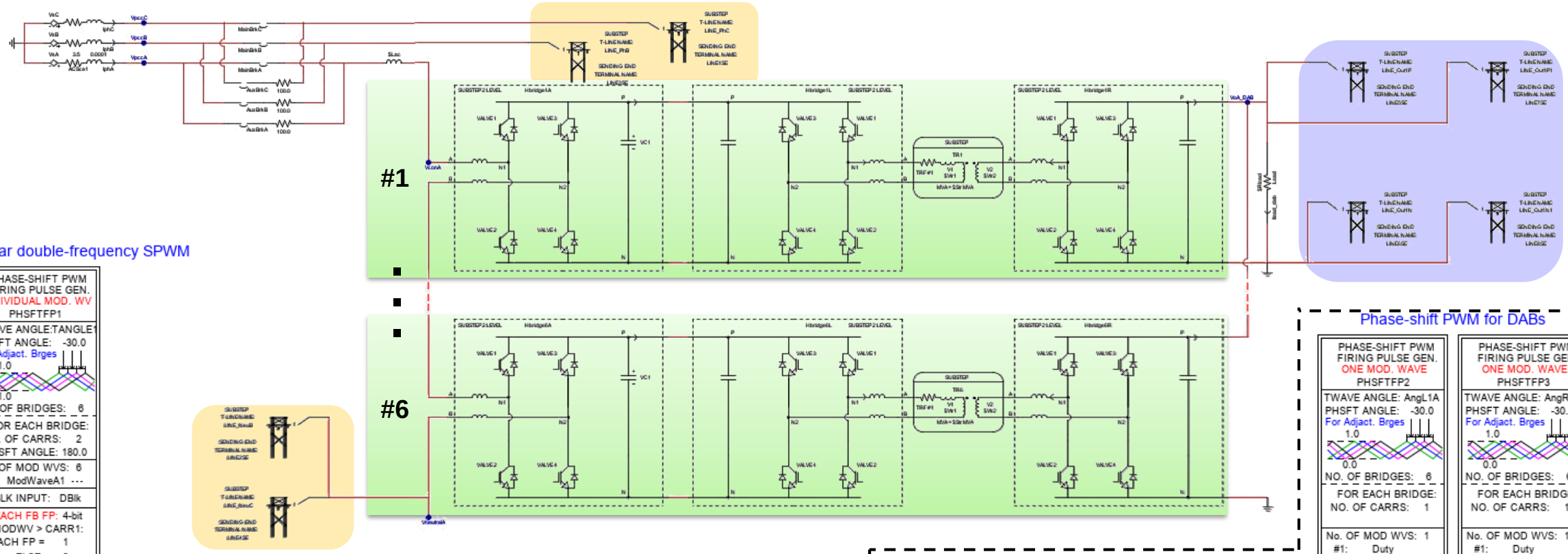
The paralleled output voltage and current harmonic frequency is significantly increased, which potentially permits the decrease of output capacitance.

SUBSTEP Simulation (AC-DC + DAB)

- Resistive switching model
- Main time step: 45 us
- Sub-timestep: 45 us/5 = 9 us
- # of modules per phase: *N* = 6 (18 H-bridges + 6 Transformers)/phase
- Substep box: 112 models, 53 nodes

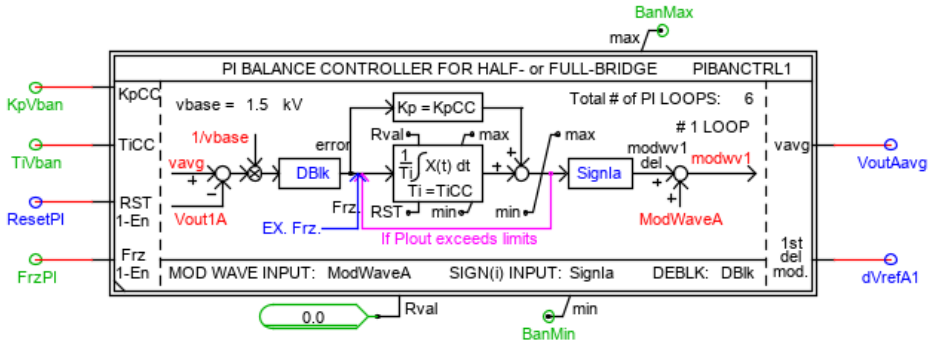


Circuit in One SubStep Box and Firing

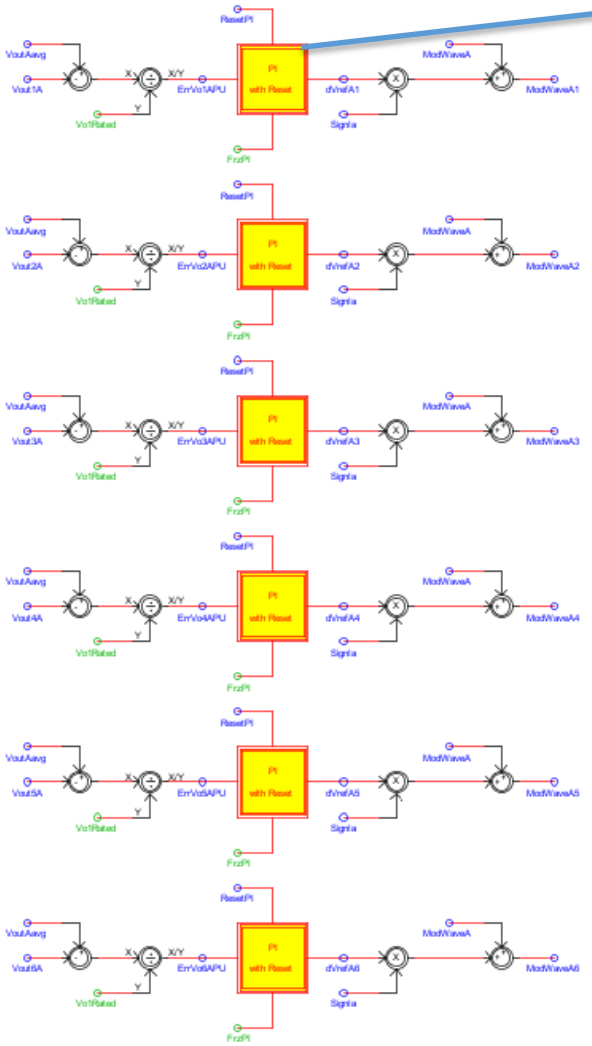


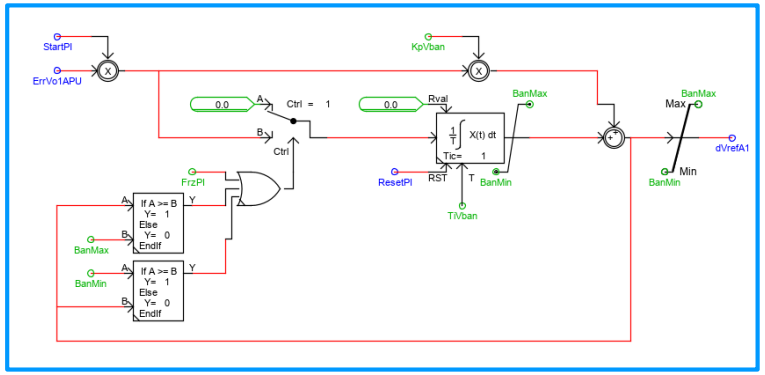
# of Modules: 6

Phase-A Capacitor Voltage Balancing PI Control Implementation



Using newly developed control component





Using existing components in RSCAD Lib

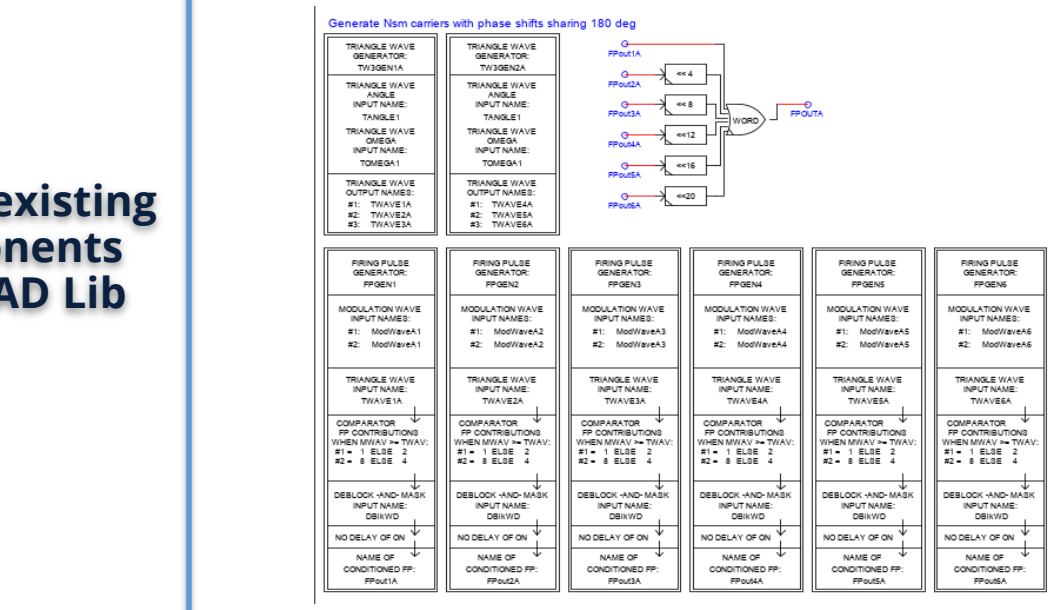
Phase-Shift PWM Firing Pulse Generation

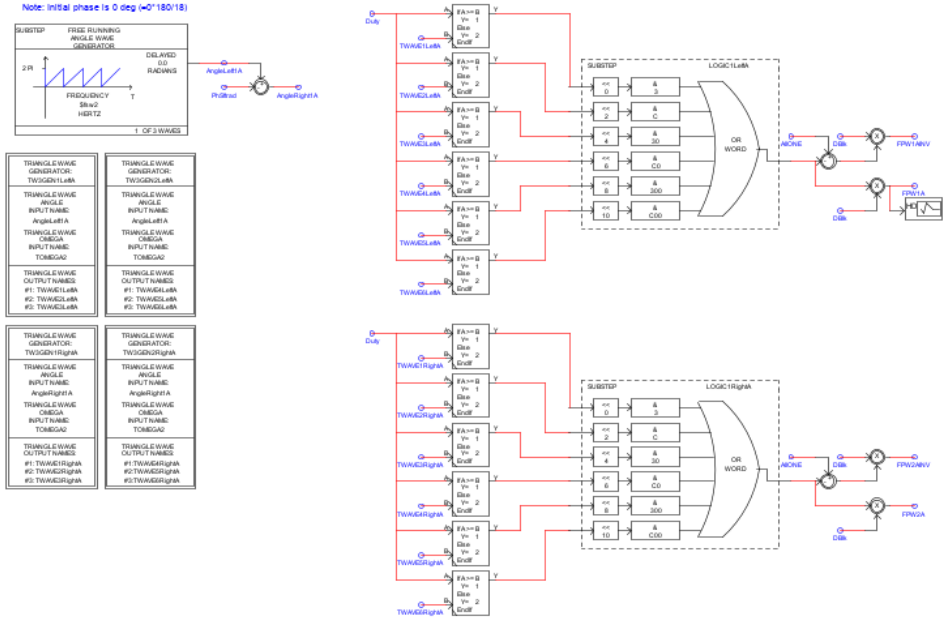
For 6 modules/phase

For AC-DC stage

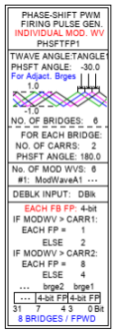
For DAB stage

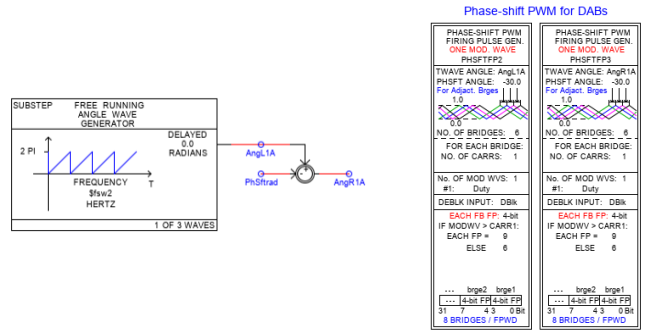
Using existing components in RSCAD Lib





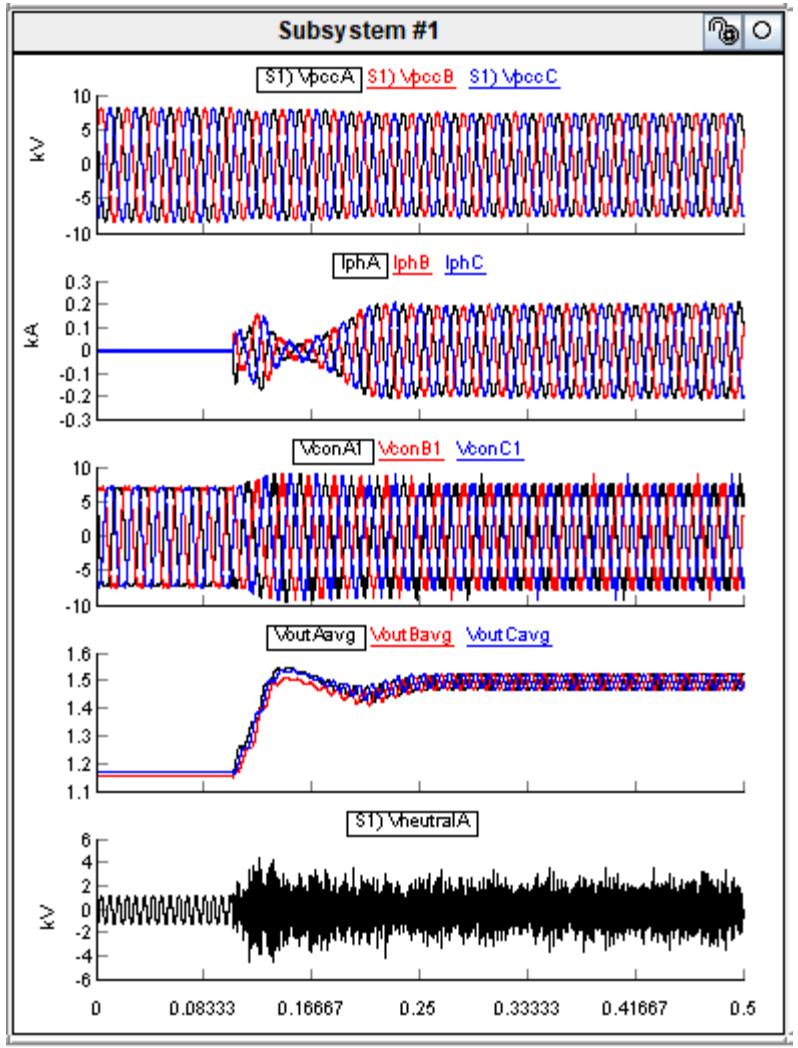
Using newly developed component



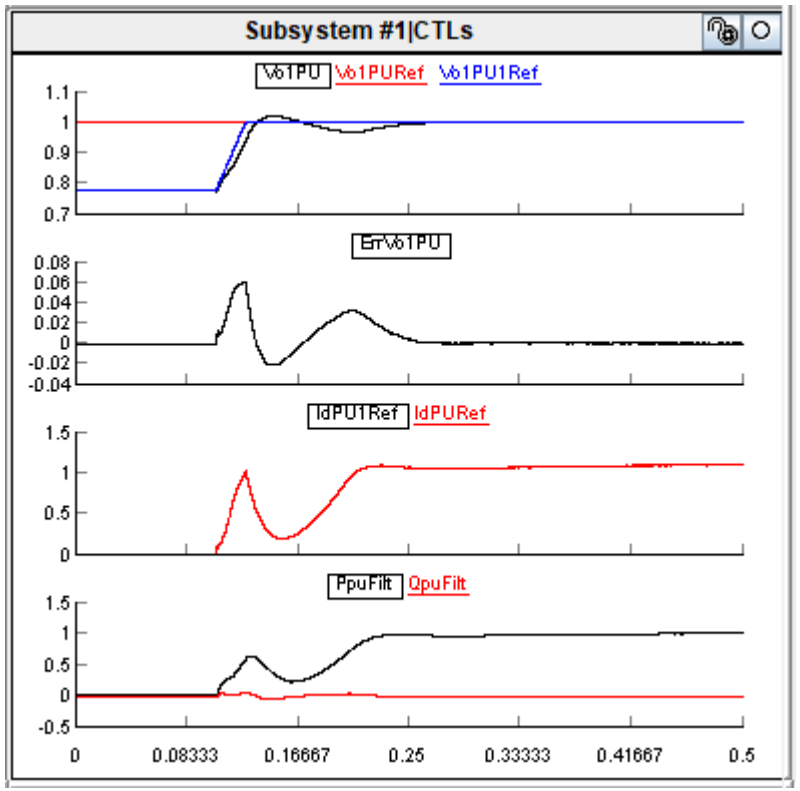


SUBSTEP Simulation Results

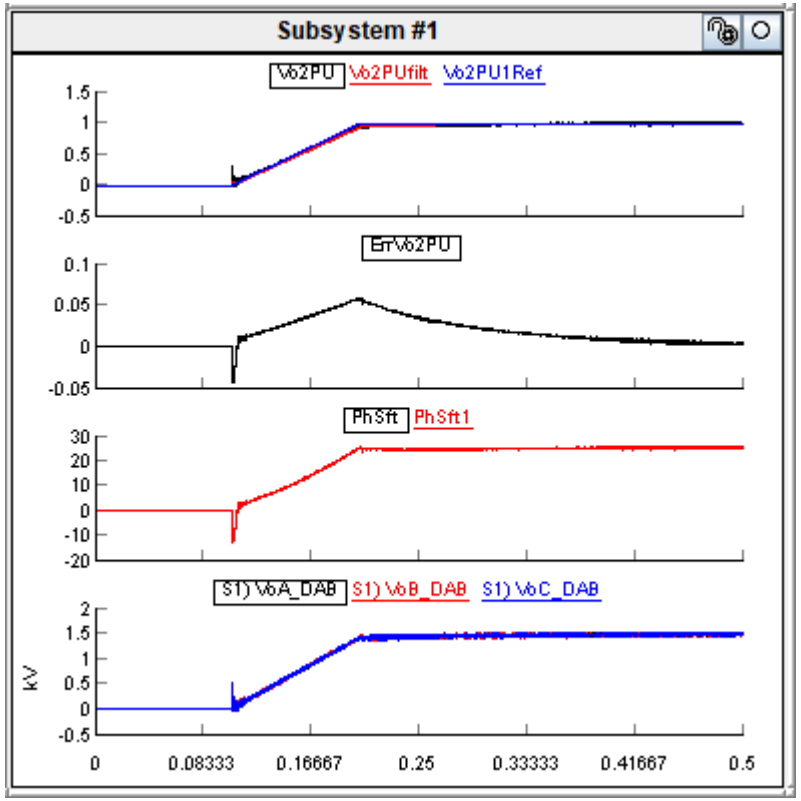
Blocking → Deblocking



AC-DC stage operating waveform



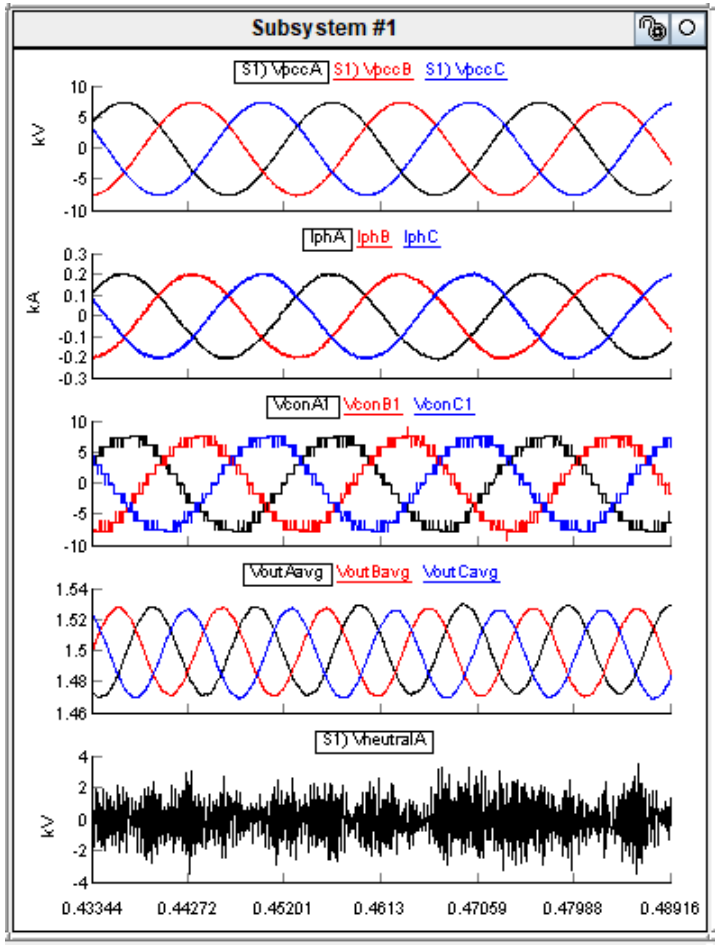
AC-DC stage Vcap control loop



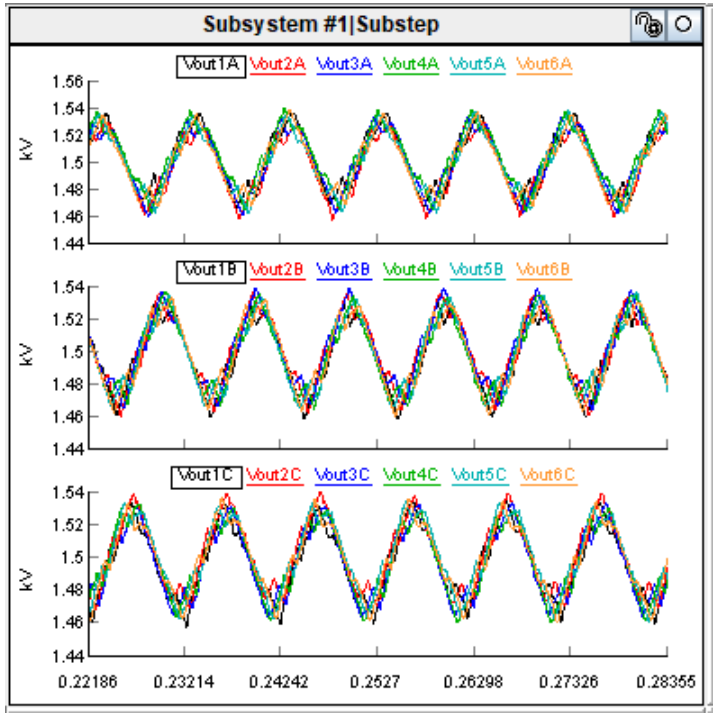
DAB output voltage control loop

SUBSTEP Simulation Results

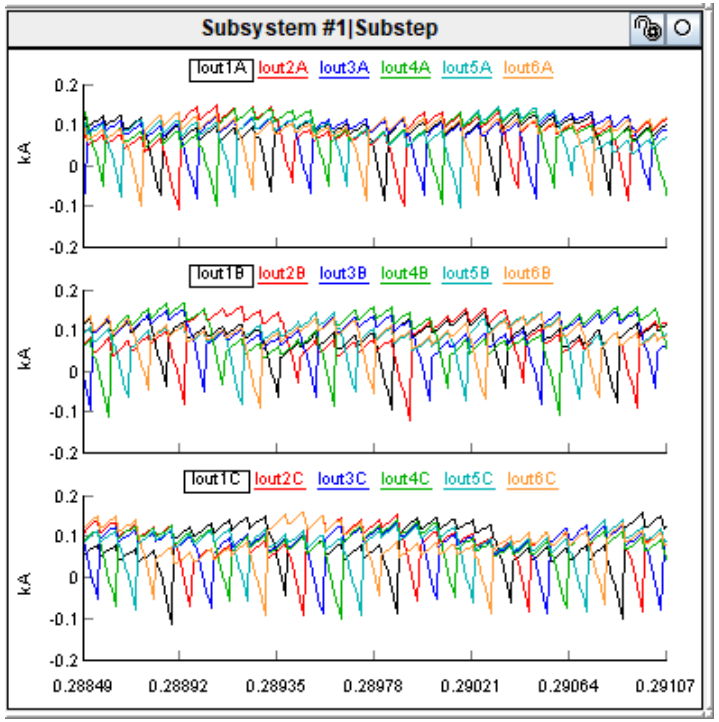
Steady-state operation: Vout = 1.0 pu → Po = 2.25 MW



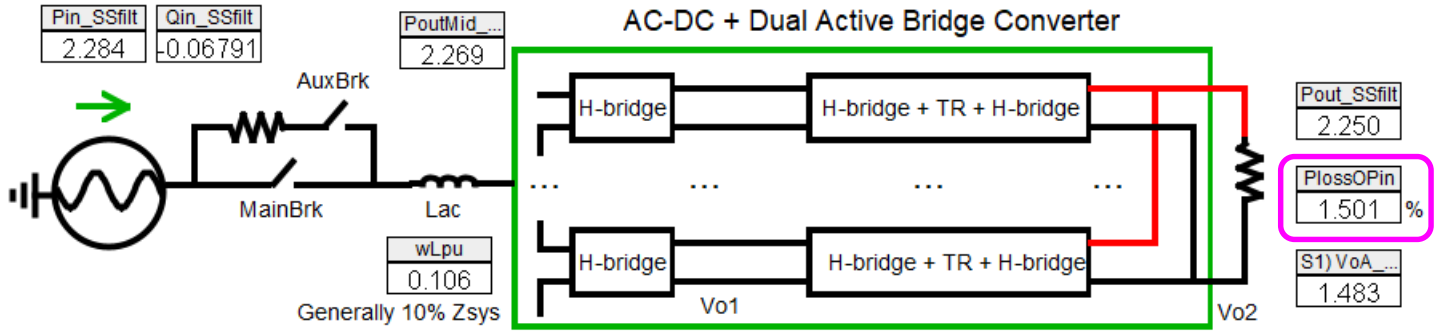
AC-DC stage operating waveform



Cap voltages in AC-DC stage

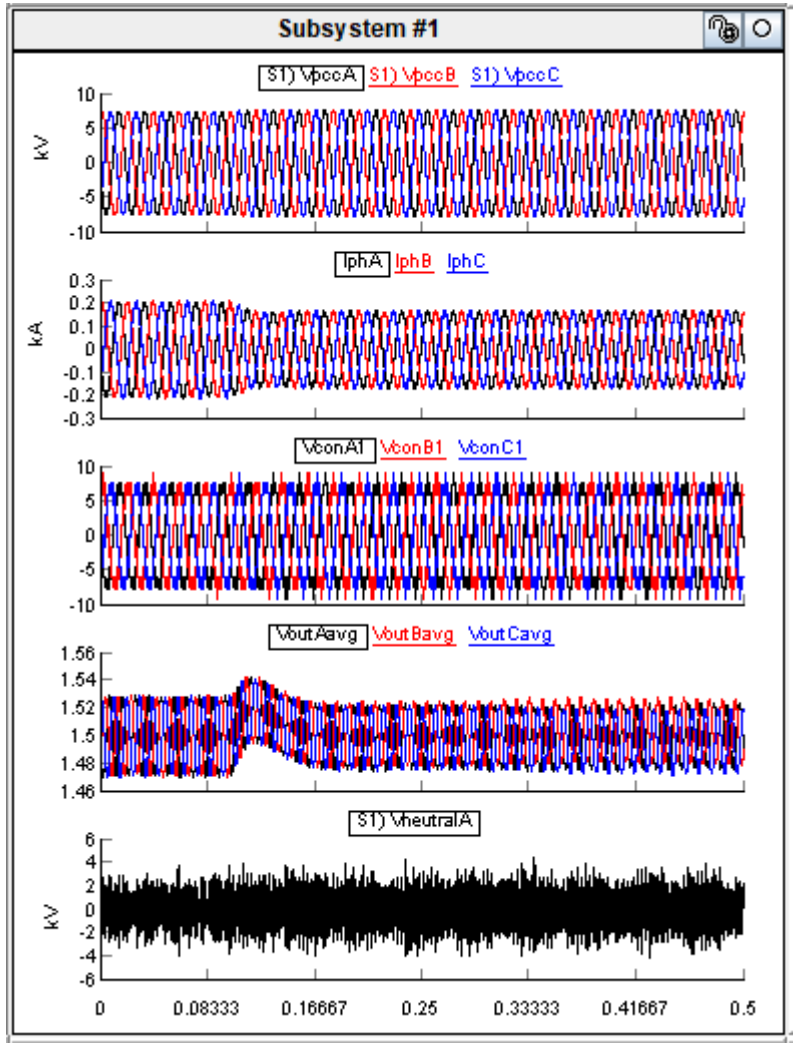


DAB output waveforms

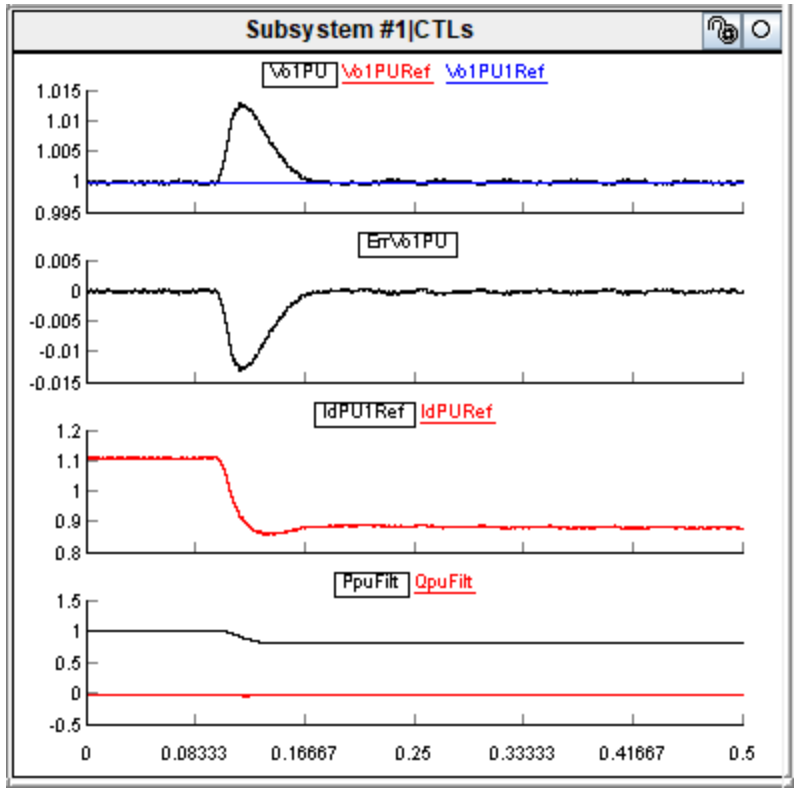


SUBSTEP Simulation Results

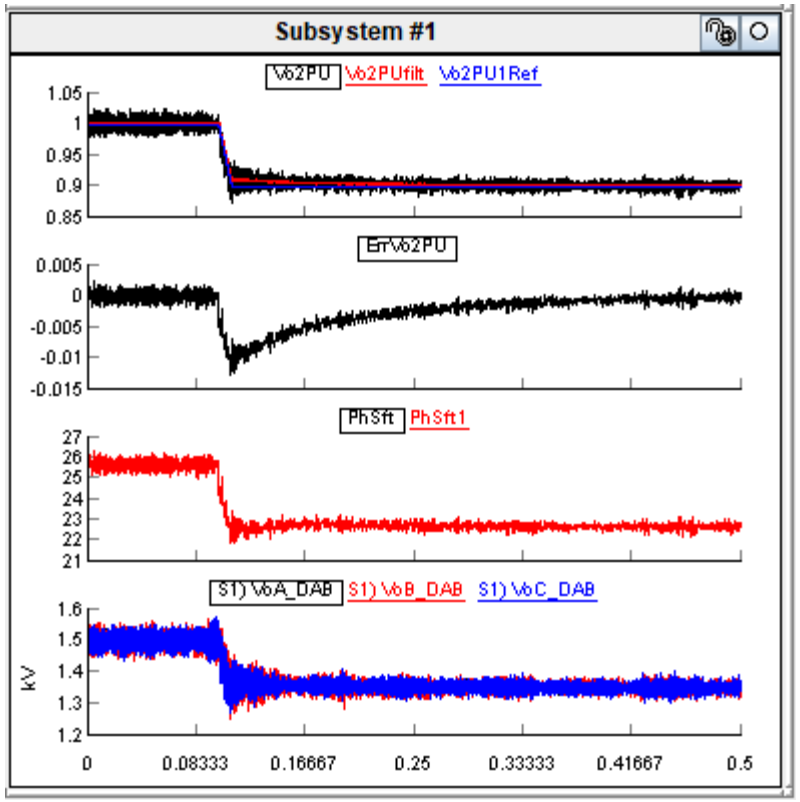
Dynamic operation: Vout = 1.0 pu → 0.9 pu



AC-DC stage operating waveform



AC-DC stage Vcap control loop



DAB output voltage control loop

DC Transformer Simulation in GPES

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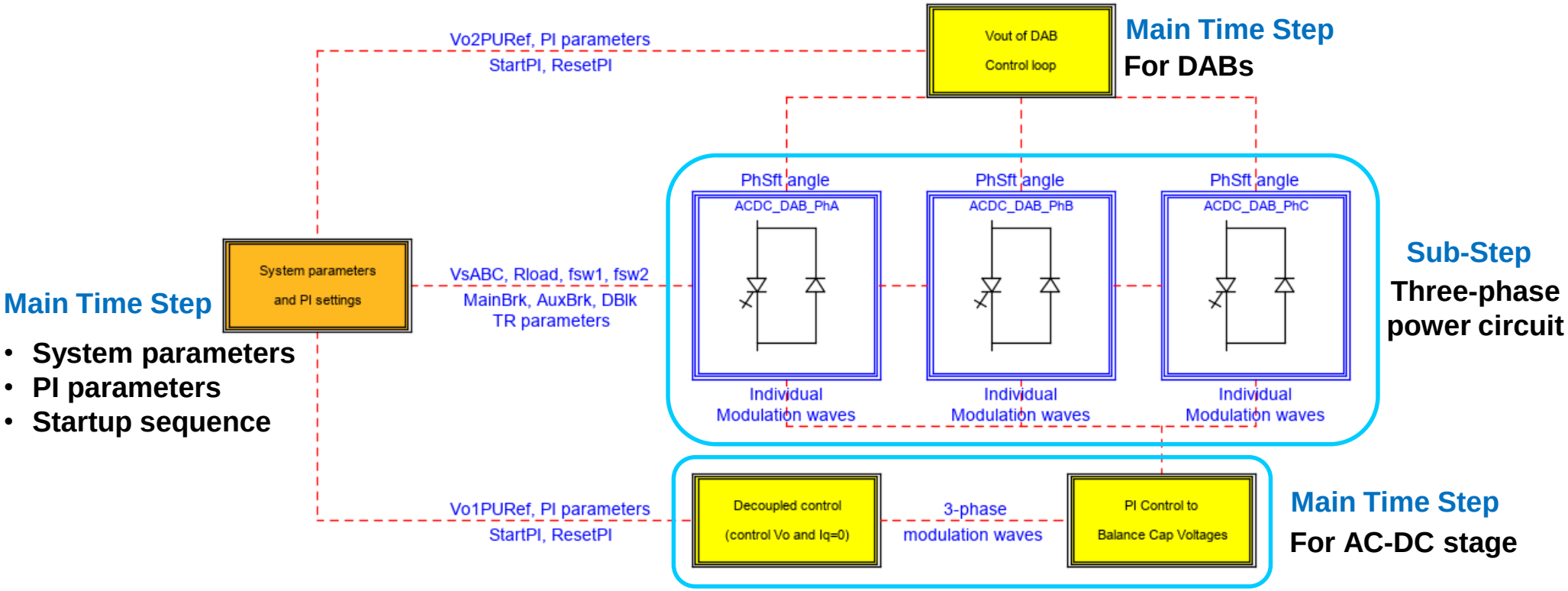
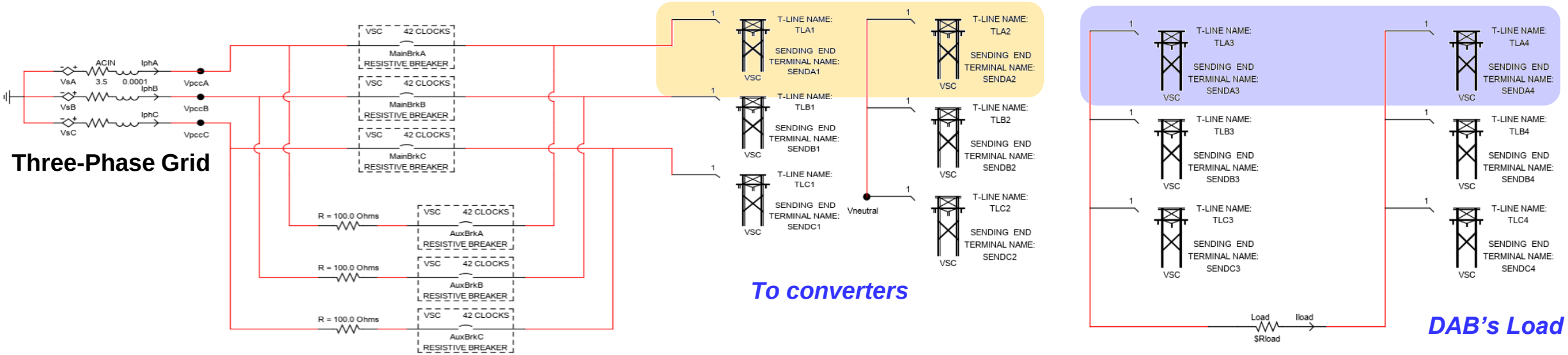
GPES Simulation in Small-dt Box (AC-DC + DAB)

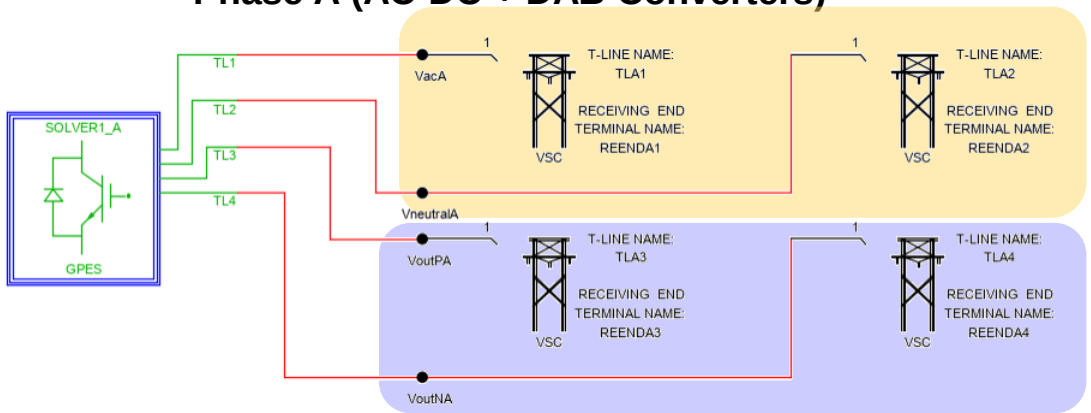
- Main time step: 45 us
- Small timestep: 2.8125 us
- GPE timestep: 0.9375 us (3 sub-small timesteps)
- # of modules per phase: *N* = 6 (18 H-bridges + 6 Transformers)/phase
- GPES box: 102 branches, and 47 nodes



Circuit in One Small-dt Box

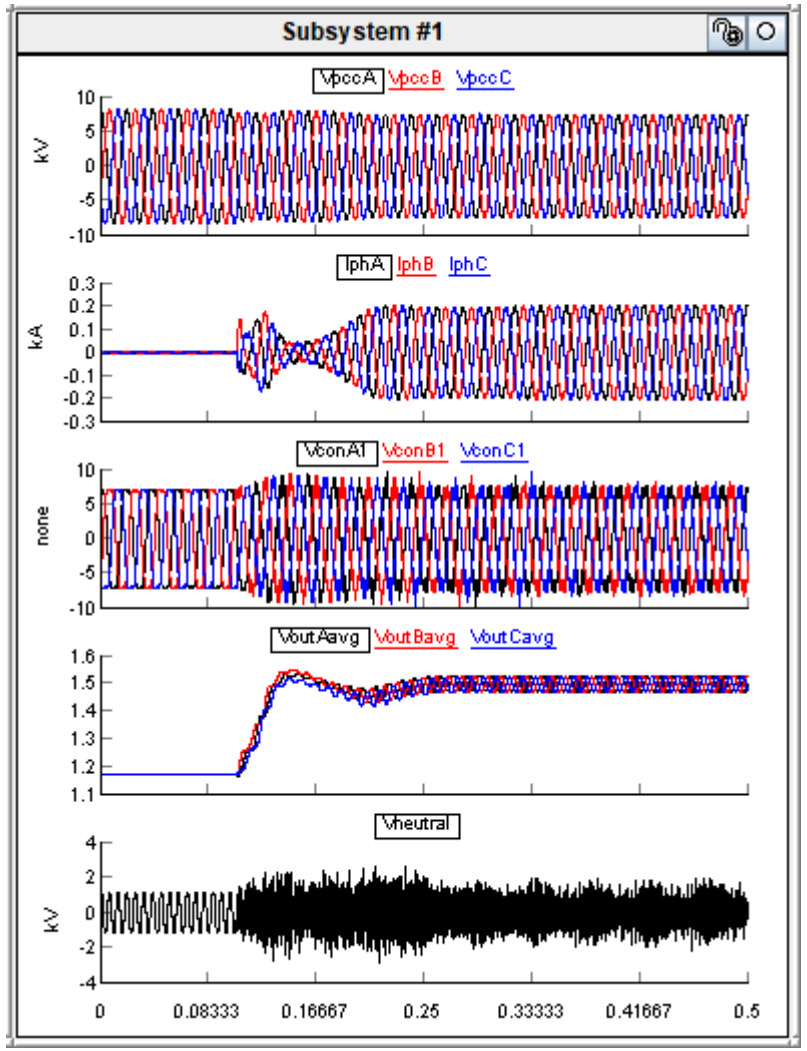


Phase A (AC-DC + DAB Converters)

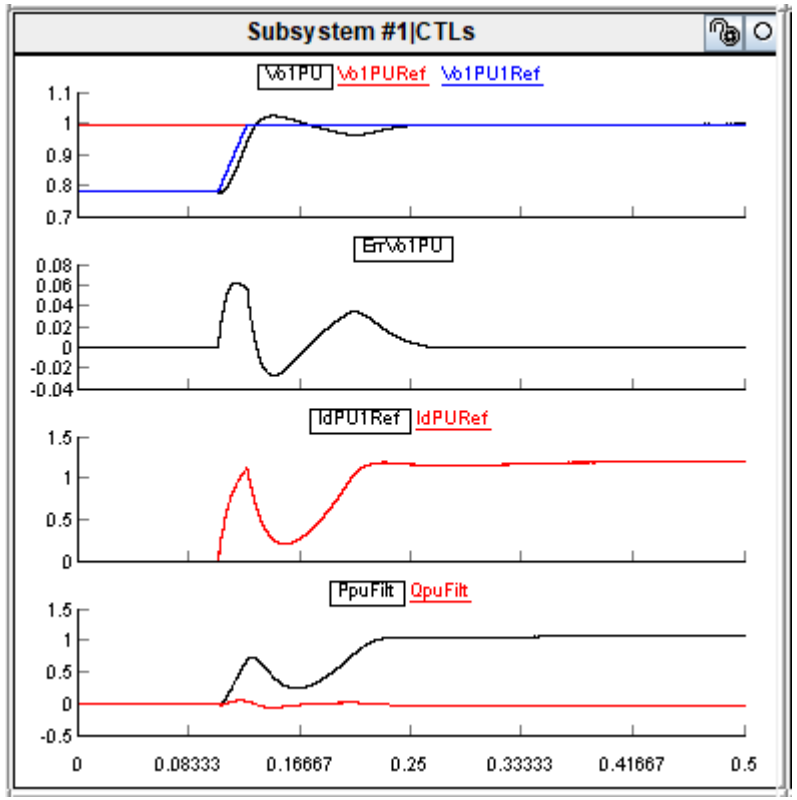


GPES Simulation Results

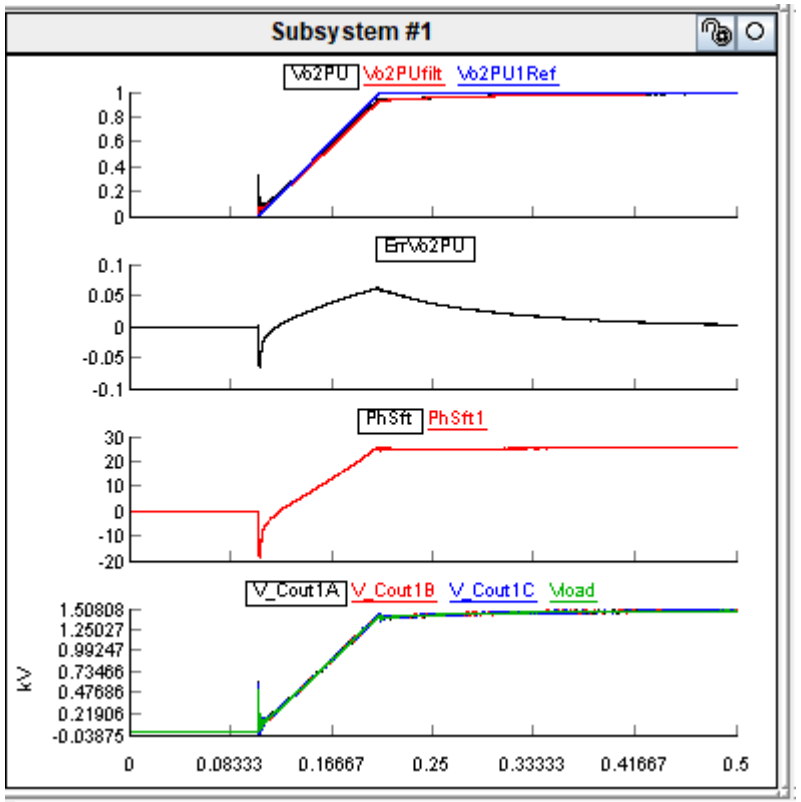
Blocking → Deblocking



AC-DC stage operating waveform



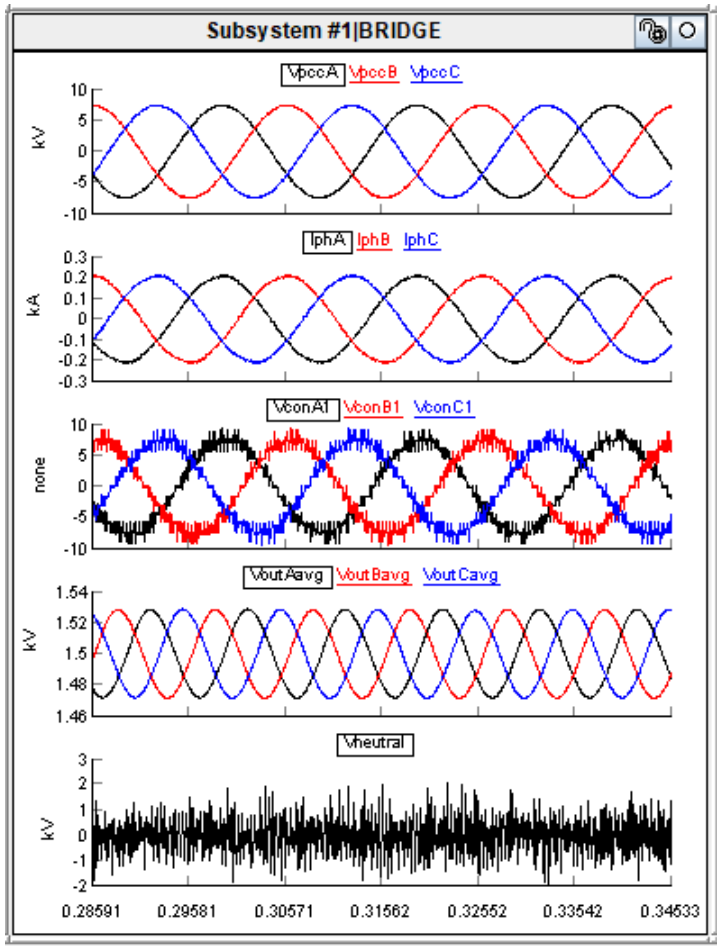
AC-DC stage Vcap control loop



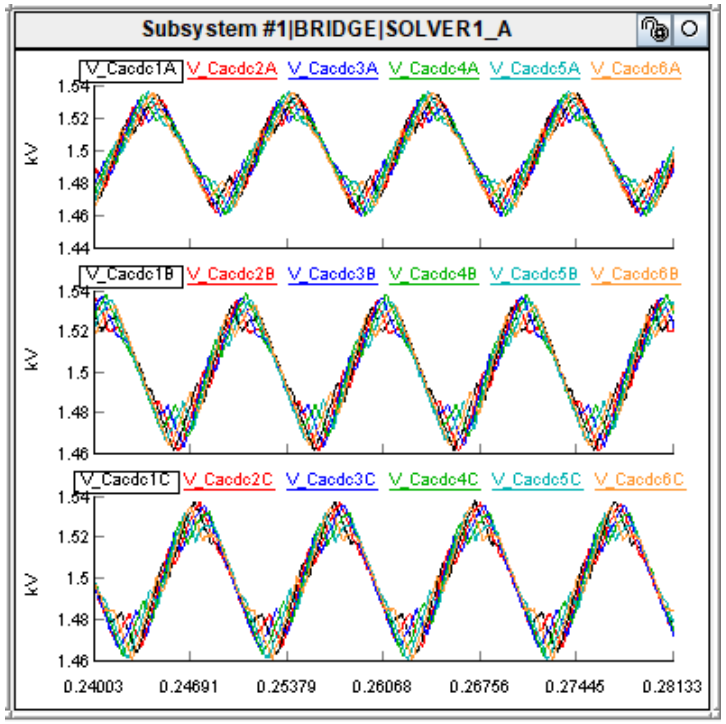
DAB output voltage control loop

GPES Simulation Results

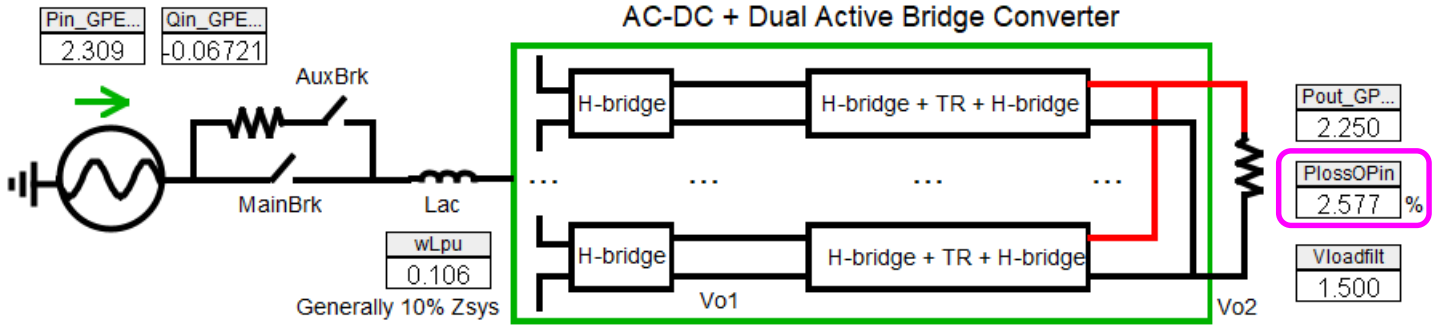
Steady-state operation: Vout = 1.0 pu → Po = 2.25 MW



AC-DC stage operating waveform

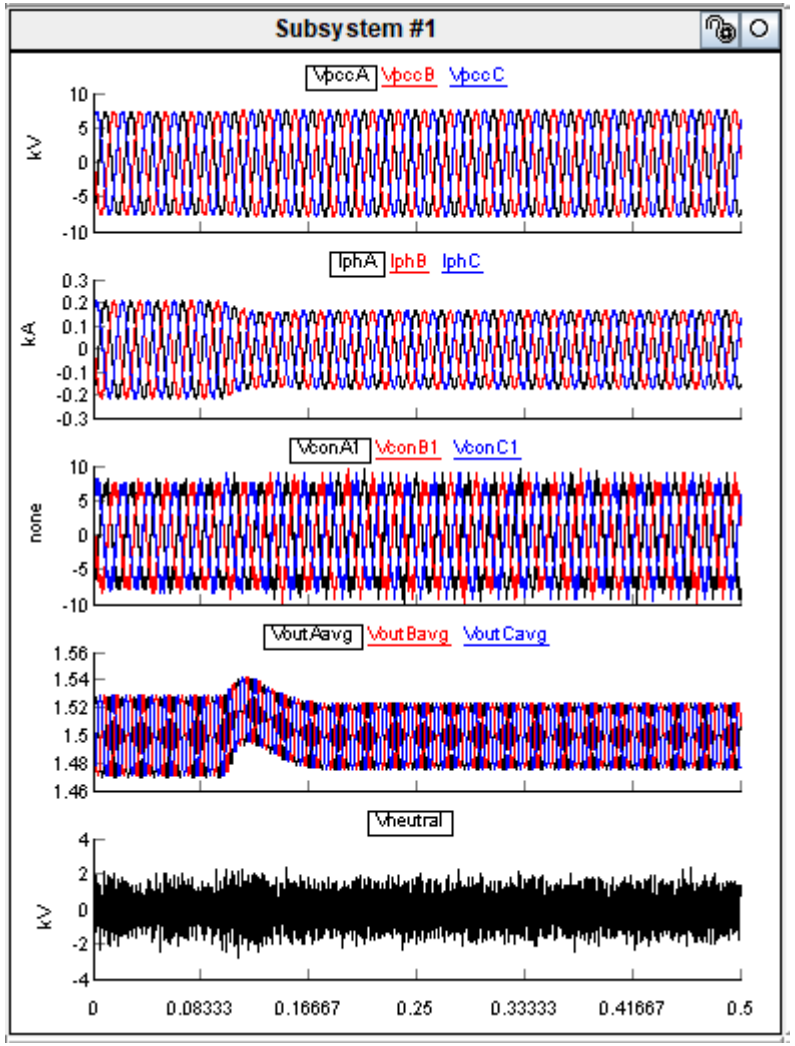


Cap voltages in AC-DC stage

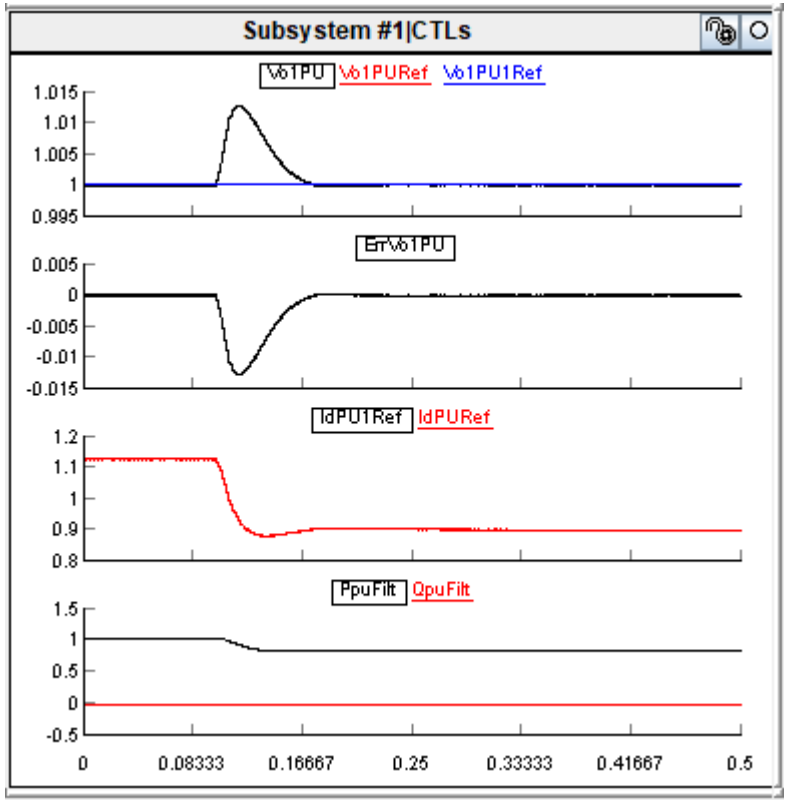


GPES Simulation Results

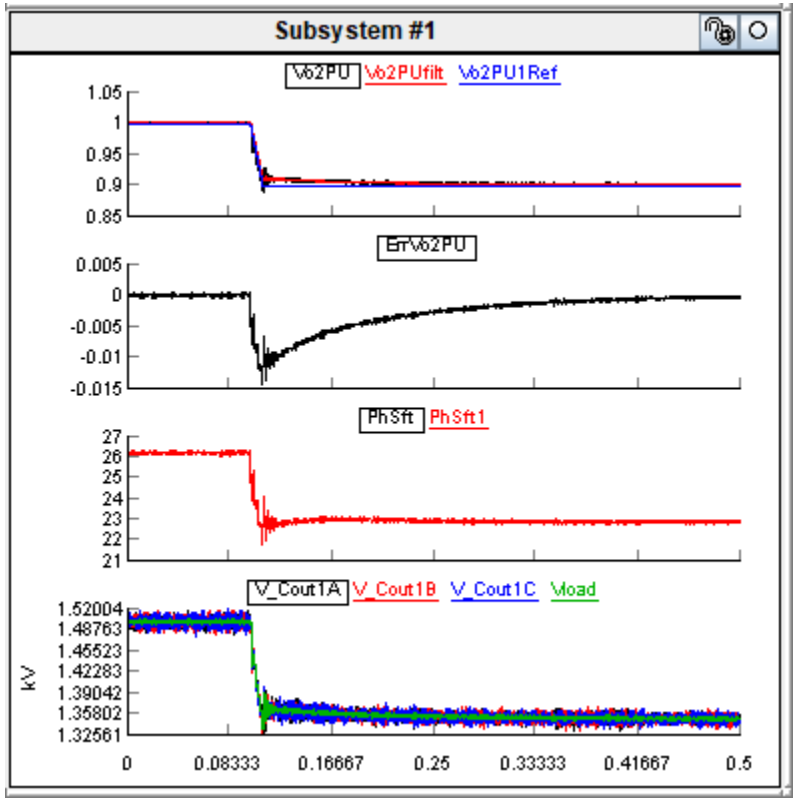
Dynamic operation: Vout = 1.0 pu → 0.9 pu



AC-DC stage operating waveform



AC-DC stage Vcap control loop



DAB output voltage control loop

Conclusions & Future Plan

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Conclusion

- **DC Transformer simulation**
  - Implemented in SUBSTEP and GPES
  - Operation with good performance
  - Easily modify to different numbers of modules
  - Per-unitization control and draft variables usage

Future Plan

- Release the developed control components to significantly simply the implementation of DC Transformer Simulation
- Release simulation examples of DC Transformer in SUBSTEP and GPES simulation environment


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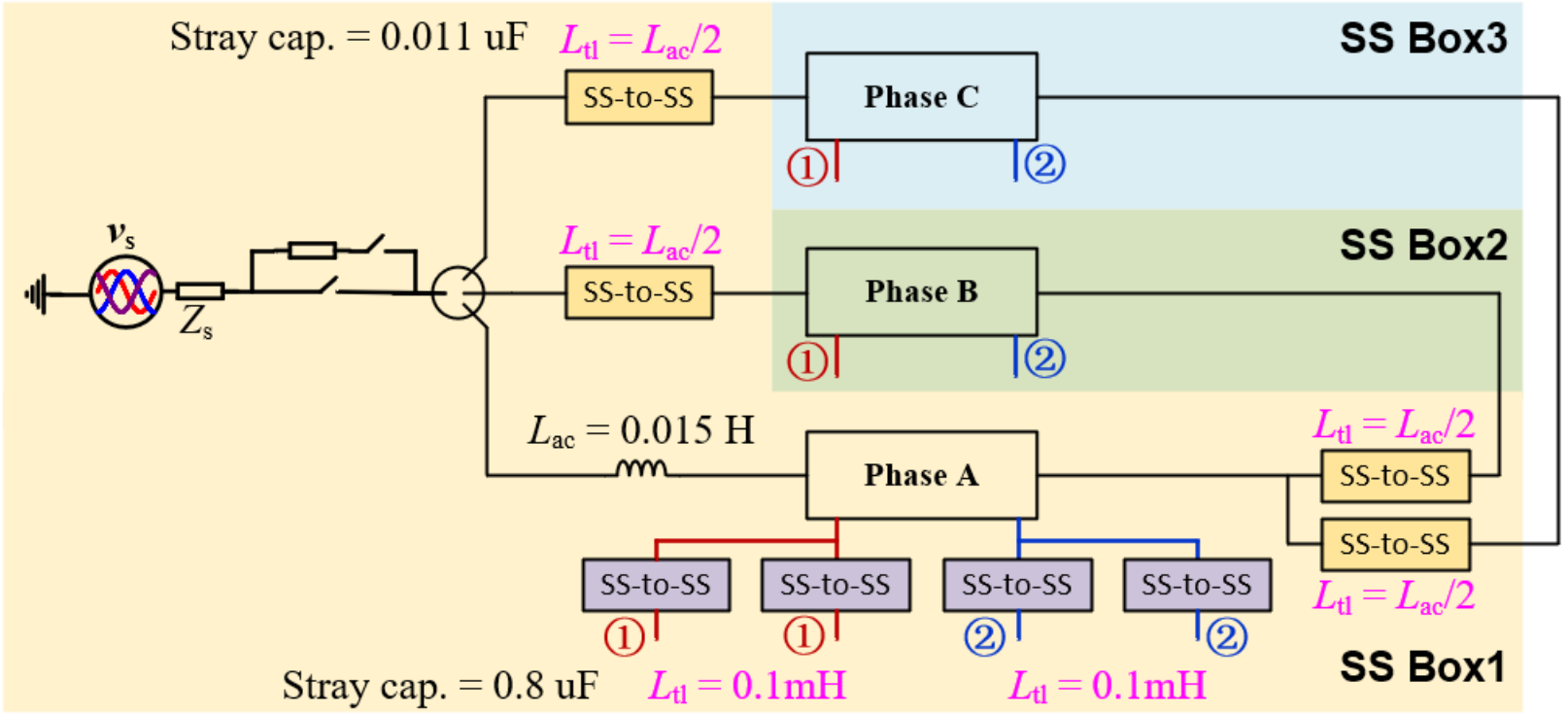
25 YEARS
RTDS.COM
THANK YOU!
QUESTIONS?

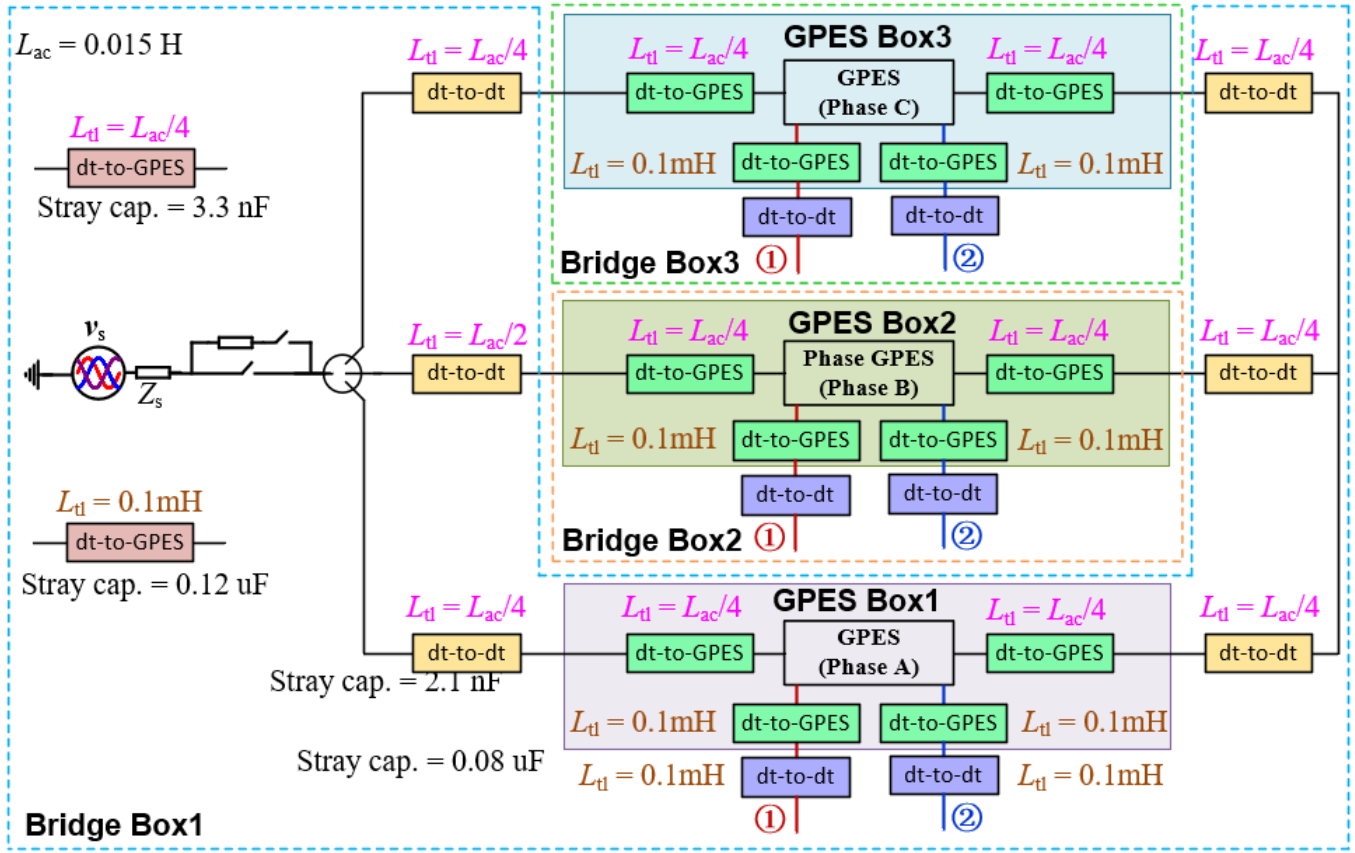
Simulation in SUBSTEP

Power circuit connection with interfaces



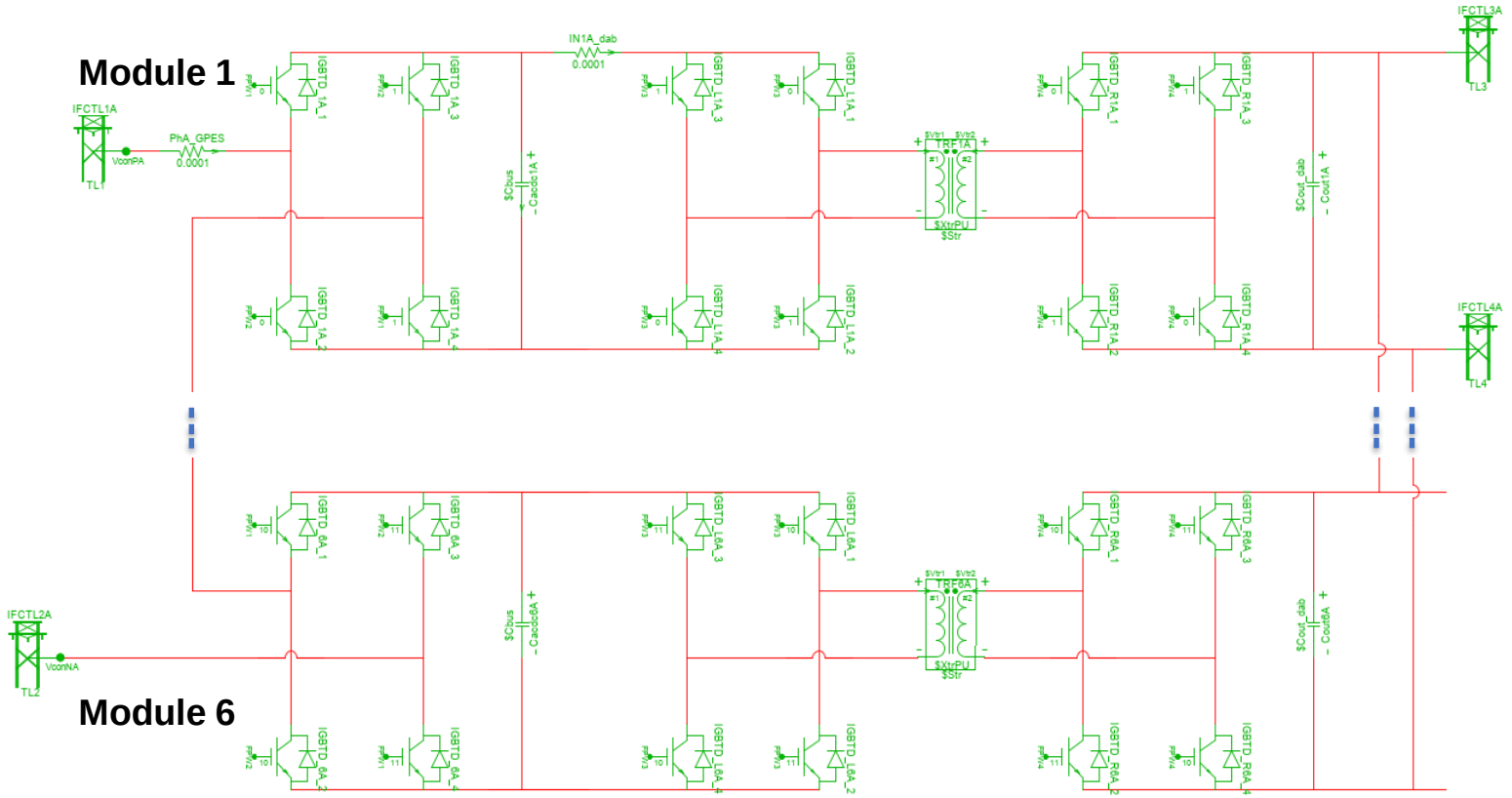
Simulation in GPES in Small-dt Box

Power circuit connection with interfaces



One Phase Circuit in GPES Box

Each module: 17 branches, and 8 nodes



Things to note:

- Transformer: base frequency equal to switching frequency
- Valve parameter for switches: vswit, iswit → (recommended to be equal to RMS/peak voltage and current in the valve)
- Interface: use the interface inductance as large as possible
- Simulation time step: as small as possible

GPES environment:

- LC switching → artificial losses

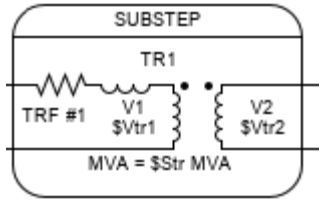
To reduce artificial losses:

(1) Use small time step

(2) Accurate vswit and iswit

(3) Low switching frequency

DAB Simulation Notes



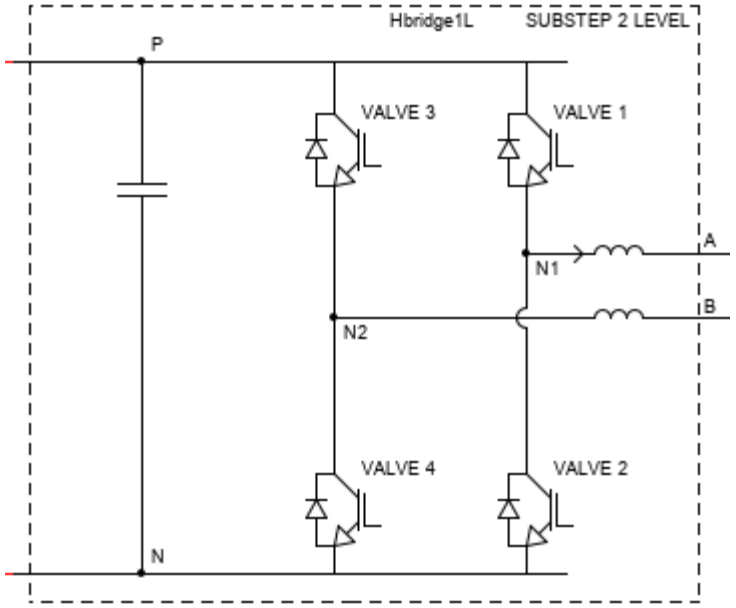
Transformer Base Frequency:
same as the switching frequency

rtds_ss_TRF S1PH.def

SIGNAL MONITORING IN RT AND CC | SIGNAL NAMES | CORE ASSIGNMENT
CONFIGURATION | SINGLE-PHASE TRANSFORMER PARAMETERS

Name	Description	Value	Unit	Min	Max
vw1t	Rated Winding 1 RMS Voltage:	$Vtr1	kV	0.001	
vw2t	Rated Winding 2 RMS Voltage:	$Vtr2	kV	0.001	
MVA	Rated 1-Phase Transformer MVA:	$Str	MVA	0.001	
frqt	Transformer Base Frequency:	$fsw2	Hz	0.01	
rput	Total Winding Resistances:	0.0	pu	0.0	
xput	Total Winding Reactances:	$XtrPU	pu	0.01	
mgls1	Winding 1 magnetizing losses:	0.00001	pu	0.00001	
mgls2	Winding 2 magnetizing losses:	0.00001	pu	0.00001	

Update | Cancel | Cancel All



rtds_ss_LEV2_V3.def

ENABLE MONITORING IN RUNTIME AND CC | SIGNAL NAMES | CORE ASSIGNMENT
VALVE PARAMETERS | DC CAPACITOR PARAMETERS
VALVE FIRING PULSES INPUT NAMES | AC REACTOR PARAMETERS
VSC 2-LEVEL EMBEDDED BRIDGE CONFIGURATION

Name	Description	Value	Unit	Min	Max
rvlon	Valve ON Resistance:	0.005	Ohms	0.0001	
rvlof	Valve OFF Resistance:	1.0e5	Ohms	1.0	
snbc	Snubber Series Capacitance:	$Csnb1	MicroF	0.001	
snbr	Snubber Series Resistance:	$Rsnb1	Ohms	1.0	

VALVE PARAMETERS:

- rvlon, rvlof: used to simulate system losses
- snbc, snbr: used to suppress numerical oscillations → should be properly selected
- **Recommendatoins: snbc*snbr = 2*SubtimeStep, and snbr = 500 Ω to 2000 Ω**

DAB Simulation Notes

Substep to Substep Interface:

- Introduce 1 sub-timestep delay
- Stray capacitance: C = sub-timestep^2/Ltl
- Ltl: Interface inductance

Recommendations:

- Dividing large system through the branch with large inductance
- Put the interface inductance as large as possible
- Use simulation time step as small as possible