#### Your world in real time.



# NEW FPGADEVELOPMENT



### AGENDA

- MMC Development
- GPES Development
- Interfacing Development









#### **MMC Model Success**

- Successfully involved in major HVDC projects all around the world, especially in China
- Model being improved and enhanced to satisfy different requirement from the real projects
- Being the first time, GMMX model is now used in the Kun-Liu-Long Project of CSG.



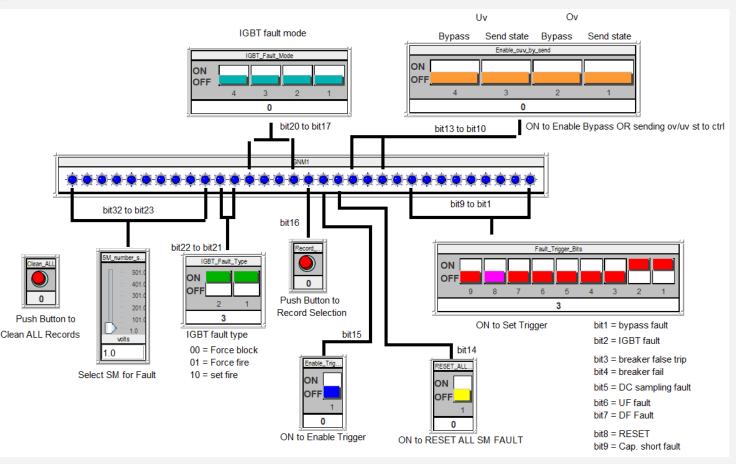
#### **New Features of GMMX Model**

- New faults: Bypass breaker fail and false trip fault, communication fault, DC sampling fault, etc.
- Trigger fault more flexibly
- Measuring IGBT switching frequency
- Monitoring all SM cap. Voltages, Firing Pulse Words, and SM state on User
   PC via UDP Ethernet
- HB and FB SM any location
- Support new Valve-to-Control protocol proposed by CSG



#### **Faults and Triggering**

- Multiple faults on the same SM
- Trigger faults one SM after the other
- Trigger faults simultaneously for many SMs
- No need to re-compile the case





#### **Monitoring MMC via Ethernet**

• A Ethernet cable connected between PC and GTFPGA MMC unit

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 SM voltage, firing pulse word, and state monitored

 Impas
 Leg No. 1: Max No. Pass-Thru Signals, RTDS to Controls:

 Impa...
 Leg No. 2: Max No. Pass-Thru Signals, RTDS to Controls:

 aneth
 Enable monitoring MMC through Ethernet (UDP):

Update

Cancel

Cancel All

ort PB5/NovaCor GTIO Fiber Port Number

コロレ								No. of SM	·	Firing Pulse/Capacitor Voltage (kV) (fibre 1)									
						Port Number		·	001	033	065	097		129	161	193	225		
							Port Nulliber	Leg kA		002	034	066	098		130	162	194	226	
							Charles 1	LegkV		003	035	067	099		131	163	195	227	
• .							Start	Legkv		004	036	068	100		132	164	196	228	
Init							Stop	Valve kV		005	037	069	101		133	165	197	229	
1111								SM Max k		006	038	070	102		134	166	198	230 231	
								SM Max K		007	040	072	103		135	167	200	231	
		CONFIGURATION	OF ETHERNE	T				SM Min k\	,	009	041	073	105		137	169	201	233	
	CONFIGURATION OF VALVE TO CONTROLLER COMMUNICATION									010	042	074	106		138	170	202	234	
	SUB MODULE VALVE PARAMETERS ( 1 SM only )						LEG 1	SM Ave. k	v	011	043	075	107		139	171	203	235	
	GENERAL MMC BRIDGE PARAMETERS						LEG 2			012	044	076	108		140	172	204	236	
	CONFIGURATION OF FPGA GENERIC MMC MODEL									013	045	077	110		141	173	205	237 238	
							RESET			015	047	079	111		143	175	207	239	
	Name	Description	Value	Unit	Min	Max				016	048	080	112		144	176	208	240	
	sport	Local UDP Port number	Value 55257	Unit	1024	65535				017	049	081	113		145	177	209	241	
	sport sip1	Local UDP IP Address 1	169		0					018	050	082	114		146	178	210	242	
					0	255				019	051	083	115		147	179	211	243	
	sip2	Local UDP IP Address 2	254		~	255				020	052	085	117		148	180	212 213	244	
	sip3	Local UDP IP Address 3	226		0	255				022	054	086	118		150	181	213	245	
2	sip4	Local UDP IP Address 4	178		0	255				023	055	087	119		151	183	215	246	
e	dport	Remote UDP Port number	15000		1024	65535				024	056	088	120		152	184	216	248	
	dip1	Remote UDP IP Address 1	172		0	254				025	057	089	121		153	185	217	249	
	dip2	Remote UDP IP Address 2	24		0	255				026	058	090	122		154	186	218	250	
	dip3	Remote UDP IP Address 3	2		0	255				027	060	092	123		155	187	219 220	251	
	dip4	Remote UDP IP Address 4	181		0	255				029	061	093	125		157	188	220	252 253	
	note	IP address is separated into 4 numbers.								030	062	094	126		158	190	222	253	
	note1	For ip 169.254.226.178,					UNDTOC			031	063	095	127		159	191	223	255	
	note2	dip1 is 169						2		032	064	096	128		160	192	224	256	
	note3	dip2 is 254					Technologies	·											
	note4	dip3 is 226																	
	note5	dip4-ia-478							$\boldsymbol{h}$										
		Update Cance	Cancel	All															
																	-		
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MMC Leg 1

**RTDS MMC Monitor** 

Fibre 1 Fibre 2 Fibre 3



#### **MMC Models in Substep**

- ✓ U5 model and controller
- ✓ GMMX model and controller
- ✓ GMMX 6vlv model and controller
- ✓ GMT3 model (controller same as for GMMX)
- ✓ GMSD (serial double submodule) model (controller same as for GMMX)
- ✓ Upgraded MMC5 model supporting HB/FB mixed

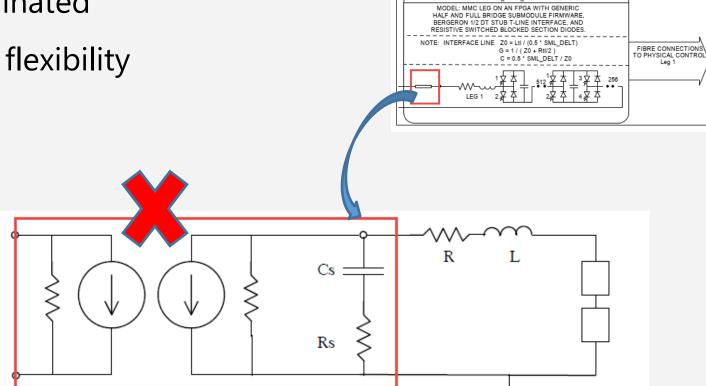


#### **New Development Next Step**

• Like many other components in substep

interface t-line eliminated

• More accuracy and flexibility



VSC MODEL TYPE: MMC\_EPGA\_GMMX\_EPGA135

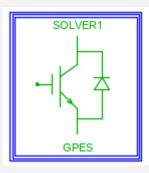


### GPES Development



#### **GPES Simulation Platform**

- A Generic Power Electronics Solver (GPES) on GTFPGA
- Uses powerful parallel processing power of FPGA
- Can model power circuits with arbitrary circuit configurations
- Larger network (128 nodes and 256 branches) and smaller time step (400<sup>+</sup> ns), e.g., the dc breaker needs 110+ nodes and 200+ switches

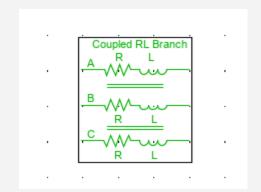


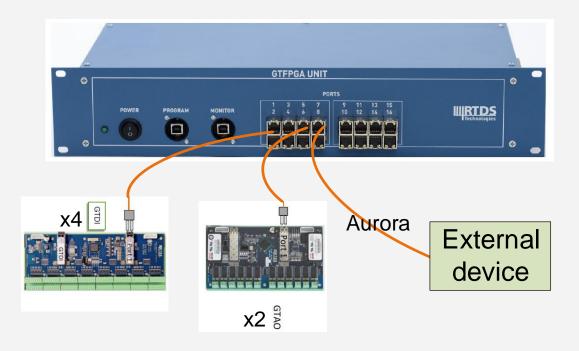




#### **New Components**

- Three-phase coupled RL component added
- 4 GTDI cards connected to Port 1-4 for firing 256 switches
- 2 GTAO cards connected to Port 5-6 for analogue output

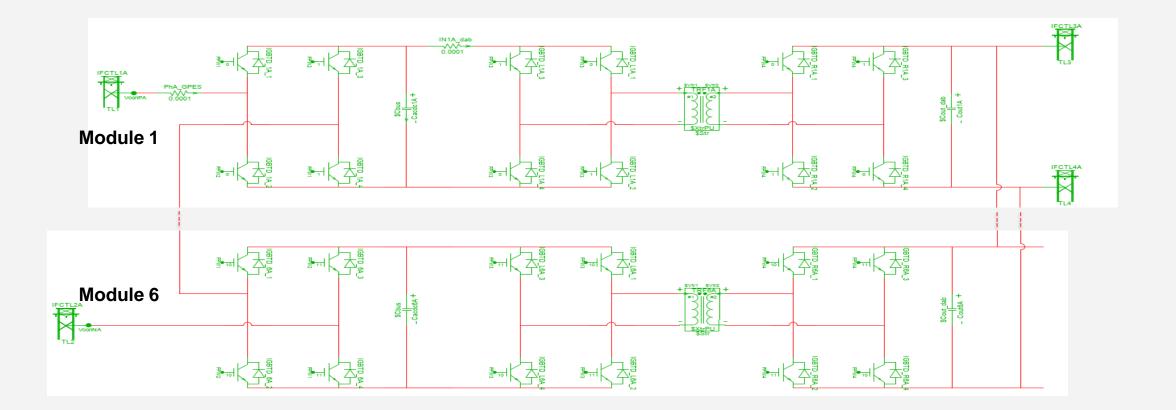






#### **GPES Example: DC-DC Transformer**

• Up to 15 modules modelled in one GPES unit



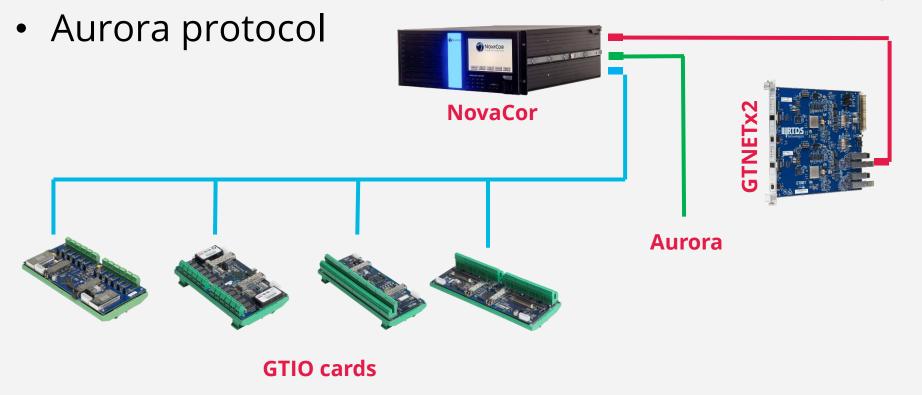


### Interfacing Development



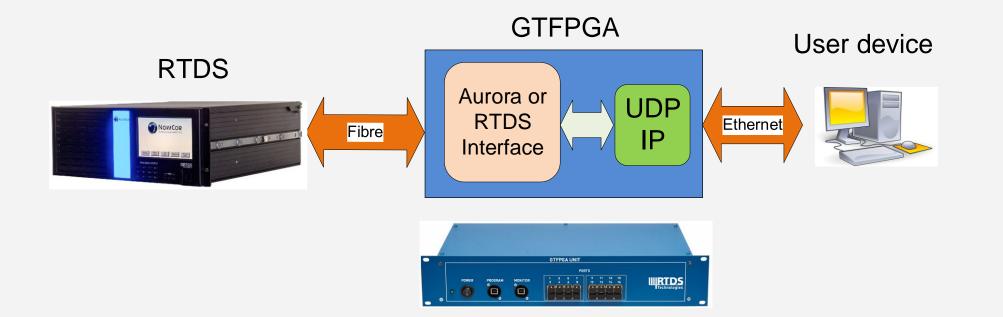
#### **Interfacing to RTDS**

- Convectional way: GTIO cards
- Network communication: GTNET cards, various protocols



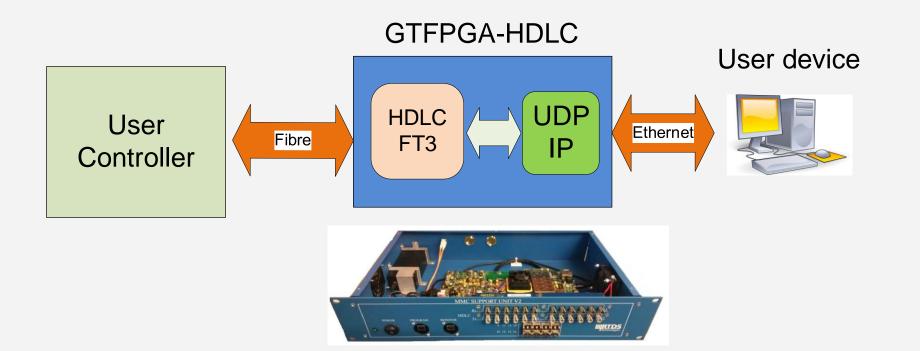


• User device interface to RTDS through Ethernet (UDP)



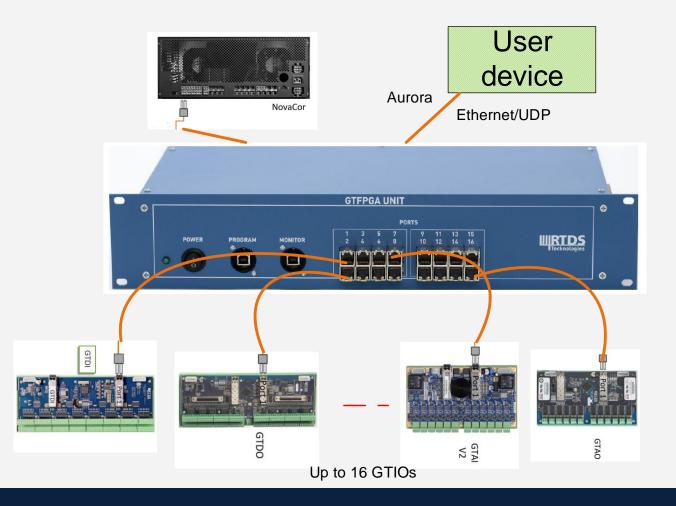


• User device (UDP) interfacing to controller (FT3)



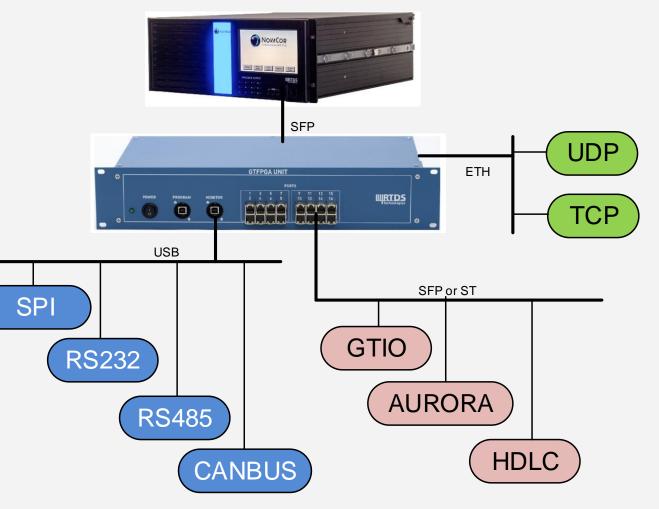


• GTIO cards connected to RTDS or User Devices





- More general
- Include many interfacing methods in a single GTFPGA





Any comment, new requests are welcome.

## We are here to listen.





