SUPERSTEP SIMULATION



RTDS.COM

Outlines

- 1. Multirate Simulation
- 2. Superstep Introduction
 - What
 - Why
 - How
- 3. Examples
- 4. Summary





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Multirate Simulation Remote Remote System System Area of Interest Power Electronics Remote System Technologies 3/18 *Introducing NovaCor*[™] – *the new world standard for real time digital power system simulation*

Multirate Simulation



IIIRTDS

Technologies

Superstep

Remote

System

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Mainstep

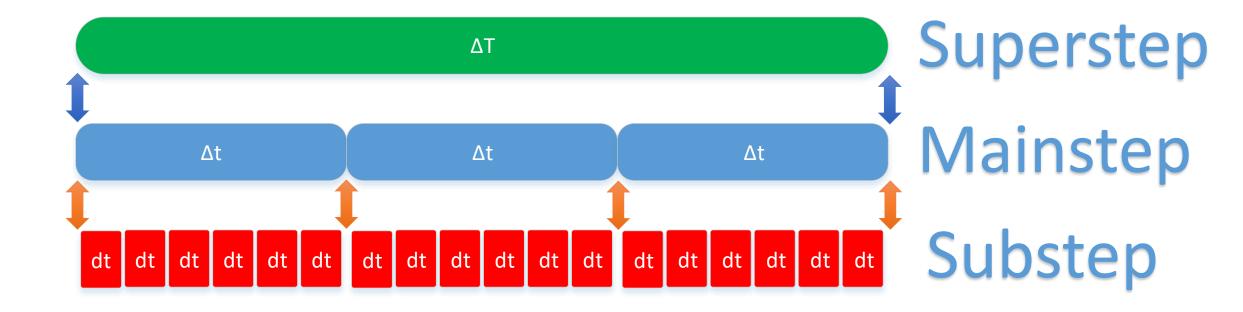
Area of Interest

Power Electronics Substep Remote System

Superstep



Multirate Simulation





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- While doing simulation, things must be considered:
 - 1. The nature of the study
 - 2. Hardware availability
 - 3. Data reliability
- Traditionally an ideal source with an impedance has been used to model a system equivalent.
- Such equivalent may not provide accurate results for all contingencies.



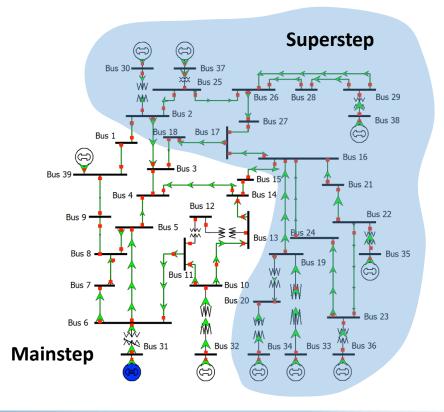


What is a Superstep?

• Superstep is an alternative approach to using a system equivalent to

model a large remote network.

- Advantages for User:
 - 1) Allows the detail of EMT simulations to be retained.
 - 2) A remote network's control elements can be modeled.
 - Generator dynamics can be modeled so frequency deviations due to the load/generation imbalance can be observed.







What is a Superstep?

- A *superstep network* is defined as a collection of components placed inside a hierarchy box and solved using the superstep.
- Use of the larger time-step and a simplified network solution significantly increases the modeling capabilities of the RTDS Simulator.
- A tradeoff between capability and accuracy when using superstep feature due to the use of a larger time-step compared to the main time-step.





- Only be used in NovaCor platform.
- Network Solution, Power System Components and Controls are all simulated on a single core.







• Timestep for *superstep* simulation is either **2x**, **3x**, **4x** or **5x** the main timestep.

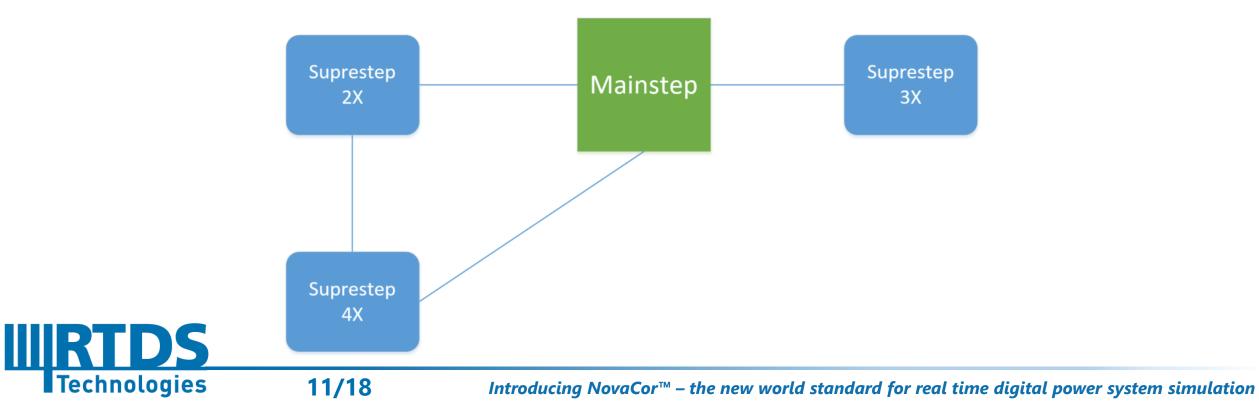
HIERARCHY						
Box Parameters	Superstep Options					
Name	Description	Value	Unit	Min	Max	
SuperstepBoxType	Superstep box type	POWER SYS 🔻		0	1	
SuperstepMultiplier	Contents will be run once every N	.2		2	5	
Update Cancel Cancel All						



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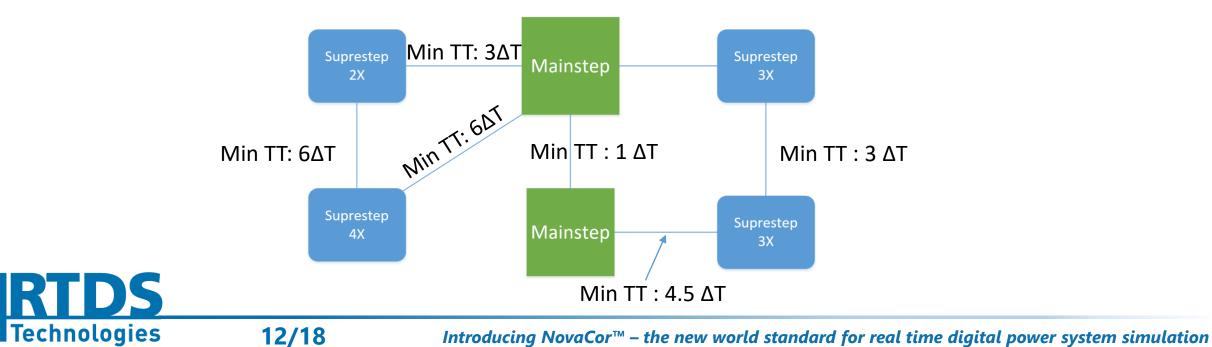


- Multiple *superstep* hierarchy boxes can be run on different cores of a chassis and can be
 - interconnected using *multi-rate transmission lines*.





- The two terminals can be run using independent timesteps that are integer multiples of each other or the main timestep.
- The minimum signal travel time must be 1.5*(larger of terminal timesteps) when terminals operate at different rates. It must be 1.0*terminal timestep when the terminals operate at the same rate.



Limits/Restrictions

- Available for NovaCor[™] Only
- Runs on one full core.
- Superstep = main timestep * n.
- Max timestep = 150us.

Technologies

- Max nodes = int(superstep timestep)*2.
- Max load units = (superstep timestep)*24

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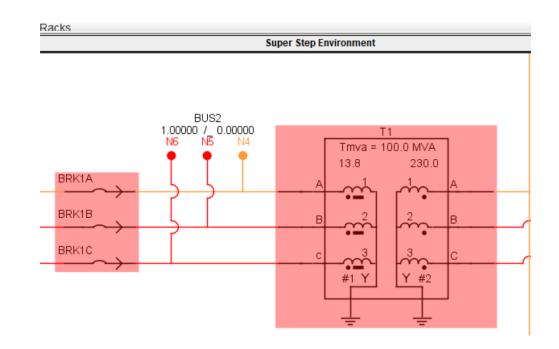
• Breakpoint Mode not supported

- At least one core on the chassis must be running at the main timestep
- *Restricted Components*:
 - No components with variable G or switched G values
 - No Faults or Breakers
 - No IO components
 - No small timestep components
 - Non-linearity such as transformer saturation





• When unsupported components are placed within a *superstep hierarchy box* their icons turn red in DRAFT. This gives the user a visual indication of the incompatibility.



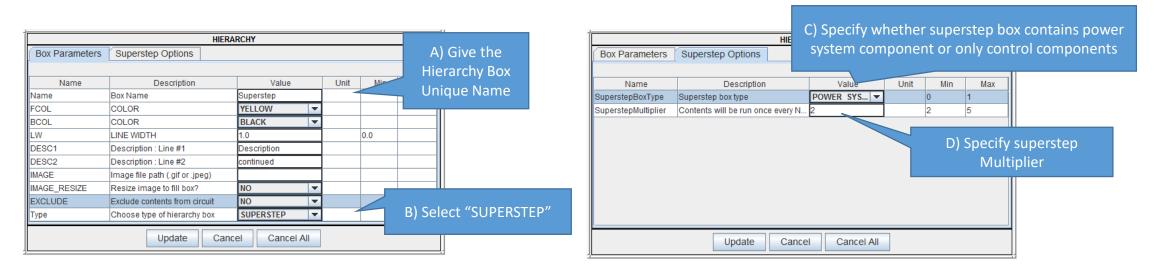


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Making a Superstep Case

- 1) Build the circuit to be simulated with a superstep inside a hierarchy box.
- 2) Change the following properties the hierarchy box:



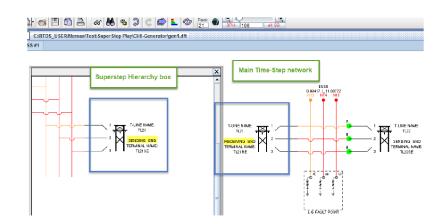
3) Place at least one component in the main timestep.

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4) Optionally use T-line or Cable to connect a *superstep hierarchy box* to other boxes **or** to the main timestep network



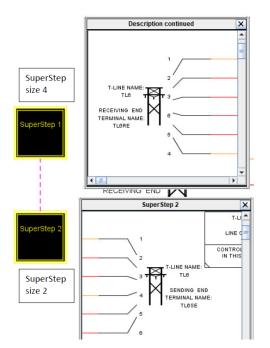
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Connecting Superstep Hierarchy to main timestep network

5) Compile and Run the case as usual.

Technologies

Connecting Two Supertep Hierarchy Boxes



EXAMPLE 1 Illinois 200-Bus System

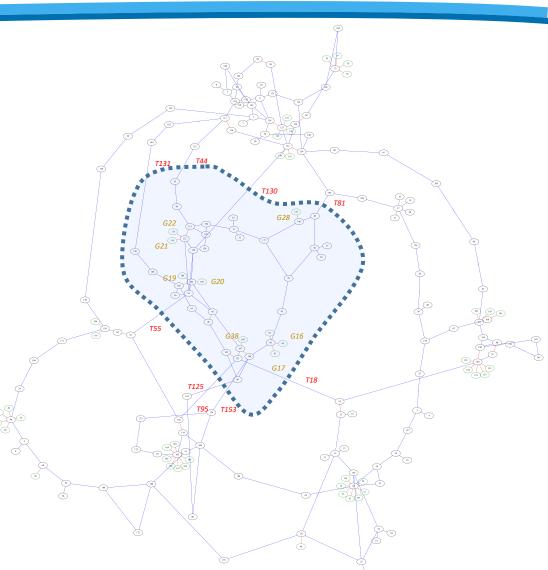




• Synthetic Test System that is built from public information and a statistical analysis of real power systems. It is not representative of the actual grid in Illinois but should be realistic.

https://electricgrids.engr.tamu.edu/electric-grid-test-cases/activsg200/

- Used PSSE-to-RSCAD Conversion Program to import into RSCAD
- This test case was used to evaluate performance in order to determine the accuracy of using a super-step.
- 486 Single Phase Nodes, ~2600 Load Units

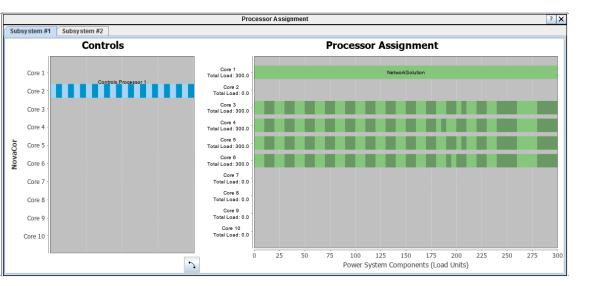




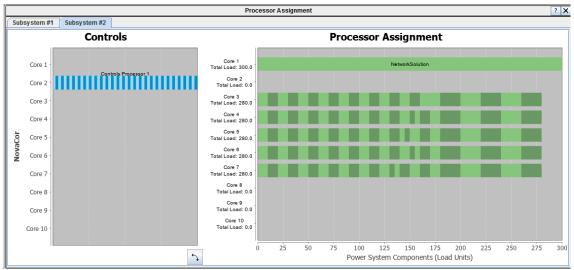


Processor Allocation

Conventional Single-Rate Simulation











IIIRT

Illinois 200-Bus System

Processor Allocation

Conventional Single-Rate Simulation (1 rack, 50 us)

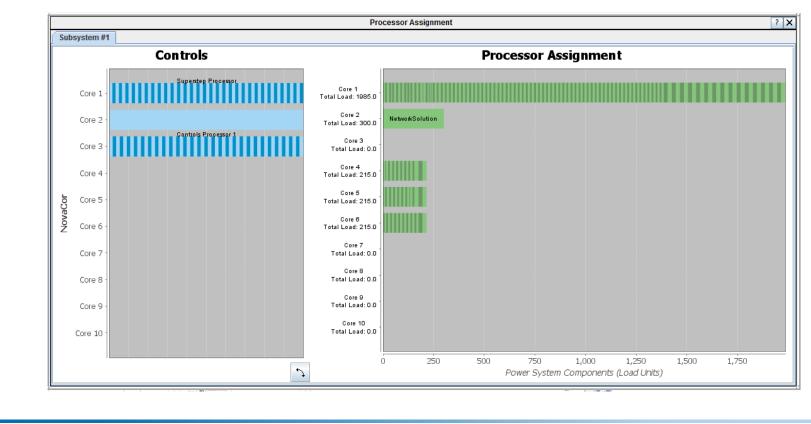
DRAFT 5.010_a File Sequencer Racks		EN 📾 😧 📜
COMMENTS C:\RTD S_U SER\fileman\Project\S	iperstep\superstep_Greg\Yue\llinois200.dft	
Subsystem #1		
CALCULATION BLOCK	CALCULATION BLOCK	CALCULATION BLOCK CALCULATION BLOCK CALCULATION BLOCK
NETWORK		T-LINE NAME;
AUTOMATIC LINE CONSTANTS: PLACEMENT CONTROL AND MONITO	Tompile Error	TANTS: LINE CONSTANTS: LINE CO
CONTROL AND MONITO	✓ Info (0) ✓ Warnings (2) ✓ Errors (3)	MONITOR CONTROL AND MONITOR CONTROL AND MONITOR SYSTEM . IN THIS SUBSYSTEM . IN THIS SUBSYSTEM IN TH
Network Solution 1 <- SS -> 1	Plages shock your merbins a svis data	$ \rightarrow 1 \qquad 1 \leftarrow 5S \rightarrow 1 \qquad 1 \leftarrow SS \rightarrow 1 \qquad 1$
2 Cores Auto Processor Assignme	Please check your machine q-axis data. (machine name: 189x1)	Assignment Auto Processor Assignment Auto Processor Assignment Auto Pro
	in subsystem: 1	
		67x1
ESAC4A parameters IEEE Type ESAC4A configured for SEX\$ Excitation	ERROR - Number of nodes (249) assigned to core 1, in subsystem 1 exceeds the processor limit of 90 nodes.	ESAC4A parameters IEEE Type ESAC4A configured for SEX\$ Excitation
System	(Node limit of 90 has been set because auxiliary components have been stacked with the network solution.)	System
	ERROR - Number of nodes (237) assigned to core 2, in subsystem 1 exceeds the processor limit of 90 nodes.	
	(Node limit of 90 has been set because auxiliary components have been stacked with the network solution.)	
49x1	ERROR - It appears that power system components have been stacked with the network solution on 2 cores. This is only 1	
	allowed on one core.	
	ОК	
nologies		tandard for real time digital power system



Processor Allocation

Mixed/Hybrid Simulation

(1 chassis, mainstep 50 us + superstep 150us)



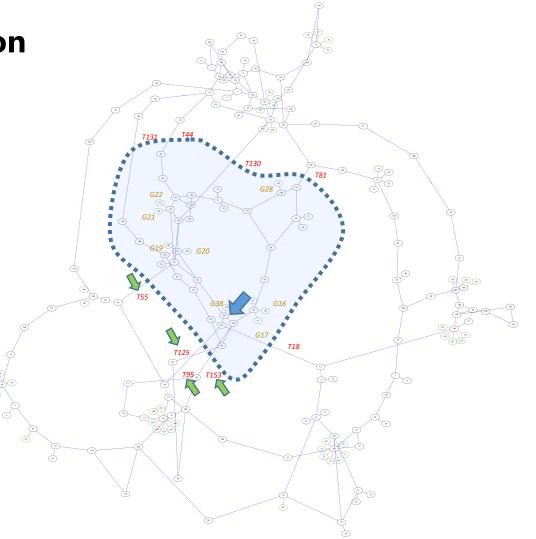




Accuracy Evaluation

Several time domain response for a conventional single-rate simulation were compared to the responses for a multi-rate simulation where the shaded portion of the network was modeled using the main time-step and the rest was modelled using a 3x super-step.

Generally P, Q and ω of all machines modeled in main time-step was monitored. Bus voltages near those machines were also monitored. The P and Q of the lines spanning the regular time-step and the super-step was also monitored.

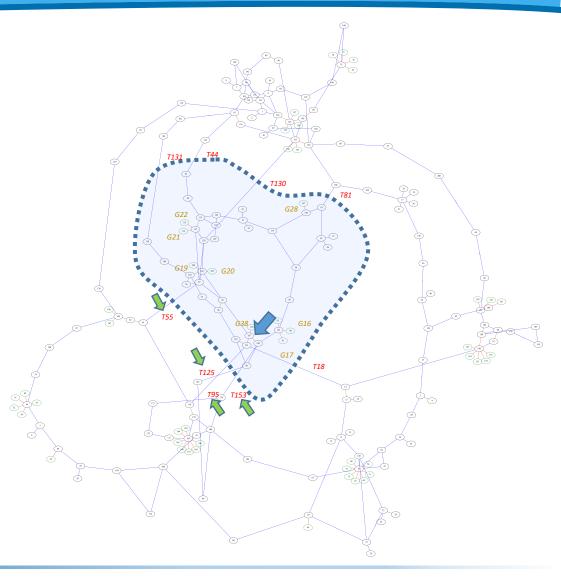






3 Scenarios to Evaluate Accuracy

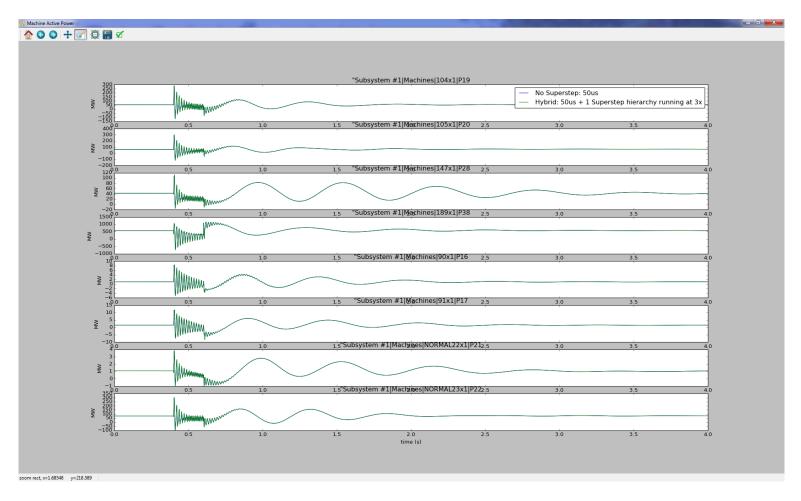
- Test 1: 200 ms AB–G fault was applied at Bus # 187
- Test 2:Four (4) multi-rate lines were successively tripped 100ms apart.
(T55, T125, T95 and then T153) All 4 lines suffered 3 phase trips.
- **Test 3:** A 200 ms ABC-G fault was applied at Bus # 187. The generator at that bus was tripped 150 ms after the application of the faults.







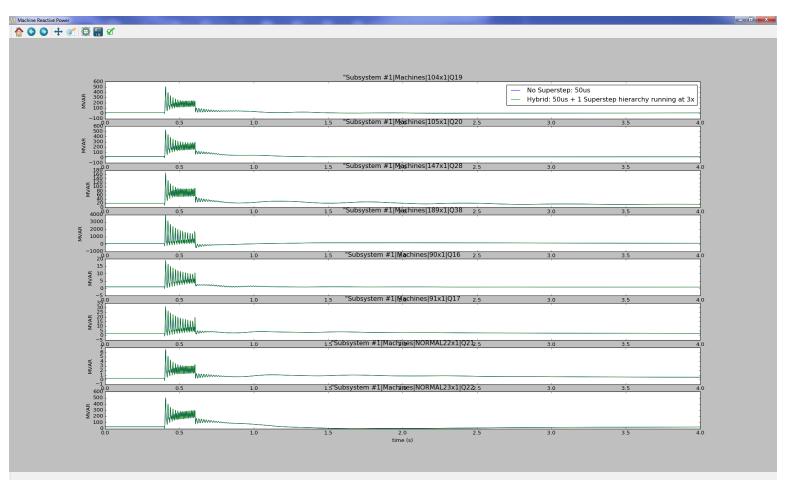
Test 1: 200 ms AB–G fault was applied at Bus # 187 (Machine Active Power)







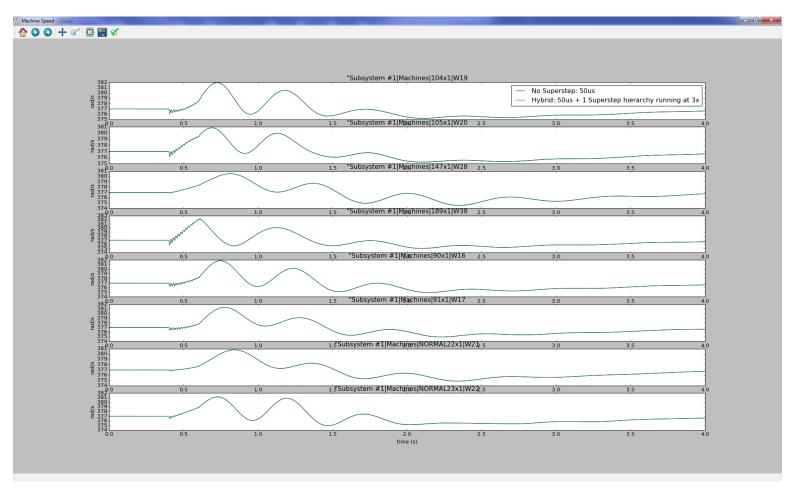
Test 1: 200 ms AB–G fault was applied at Bus # 187 (Machine Reactive Power)







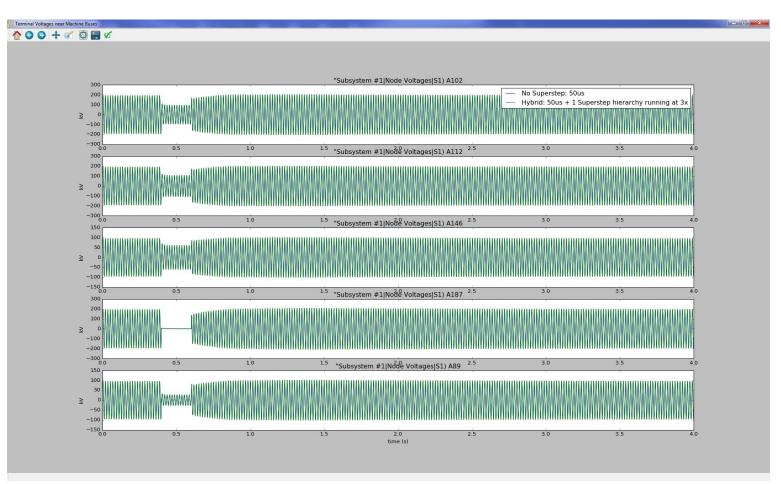
Test 1: 200 ms AB–G fault was applied at Bus # 187 (Machine Speed)







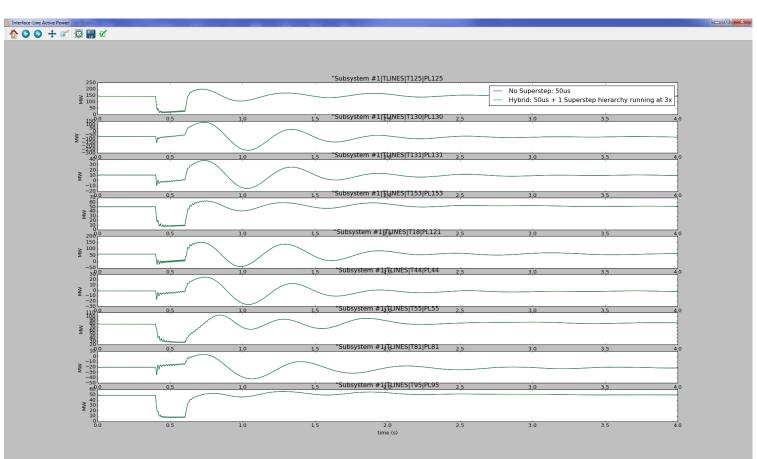
Test 1: 200 ms AB–G fault was applied at Bus # 187 (Terminal Voltages near Machine Buses)







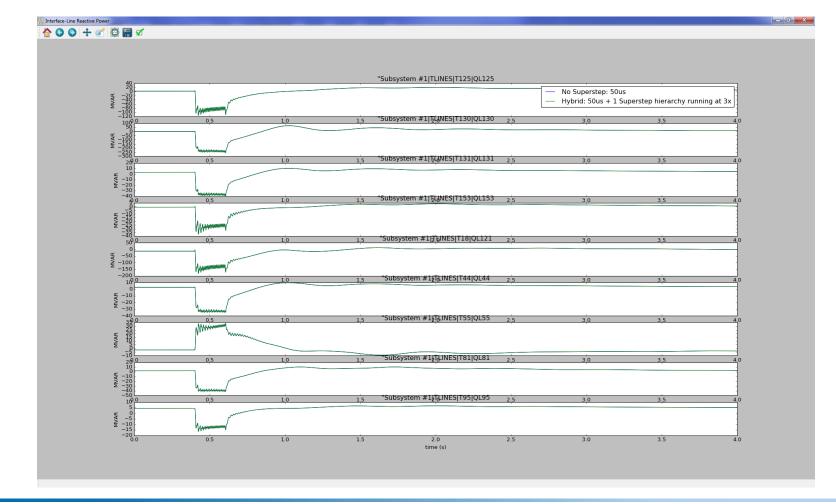
Test 1: 200 ms AB–G fault was applied at Bus # 187 (Interface-Line Active Power)







Test 1: 200 ms AB–G fault was applied at Bus # 187 (Interface-Line Reactive Power)

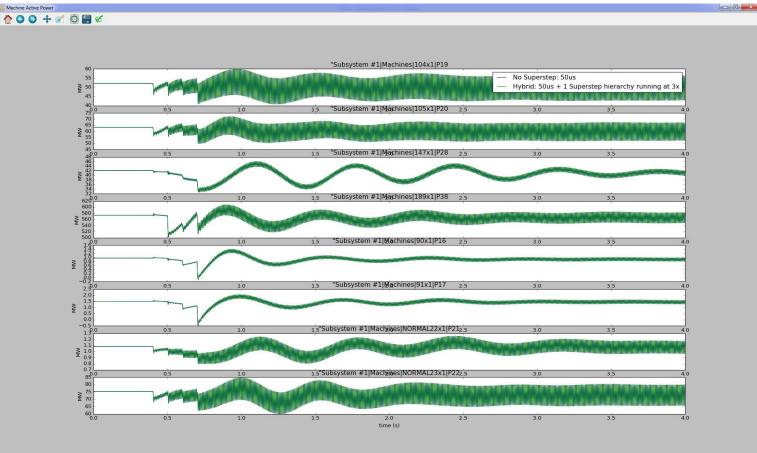






Test 2: Successive trip of four interface lines (100ms intervals)

Machine active power

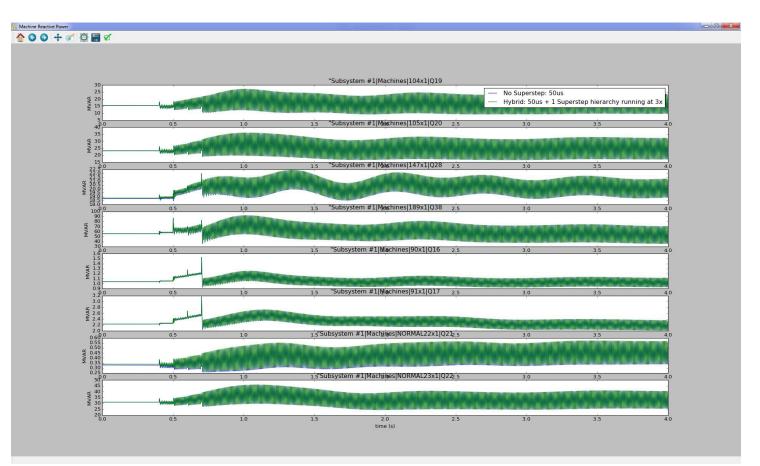






Test 2: Successive trip of four interface lines (100ms intervals)

Machine reactive power

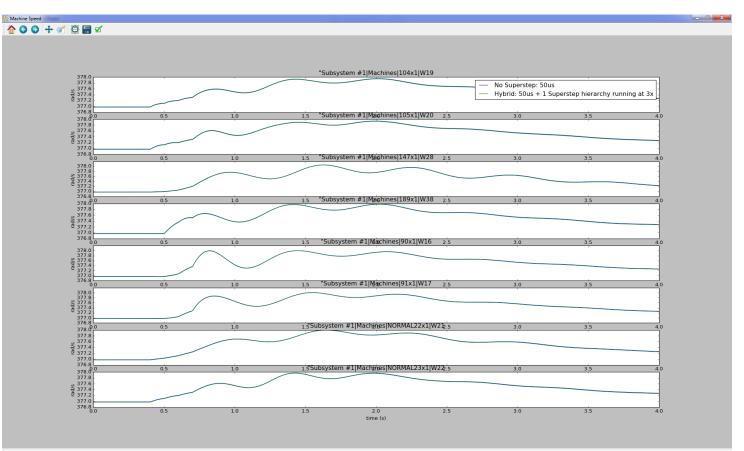






Test 2: Successive trip of four interface lines (100ms intervals)

Machine Speed

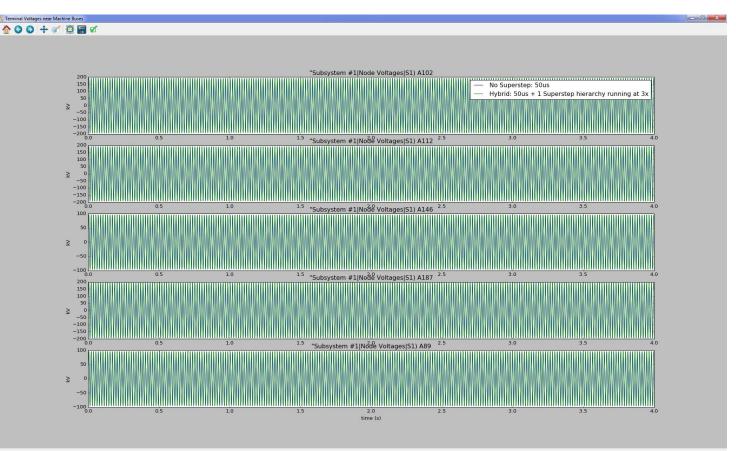






Test 2: Successive trip of four interface lines (100ms intervals)

Terminal voltages near machine buses

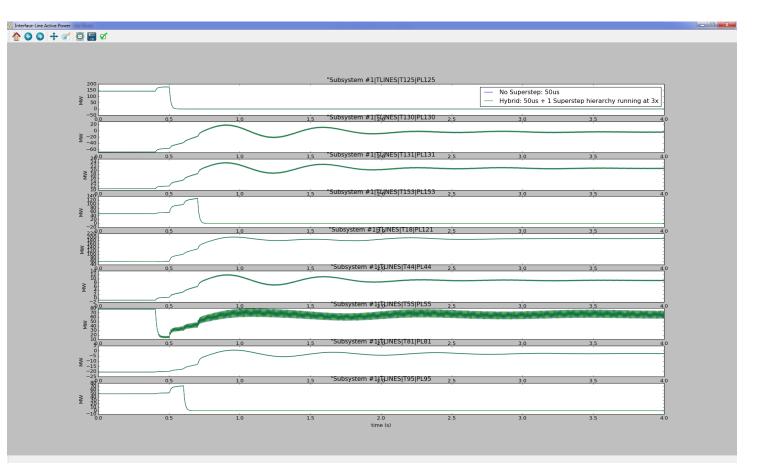






Test 2: Successive trip of four interface lines (100ms intervals)

Interface-line active power

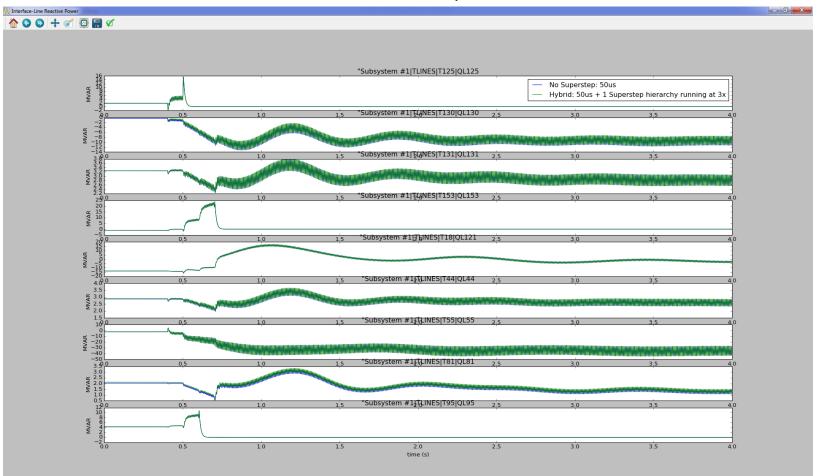






Test 2: Successive trip of four interface lines (100ms intervals)

Interface-line reactive power



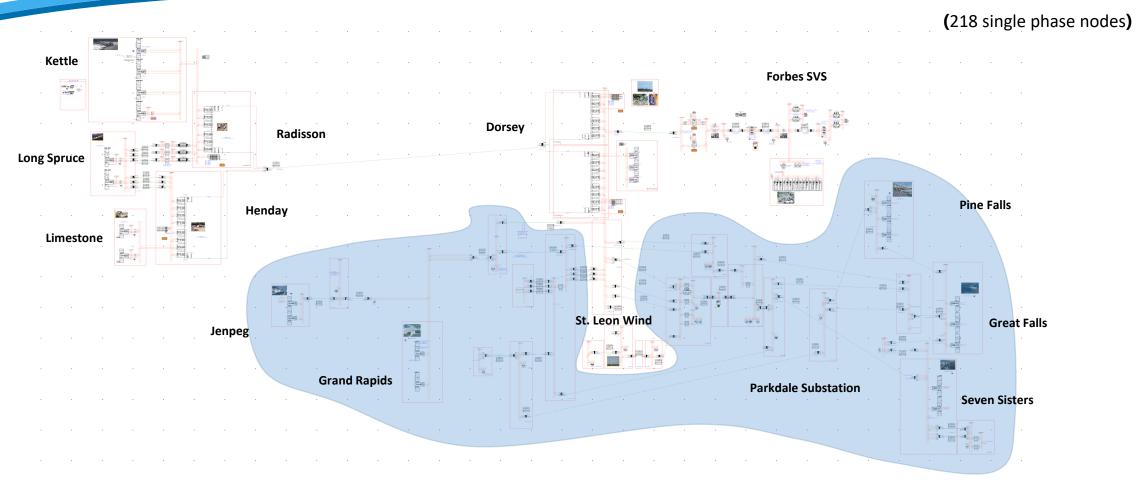


EXAMPLE 2 Manitoba Hydro Network











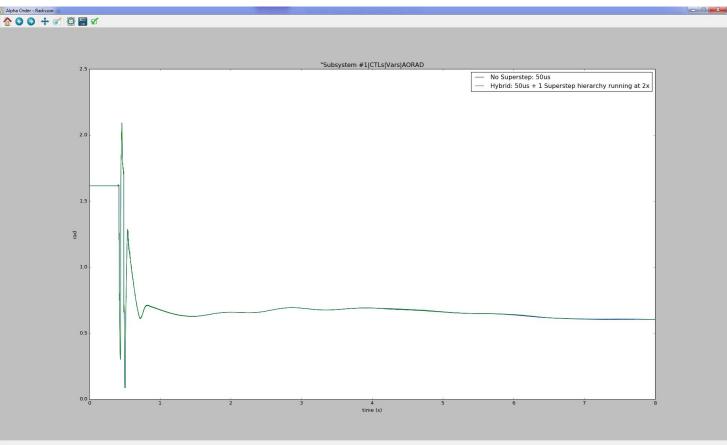
- Simulation results for a conventional single rate simulation were compared to the results for a mixed/hybrid simulation where the shaded portion of the network was modeled using a 3x super-step.
- The following modifications had to be made to the portion of the network modeled using a super-step:
 - Within the super-step hierarchy, the fault at bus YV5FLT had be removed.
 - Three (3) lines (GP1, YV51 and YV52) found completely within the super-step, required that their *alwpi* parameter be set to 'Yes', allowing them to represented as a PI. Presumably because they are too short for the super-step. (1.5 * super-step Δt)
 - Also, three (3) lines interfacing the super-step and main time-step had to be artificially lengthened so that their modal travel times were extended to 1 time-step. (lines D5R, D13R and D16R)
- Time Domain signals were compared for the start-up of Bipole 1 nine seconds into the simulation. The Power order was set to 400 MW. Various signals in the vicinity of the HVDC converters were monitored including DC bus voltages, AC side voltages and DC currents. Results are presented below. Qualitatively, at least, the results look like they match well.





Bipole 1 Start-up

Alpha Order Radisson

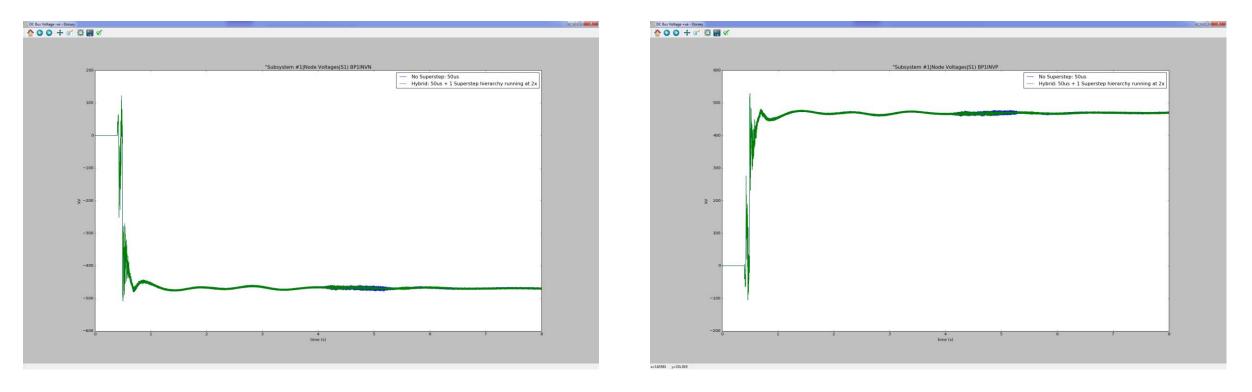






Bipole 1 Start-up

Positive and Negative DC Voltages at Dorsey



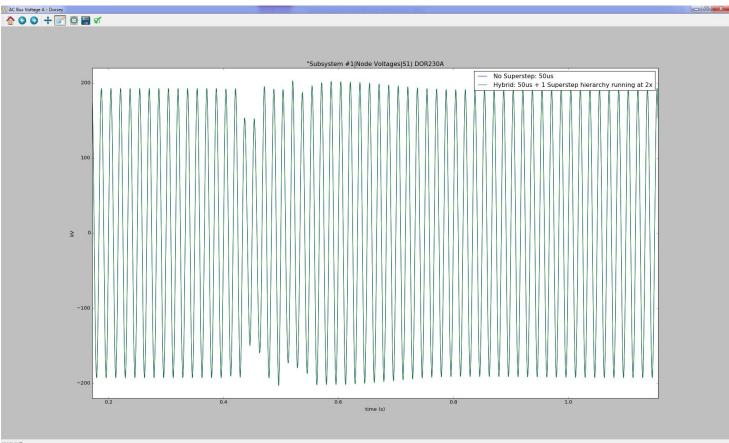


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Bipole 1 Start-up

AC Bus Voltage (Dorsey)





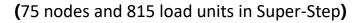


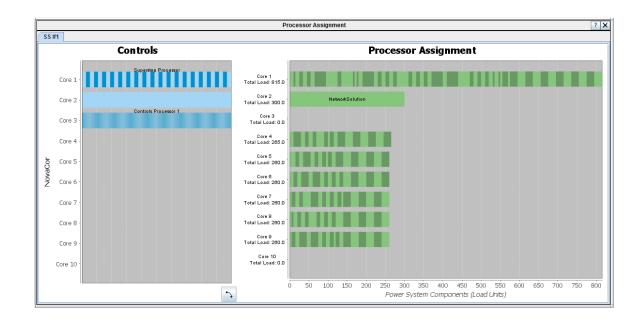
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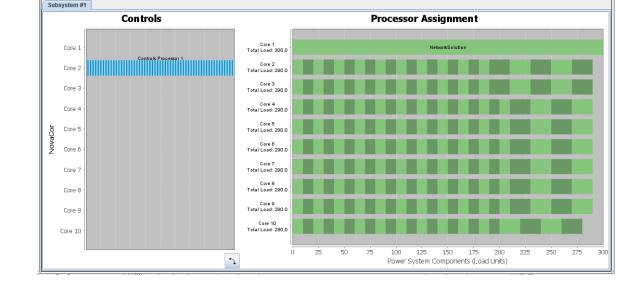
Conventional Single-Rate Simulation

(218 nodes and 2600 load units on Chassis)









Processor Assignment

Technologies



- The superstep feature provides a convenient, accurate, and stable approach to model system equivalents for large networks in RSCAD. This feature makes it possible to preserve the detail of the EMT environment for the system equivalent.
- Superstep allows a large network to be simulated in a span of several timesteps
- It is used to model remote systems
- Network Solution, Power System Components and Controls are all simulated on a single core
- Multi-rate Tline allows connecting systems with different timesteps together



Thank You.

Questions?