Designing and Testing Protective Overcurrent Relay Using Real Time Digital Simulation

Ankush Saran
Mississippi State University
as642@msstate.edu

Padmavathy Kankanala
Mississippi State University
pk150@msstate.edu

Anurag K. Srivastava
Mississippi State University
srivastava@ece.msstate.edu

Noel N. Schulz
Mississippi State University
schulz@ece.msstate.edu

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Abstract

The Real Time Digital Simulator (RTDS) is a tool for the design, development, and testing of power system protection and control schemes. RTDS can be used for the investigation, development, and integration of new and complex power system components. The user is able to study both the device itself and the response of the existing power system to its operation (or misoperation). The Hardware in the Loop (HIL) test provides an opportunity for understanding the behavior and validating the model of physical device. In the HIL simulation, parts or components of the virtual power system are replaced with physical devices. In the Software in the Loop (SIL) simulation, the software model replaces the physical protective device. This paper presents the modeling and testing of a Schweitzer Engineering Laboratories (SEL) 351S protective overcurrent relay using RTDS. The first part of the paper discusses HIL tests conducted with the physical SEL 351S overcurrent relay for an eight-bus power system. The second part discusses the development of a software relay model in RSCAD and real time SIL simulation. The results obtained by conducting the real time HIL are presented and procedure to conduct the SIL tests is proposed.

1. INTRODUCTION

Real time simulation is a commonly used tool for studying power system behavior in response to events. This kind of virtual test could uncover potential problems in advance. Corrective measures could then be taken before implementing the algorithm or logic in the real system. In HIL simulation, some of the components of the virtual power system are replaced with physical devices. HIL technology is one of the methods to understand nonlinear and dynamic behavior of the system and helps in building and validating a model for physical devices. Authors in [1] presented experimental design for a hardware in the loop test and a HIL test has been used for testing electric machines in [2].

Different approaches and preliminary design for HIL using National Instruments (NI) devices have been discussed in [3]. Real time digital simulator Real Time Digital Simulator (RTDS) is an effective tool for modeling and simulation of power and control systems. RTDS hardware employs high-speed DSP (digital signal processor) cords, operating in parallel, to compute simulations results with simulation step sizes as small as 2 microseconds.

Different approaches and preliminary design for HIL using National Instruments (NI) devices have been discussed in [3]. Real time digital simulator developments at Western Area Power Administration (WAPA) for testing protective relay in real time have been presented in [4]. Hardware in the loop simulation of a distance relay using RTDS had been discussed in [5].

Real time digital simulator Real Time Digital Simulator (RTDS) is an effective tool for modeling and simulation of power and control systems. RTDS hardware employs high-speed DSP (digital signal processor) cords, operating in parallel, to compute simulations results with simulation step sizes as small as 2 microseconds.

RTDS software, RSCAD includes a graphical user interface and detailed model library for power and control system components. Researchers at Mississippi State University (MSU) are working on conducting Hardware in the Loop (HIL) test and Software in the Loop (SIL) tests on the 8-bus power system model and the SEL-351S (manufactured by Schweitzer Engineering Laboratories). The first step in this process is to develop the hardware simulation interface platform in RTDS to conduct the HIL test. The second step is to develop the software overcurrent relay model. To validate the performance of developed models, the HIL and SIL results are compared and validated. Issues and challenges faced in using RTDS for HIL simulation have been discussed in [6]. Modeling of impedance relays using RTDS is presented in [7].

This paper describes the testing of a SEL-351 high speed transmission protection relay using a simulated 8-bus power system. Test results obtained for different types of faults are presented.

2. MAIN COMPONENTS REQUIRED TO CONDUCT HIL AND SIL TEST

The three main pieces of equipment that are required to conduct the HIL and SIL tests are:

1. Real Time Digital Simulator (RTDS).
2. RSCAD software.
3. SEL 351S directional overcurrent relay.

These components mentioned above are explained one by one in order to give the general idea about the equipment and how they work.

2.1 Real Time Digital Simulator (RTDS)

RTDS (Real-Time Digital Simulator) is a real-time power system simulator, which employs an advanced, and easy to use graphical user interface. The RTDS allows users to accurately develop their models and simulate them efficiently. The software used to design the power system model in RTDS is RSCAD, which involves a library of power and control system components. RSCAD allows the user to select a pictorial representation of the power system or control system components from the library in order to build the desired circuit. Once the system has been drawn with the entry of required parameters, the compiler in RTDS generates the low level code that is needed to perform simulation on the RTDS simulator. RTDS is capable of generating the real time signals, which enable the user to simulate the situations, which generally occurs in the power system.

2.2 RSCAD software

RSCAD is software that allows the user to build a test case by using the different components present in the RSCAD library. The following steps are required to prepare and run a new simulation case.

- Start the RSCAD/Draft software module.
- Create a new 'Project' and 'Case' directory in the 'File Manager' module.
- Create the new circuit diagram for simulation.
- Compile the new circuit.
- Start the simulation case from RSCAD/RunTime.

The RSCAD/Draft software module is used to create the circuit that will be simulated using the RTDS simulator. The file manager of RSCAD is shown below in figure 1. The RSCAD/Draft file menu is shown in figure 2.

Figure 1. RSCAD File Manager

Compile button Rack No.

Figure 2. RSCAD/Draft File Menu

After the successful compilation of the system, the user simulates the system by using the RSCAD/RunTime software module. The RSCAD/RunTime module is shown in figure 3.

Figure 3. RunTime Menu in File Manager

In RunTime mode, the user can plot graphs for voltage, current, power, fault, and frequency etc, can add switches, buttons, meters and sliders for fault application, to increase or decrease different physical quantities. After completing the selection of plots in the RunTime, then the user can simulate the system by pressing a button "Start Simulation" which is present in the RSCAD/RunTime module. The RSCAD/ RunTime toolbar is shown in figure 4.

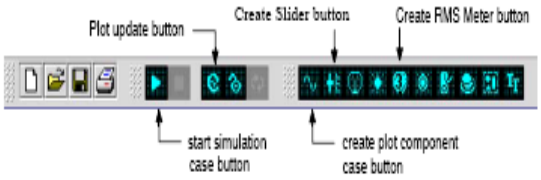

Figure 4. RSCAD/RunTime toolbar

2.3 SEL 351S directional overcurrent relay

SEL 351S is a directional overcurrent relay, which operates for a given value of current, and if the current goes above the given value then it generates a trip signal. SEL 351 has automatic as well as manual open and reclose mechanisms for line to line and line to ground faults. SEL 351 relay setting can be done through AC**SEL**ERATOR software installed on a computer using serial input/output wire. The relay can be set directly from the front panel also.

3. TEST CASE USED FOR SIMULATION

An 8-bus terrestrial based power system developed from a modified version of an RTDS test system is used as a test case to perform HIL test using SEL 351 overcurrent relay and SIL test using software relay model. The power system was built in RSCAD. Components of 8-bus system are:

- 230 kV AC source
- Speed governor and turbines, Static exciter
- Circuit Breaker
- 230 kV/230kV(delta-star) Transformer
- Transmission line
- 1200 MVA, 15KV Synchronous machine

The 8-bus power system is shown in the figure 5 and all the components are labeled. The fault is applied on bus 8 and the type of fault applied is line to ground fault. The test system consists of two parallel transmission lines between source and load. There are in total 4 circuit breakers in the system namely BRK1, BRK2, BRK3 and BRK4. BRK1 and BRK2 are on the transmission line 2 while BRK3 and BRK4 are present on the transmission line 1.

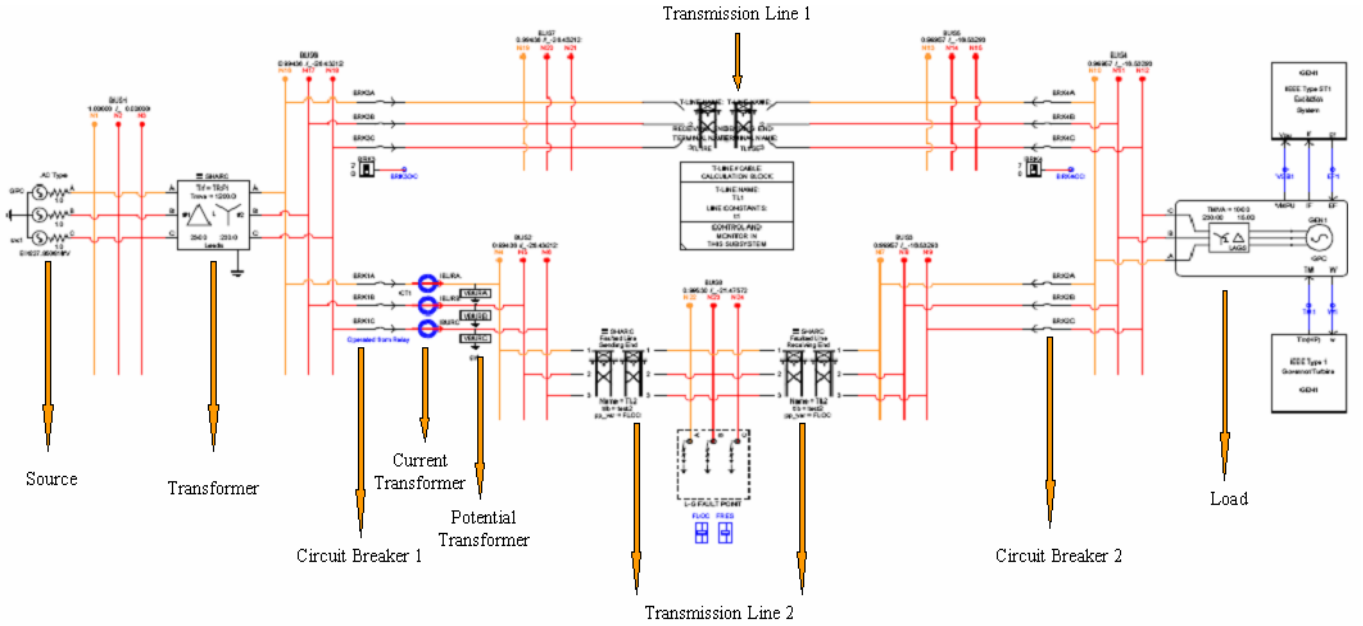

Figure 5. Test case: 8-bus power system

Here, the circuit breaker 1 is controlled by SEL 351 relay while circuit breaker 2 is controlled by the logic designed in RSCAD software. Current transformer and potential transformer are modeled in detail to reflect real system characteristics. The CT ratio of the current transformer is 300 and the PT ratio of potential transformer is 64.70.

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4. HARDWARE IN THE LOOP (HIL) TEST

Hardware in the loop test is defined as "a test in which software model of a power system designed in RSCAD is connected with an actual physical hardware device in order to observe the system behavior or response to different conditions" [5]. In a HIL simulation, parts of components of the virtual power system are replaced with physical devices. HIL technology is one of the methods to understand non-linear and dynamic system and helps in building and validating a model for physical devices. The block diagram for HIL test is given in figure 6. Figure 6 shows the block diagram of Hardware in the loop test. The 8-bus system, fault logic and control logic are formed in RSCAD.

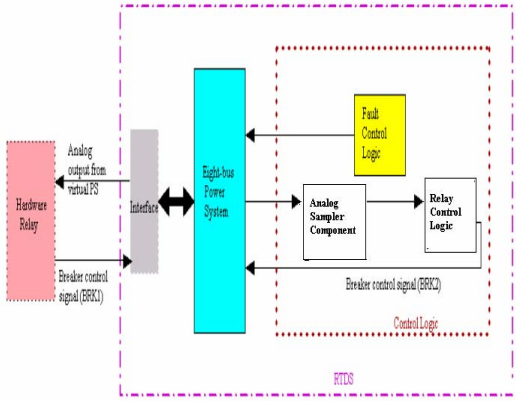

Figure 6. HIL test block diagram

In this test the signals are interfaced between the SEL 351 relay and RTDS. The 8-bus power system built in RSCAD is uploaded in the RTDS and then SEL 351S relay is connected to the RTDS through cables. The relay senses the voltage and current from the RTDS system and in case of any fault; it sends out the trip and reclose signals to the simulated circuit breakers in the power system. Figure 7 shows the HIL simulation with RTDS and SEL relay.

5. SOFTWARE IN THE LOOP

Software in the loop (SIL) test is defined as "A test in which software model of the power system designed in RSCAD is connected to a software model of the device, which performs the same operation as a physical hardware device in order to observe the system behavior in different conditions. [4]"

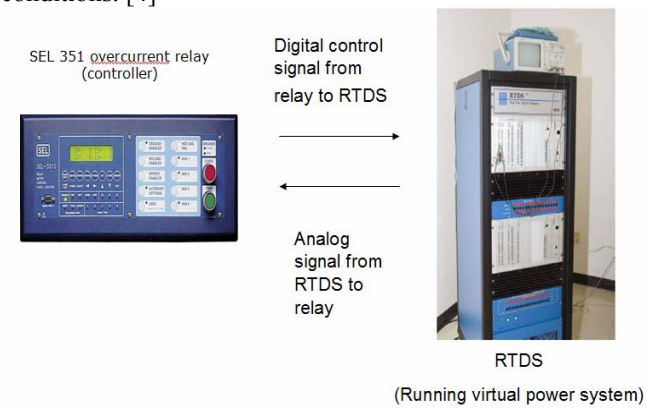

Figure 7. HIL simulation with RTDS and Relay

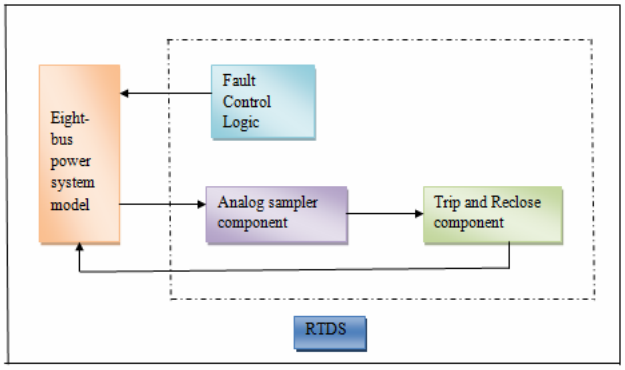

Figure 8. SIL Test Block Diagram

Figure 8 shows Software in the Loop (SIL) test. The 8-bus system, fault control logic, analog sampler component, trip and reclose component are formed in RSCAD and then compiled in the RTDS to run the simulation. The 8-bus power system and relay logic built in RSCAD is uploaded in the RTDS. The analog sampler calculates the I_{RMS} values of the three phases and if the calculated I_{RMS} (RMS current) value is greater than the pickup values the relay senses the fault and sends out the trip and reclose signal to the simulated circuit breakers in the power system. This paper will discuss the development of a software model of an overcurrent relay in RSCAD, where the current magnitude is measured using a technique involving two samples of a waveforms taken at discrete time intervals.

6. CONTROL LOGIC

Different control logic models developed in the RSCAD for conducting the HIL and SIL are discussed in this section.

6.1. Fault Control Logic

The fault control logic is built in RSCAD. The fault logic is built in order to put a fault on transmission line 2. The fault type used here is a line to ground faults and is applied on bus 8.

The fault logic consists of two parts. The first part of the fault control logic is used to control the point on the wave called as fault inception point. The fault button when pressed produces a 20millisecond pulse, which is longer then the one cycle at 60Hz. A pulse is produced by the AND gate and then combined with the zero crossing and fault button. The pulse drives the point on wave logic, which is comprised of a slider, a gain block, and a pulse duration timer to detect the rising edge. The figure 9 shows the fault control logic circuit.

The second part of the control logic circuit is used to control the fault type and location. Fault switches for the phase to ground fault types are combined to create the necessary integer value. This value is multiplied by the pulse from the first part of the logic, thereby creating a pulse width with an integer value that can control the fault branches.

6.2. Analog Signal Sampling

Digital relays require that an analog signal is sampled at a rate equivalent to the protection cycle time. The analog signal is sampled at a rate of 5.76 kHz or 96 samples per cycle for a 60Hz base. The signal is down sampled at a rate of 0.480 kHz or 8 times per cycle as the protection cycle is set to 8 times per cycle. The root mean square value will be calculated using two sampling technique and the equation (1) calculates the magnitude of input signal using this technique [8].

$$I^2 = \frac{i_k^2 + i_{k-1}^2 - 2i_k i_{k-1}\cos w_0 \Delta t}{\sin w_0 \Delta t^2} \qquad (1)$$

The input signal is first up sampled at 5.76 kHz and then down sampled at 0.480 kHz. Equation 1 introduces the two-sample technique for determining the magnitude of a signal from sampled data taken at discrete intervals. In this model, sampling is done at a constant rate. Therefore the numerator and denominator containing the terms cos, sin, Δt and w can be computed. A single state buffer is used to get the present and previous sampled data. The sampled data is squared and summed together completing the first part of the numerator in the equation 1.

6.3. Circuit Breaker Control Logic

6.3.1. CB Control Logic for HIL Test

The circuit breaker logic was built in RSCAD. Circuit breaker 1 (CB1) is operated by external hardware SEL 351S

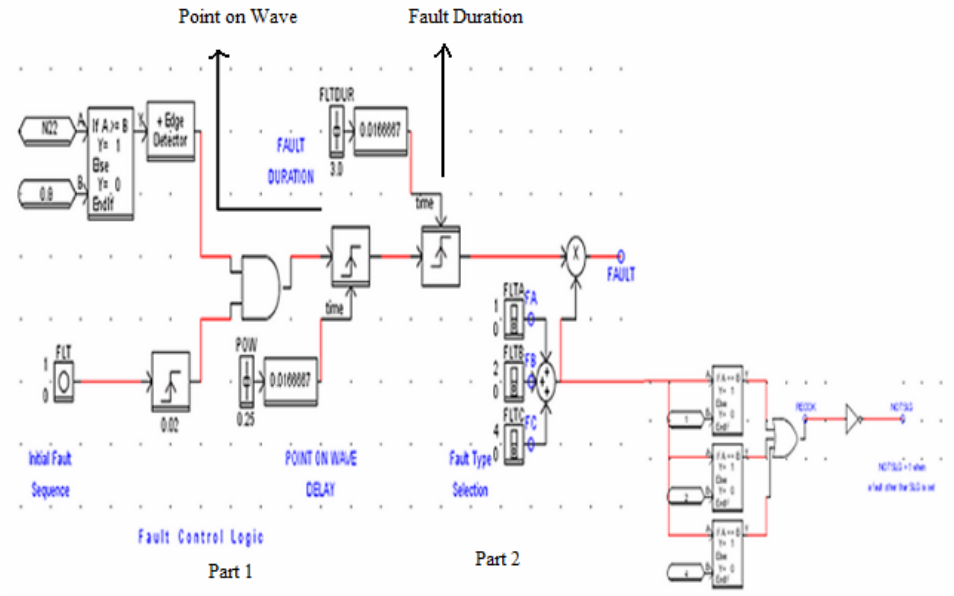

Figure 9. Fault control logic

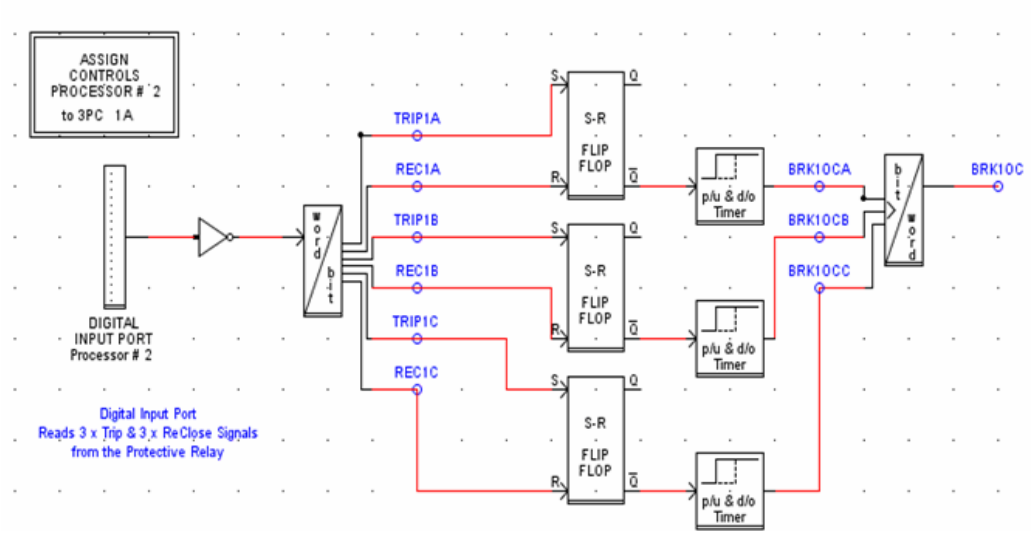

Figure 10. Sampling logic

overcurrent relay. Circuit breaker 2 (CB2) is operated by a logic designed in RSCAD. The logic for CB2 is designed in order to coordinate with the breaker 1. This implies that if the CB1 opens then CB2 should also open but after a delay of one or two cycles and similarly if CB1 recloses then CB2 should also reclose after some delay.

6.3.2. CB Control Logic for SIL Test

The circuit breaker 1 (BRK1) and 2 (BRK2) control logic methods were built in RSCAD. When the measured/calculated RMS current is greater than the specified pick up value, the IF THEN ELSE block output will be 1. The type of fault is checked by the second IF THEN ELSE block, if the fault applied is phase to ground then the output will be 1. These two outputs forms an input to the AND gate. A trip signal to the BRK1 and BRK2 are send out if the output of the AND gate is high.

7. BASIC OPERATION OF HIL TEST

The current flowing in to the circuit breaker 1 which is sensed by SEL 351S relay is 646Amps for considered test case and the CT ratio of a current transformer is 300. So the current flowing out of the current transformer is 2.15 A (646/300). This RMS current of 2.15Amps can be viewed

and verified in the plot of currents coming out of the current transformer i.e., IburA, IburB, and IburC.

For the 8-bus power system, the nominal RMS voltage and RMS current during the normal operation of the system is 132kV and 2.15 Amps in CT. Now, if the fault is applied say single line to ground fault, then the voltages in the transmission line 2 shoots up to 212kV approximately and current shoot up to 3.35A in CT. Now, in the SEL 351S settings we specified that the current across the breaker should not be greater than 1.5 times of the nominal current. So the threshold current at which the breakers stay closed is 1.5*646 = 969Amps or RMS current (burden current Ibur) coming out of the CT should not be more than 3.20Amps.

In the HIL test there are two main functions. Firstly, at any type of line to ground fault breaker 1 should open and reclose by getting the signals from SEL 351S relay. Secondly, to design circuit breaker 2 control logic in RSCAD, such that the breaker 2 should open and reclose in accordance with breaker 1 but after a delay of few cycles.

SEL351 relay senses the current and voltages from the RTDS and in case of any fault, sends out the trip and reclose signals to the simulated circuit breakers in the power system. Circuit breaker 2 in the system on the transmission line 2 should be coordinated with breaker 1. During the fault condition, breaker 1 opens then after a delay of three cycles breaker 2 opens. Now if the fault is cleared then a reclose signal is generated in breaker 1 to close the breaker 1 after 65 cycles. Similarly, a reclose signal is generated in breaker 2 to close the breaker 2 after a delay of five cycles from the reclose signal generated in breaker 1.

7.1. Hardware in the Loop Simulation Results

The HIL test is conducted and the system is simulated for 2 seconds in order to show the tripping, opening and reclosing of breakers clearly. The results of the HIL test for different line to ground fault are presented here.

7.1.1. No Fault condition

During the no fault condition, the nominal voltage and nominal current flows in to the system and there is no trip signal and circuit breaker 1 and circuit breaker 2 are closed. The voltage and current measured by potential transformer and current transformer are perfectly sinusoidal.

7.1.2. Fault Conditions

When a line to ground faults like single line to ground (SLG), double line to ground (L-L-G), and three phase to ground faults are applied on bus 8 then a trip signal is generated in the circuit breaker 1 and after a delay of one cycle breaker 2 trip signal is generated. After a trip signal, the breaker one open and then breaker 2 opens after a delay of three cycles. If the fault is cleared then a reclose signal is generated in breaker 1 to close it after a delay of 65 cycles from breaker 1 opening and in the similar way reclose signal is generated in breaker 2 after a delay of 65 cycles from the breaker 2 opening to close it. If the fault is not cleared then the breaker 1 and 2 remains open to protect the system from heavy damages. Simulations are done for single lint to ground, double line to ground fault, and three phase to ground faults. Here only the behavior of system for three phase to ground fault is presented and shown in figure 12.

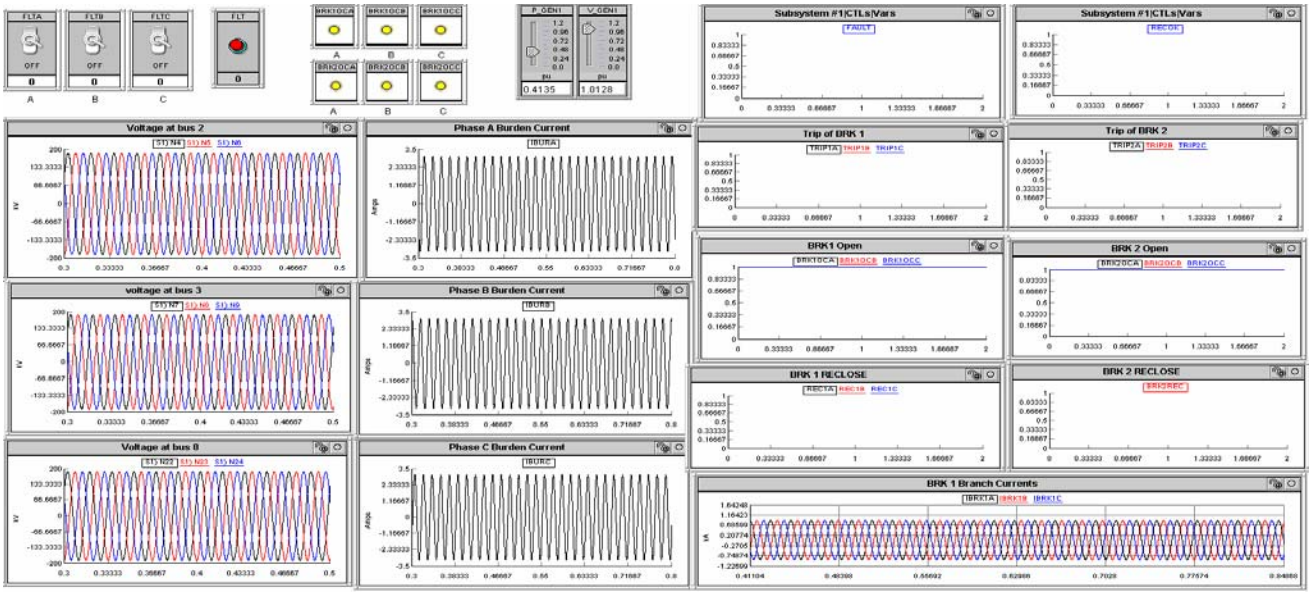

Figure 11. No Fault condition

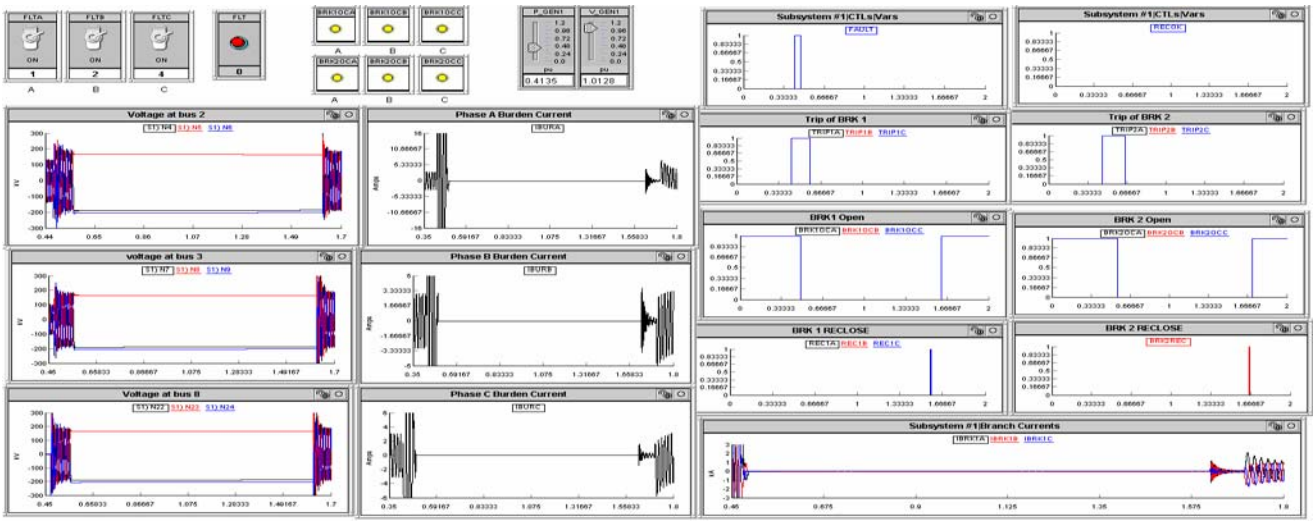

Figure 12. Three phase to ground fault

8. SIL Test Basic Operation

The basic operation in the SIL test is to develop an overcurrent relay model in RSCAD and conduct the SIL test to know the behavior of the eight-bus power system model developed in RSCAD. Different phase to ground fault conditions will be applied and the behavior of the system has to be studied. The basic operation of the SIL test is same as the basic operation of the HIL test. When a fault is applied, the IRMS value is calculated and compared with the pickup value. If the IRMS calculated value is greater than the pickup value, the relay control logic sends a trip and reset signal to the circuit breaker 1 and 2 (BRK1 and BRK2). Design for the most of the block has been done and simulation will be future work.

9. SUMMARY

In this paper, Hardware in the Loop (HIL) test has been presented using RTDS and SEL-351S relay. The development of an eight- bus power system, control logic, hardware and software setup were discussed in detail. Simulation results for three phase to ground fault was presented. The Software in the Loop (SIL) test and relay model development is ongoing research work going at Mississippi State University. Future work also includes conducting the HIL test and SIL test for the 4-bus Shipboard power model.

9. ACKNOWLEDGEMENT

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Biography

Ankush Saran is pursuing his Master's degree at Mississippi State University in the Electrical and Computer Engineering Department and he received his Bachelor of Engineering (B.E) degree from Vaish College of Engineering, Haryana, India in 2007. He is a member of IEEE and his research interest includes protection, security, simulation and modeling of power system.

Padmavathy Kankanala is pursuing her Master's degree at Mississippi State University (MSU) in the Electrical and Computer Engineering Department and received her Bachelor of Technology (B.Tech) degree in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University (JNTU), Andhra Pradesh, India in 2006. She is a member of IEEE and her research interests include power system protection, modeling and simulation, real time analysis and artificial intelligence.

Anurag K. Srivastava received his Ph.D. degree from Illinois Institute of Technology (IIT), Chicago, in 2005, M.Tech from Institute of Technology, India in 1999 and B.Tech in Electrical Engineering from Harcourt Butler Technological Institute, India in 1997. He is working as Assistant Research Professor at Mississippi State University since September 2005. Before that, he worked as research assistant and teaching assistant at IIT, Chicago, USA and as Senior Research Associate at Electrical Engineering Department at the Indian Institute of Technology, Bangkok, Thailand. His research interest includes real time simulation, power system modeling, power system security, power system deregulation and artificial intelligent application in power system.

Noel N. Schulz received her B.S.E.E and M.S.E.E degrees from Virginia Polytechnic Institute and State University in 1988 and 1990, respectively. She received her Ph.D. in EE from the University of Minnesota in 1995. She has been an Associate Professor in the ECE department at Mississippi State University since July 2001. She currently holds the TVA endowed professorship in power systems engineering. Her Research interests are in computer applications in power system operations (terrestrial and ship systems) including artificial intelligence techniques. She is a NSF CAREER award recipient. She has been active in the IEEE Power and Energy Society and served as Secretary for 2004-2007 and Treasurer from 2008-2009. She was the 2002 recipient of the IEEE/PES Walter Fee Outstanding Young Power Engineer Award.