

Comparative Assessment of Differential Relay Model Performance with Hardware Equipment

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Keywords— Hardware in the loop, real time digital simulator, differential relay, relay modeling, bus protection.

Abstract

The stability and security of the power system has to be maintained under different fault conditions. Modeling and simulation of different fault conditions are needed for a better design of future Shipboard Power Systems (SPS). The protective relay plays a major role in the protection of the power system. The real time digital simulator (RTDS) is an effective tool for modeling and simulation of a power system, protective relay and the controls needed to simulate different fault conditions in real time. The Hardware in the Loop Testing (HIL) provides the opportunity to understand the behavior and validate the model of a physical device. This paper addresses the HIL tests of the Schweitzer Engineering Laboratories SEL-487B bus differential relay and the software differential relay model development. The software relay model is designed by using the RSCAD software suite and is validated using the results from the HIL testing.

The Hardware in the Loop (HIL) tests and the software relay model tests has been implemented using an 8-bus terrestrial power system test case. The consistency and performance of the software differential relay model has been analyzed.

1. INTRODUCTION

Real time simulation is quite beneficial to observe the power system behavior in response to transients and changes in the power system. Modeling and simulation of different fault conditions are needed to provide better security and maintain the stability of the power system. Real time simulation is a widely used tool to study the behavior of a power system in different conditions. The Real Time Digital Simulator (RTDS) is an effective tool for modeling and simulation of power and control systems.

In a HIL simulation, the virtual power system is connected to the actual physical devices. HIL technology is one of the techniques used to understand the nonlinear and dynamic behavior of the physical device, and helps in building and validating a model to control the physical devices. Authors in [1] presented experimental design for hardware in the loop test and HIL test has been used for testing electric machines in [2]. The basic functionality and applications of the SEL-487B bus differential relay given in [3] were analyzed.

Shipboard Power Systems (SPS) have unique characteristics and SPS devices have to be tested under different conditions. It becomes very important to investigate the efficiency of a protection device and how it behaves in different scenarios. The HIL test provides a platform to test the performance of the equipment under different conditions and HIL simulation will be very helpful for designing protection system for SPS. Real time

assessment for SPS protection has been presented in [6], while simulation of an electric ship in an efficient way has been discussed in [7].

Issues and challenges faced in using RTDS for HIL simulation of SPS have been discussed in [8]. Authors in [9] presented modeling effort for impedance relay using RTDS.

This paper describes HIL testing of SEL-487B bus differential relay and also software in the loop testing. Test results obtained for different types of faults have been presented. The software relay model was verified using the simulation results.

2. POWER SYSTEM TEST CASE IN RSCAD

The power system test case considered for the research work consists of eight-buses and was developed in RSCAD as shown in Fig. 1. The test case is comprised of the following components:

1. 230kV AC source;
2. 230kV (Δ -Y) transformer;
3. 100 km long transmission lines;
4. A 1200MVA, 15kV synchronous machine with a base frequency of 60Hz;
5. Governor mechanism with base frequency of 60Hz;
6. Current transformers CT1 and CT2 respectively.

Fault Inception logic was used to simulate different conditions at Bus 8. Breakers on either side of the bus 8 are

operated by the SEL-487B bus differential relay. The relay isolates the bus 8 when there is a fault by opening both the breakers at once. The test system has two parallel transmission lines between source and load. The current transformers draw currents and send them to the hardware relay through a hardware interface designed in RSCAD.

The RSCAD software suite employs an advanced and easy to use graphical user interface. The software is comprised of several modules, which enable the user to design, simulate and analyze the simulation output. The users can model the system using the components present in the power and control system library and simulate it using the RTDS after compilation. The file manager window in the RSCAD has ‘Draft’, ‘Runtime’, ‘Multiplot’, ‘Cable’, ‘T-Line’, ‘Help’, ‘Convert’ and ‘Manuals’ menus. The power system modeling is done through the ‘Draft’ option in RSCAD, where the requisite components can be modeled using a drag and drop interface provided. The transmission lines present in the power system test case have been modeled using the ‘T-Line’ option. Once the model is compiled without any errors, the simulation results can be observed through the ‘Runtime’ option.

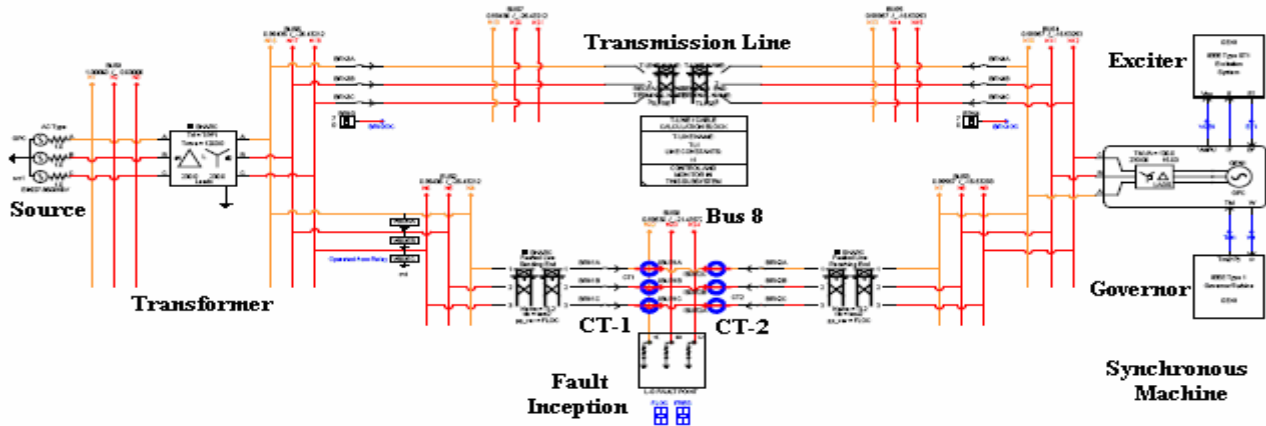


Fig. 1. 8-bus power system test case

3. SEL-487B BUS DIFFERENTIAL RELAY

The SEL-487B bus differential relay can protect bus systems with up to 18 terminals (54 CTs) and six protection zones. In order to improve the efficiency of protection the six zones of the power system can be defined and the relay can be coordinated accordingly. The use of differential relay increases the security and improves the speed of fault detection. The SEL-487B relay can be set based upon the power system characteristics through the ACSELERATOR software.

4. HARDWARE IN THE LOOP SETUP

The SEL-487B bus differential relay was set up and interfaced to the RTDS as shown in Fig.2. The relay senses the currents from the power system running in the RTDS system through the sensors, and in the case of any fault condition, the relay sends out the tripping signals to the circuit breakers present in the power system through actuators.

Hardware in the Loop Test using RTDS

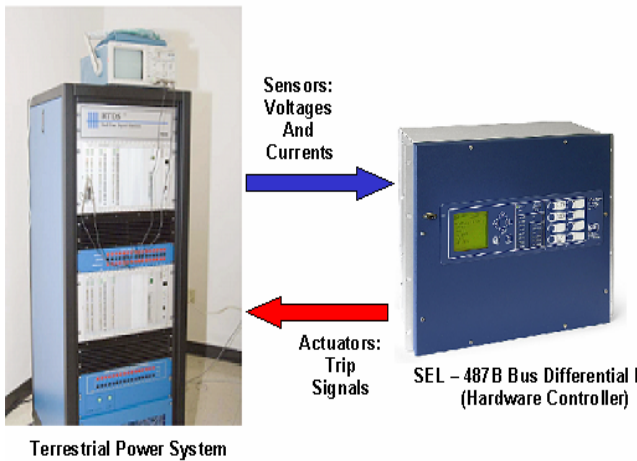


Fig. 2. HIL setup using RTDS for SEL-487B

The currents from the power system being simulated in the RTDS are sent out through the output of DDAC board as shown in Fig.3. The signals from the relay are sent to the breaker through the digital input port in the front panel of the RTDS.

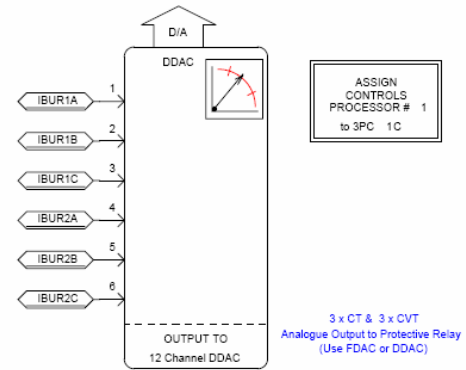


Fig. 3. Analog output currents to relay

The logic present in the fault inception block allows the user to inject single phase line to ground, double phase line to ground and three phase line to ground faults at the bus and eventually look at the behavior of the hardware relay.

5. SIMULATION RESULTS

The simulation results mainly portray the results of the hardware in the loop (HIL) testing using the actual relay hardware and the software in the loop (SIL) testing using the software bus differential relay model. Single phase line to ground and two phase line to ground faults were simulated at bus 8 of the power system test case. Fig. 4 shows the CT currents, voltage at bus 8 and the status of the breakers in the case of HIL testing when there is no fault at the bus 8. When there is no fault at bus 8, the breakers are closed, and there is no signal sent by the relay to the circuit breakers present in the system.

The simulation results for single line to ground fault on phase A and double line to ground faults on phases A and B at bus 8 are shown in Fig. 5. In Fig. 5 the CT currents and voltages have been shown along with the status of the breakers when there is a single line to ground or double line to ground fault.

Based upon the normal usage by the utility, it does not re-close in this HIL test. The way the trip signal is issued to the breakers in the power system, after the fault inception can be seen in Fig. 6 and Fig. 7. You can see that the breakers trip, but do not re-close after the fault is cleared.

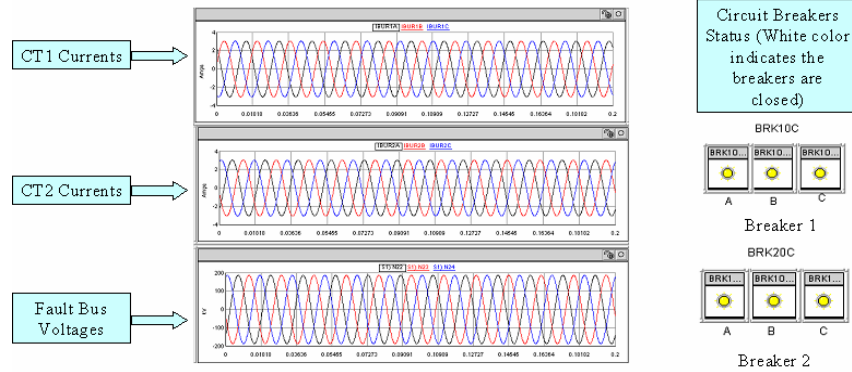


Fig. 4. CT currents & voltage at bus 8 without fault

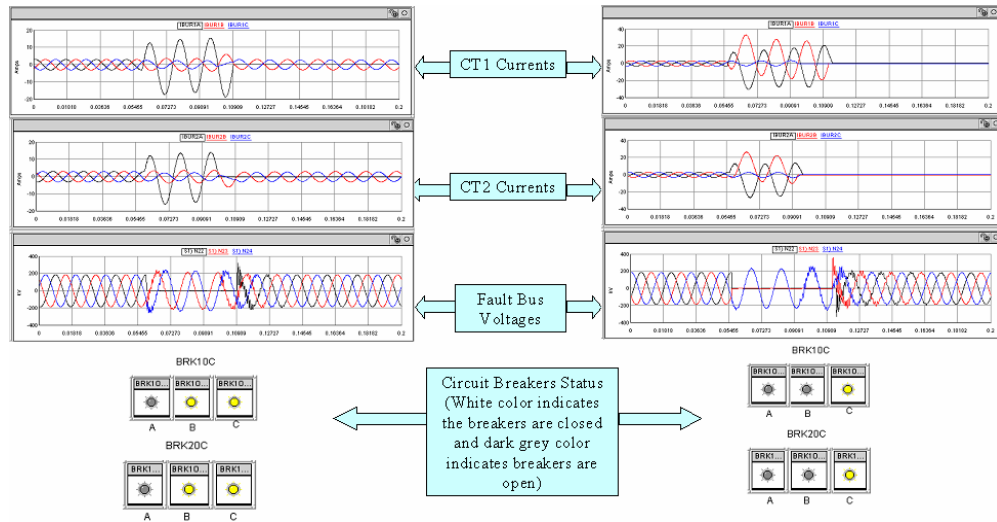


Fig. 5. CT currents & voltage at bus 8 for LG (phase A) and LLG fault (phases A & B)

The software bus differential relay has been developed in RSCAD based upon the functionality of the actual SEL-487B bus differential relay. The relay model includes Discrete Fourier Transform (DFT) filters, and sampling components to extract the fundamental component of the current by filtering out the harmonics present.

The sampled fundamental component of the current in each phase is used to define the trip logic for phases A, B and C respectively. The software relay model has the capability to issue the trip and a re-close signal as soon as there is a fault incepted in the protected bus.

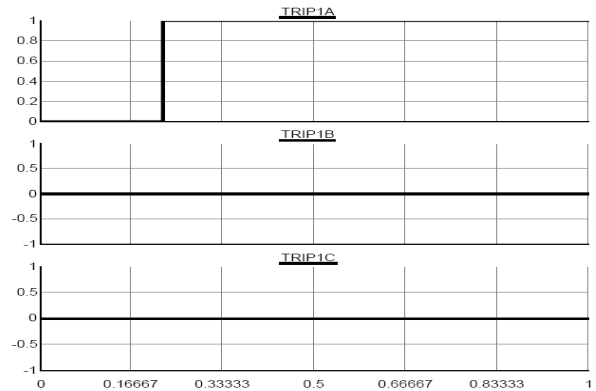


Fig. 6. Trip signal – LG fault in phase A

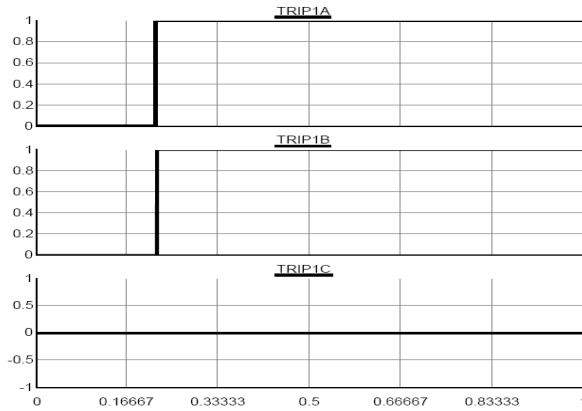


Fig. 7. Trip signal – LLG fault in phases A & B

The faults were incepted at bus 8 of the eight-bus power system using the similar fault control logic, as in the case of the HIL test. When there is a fault in phase A, the relay model could sense it and issue a trip signal to open the breaker and also a re-close signal to close the breaker as soon as the fault is cleared. In Fig. 8 the trip and re-close signal for the fault in phase A is shown, and in Fig. 9 the trip and re-close signals for the fault in phases A and B respectively is shown.

The simulation results of the software in the loop (SIL) test using the software differential relay model in RSCAD and the hardware in the loop (HIL) test using the actual SEL-487B bus differential relay were compared in order to validate the software differential relay model in RSCAD. Upon comparison it was found out that the software relay model trips the breaker as quickly as the actual relay hardware, and also re-closes the breaker. For a fault duration of 0.5seconds, as soon as the fault is incepted at 0.1seconds at the bus 8, the software relay model trips at 0.25seconds, which is exactly where the actual hardware relay trips, the breakers.

The software differential relay model, does not include all the functionality of the actual hardware relay, but when it models the basic operations of fault detection, and issuing trip and re-close signals to the breakers in the power system, the relay model gave consistent results. If the other functionalities like the breaker failure detection, which are present in the actual relay hardware, are included, the

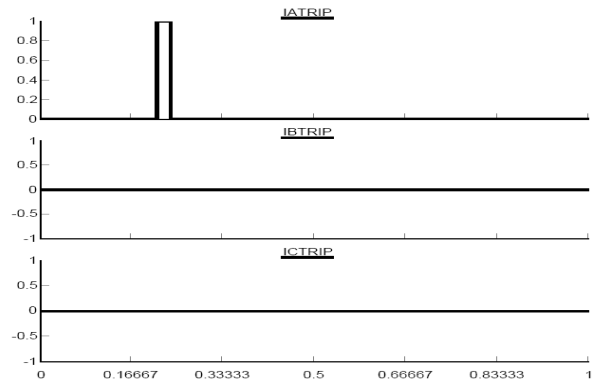


Fig. 8. Trip & re-close – LG fault in phase A

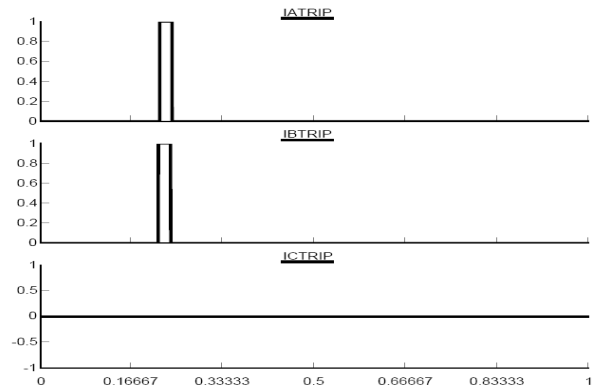


Fig. 9. Trip & re-close – LLG fault in phases A & B

software differential relay model can be used for a wider range of tests.

6. SUMMARY

Hardware in the loop (HIL) testing of the SEL-487B bus differential relay has been presented in this paper. The hardware setup, fault control logic and the power system test case development have been discussed in detail. The development of the software bus differential relay model has also been explained. The SEL-487B bus differential relay and the software bus differential relay model in RSCAD were looped in with the eight-power system and tested for different fault conditions. Comparing its results with those of the HIL test finally validated the software relay model. The software relay model was consistent with adequate functionality.

The future work is to conduct the hardware in the loop and the software in the loop using a 4-bus shipboard power system. The main idea behind this test would be to look at the consistency of the software bus differential relay model developed in RSCAD.

7. ACKNOWLEDGEMENT

The authors would like to thank Heather Meiklejohn at RTDS Technologies for her help with modeling activities. This research was funded through ONR Grant No. N00014-02-1-0623, ONR Grant No. N00014-08-1-0080, and DoD DURIP Funds Grant No. N00014-06-1-0752.

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Biography

Vamsi K Vijapurapu was born in Andhra Pradesh, India in 1985. He received his Bachelor of Technology (B.Tech) Degree in Electrical & Electronics Engineering from Chaitanya Engineering College, Andhra Pradesh, India in 2006. He is presently pursuing his Master's Degree at Mississippi State University (MSU) in the Electrical &

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