

# Small Time-step ( $< 2\mu\text{Sec}$ ) VSC Model for the Real Time Digital Simulator

Trevor Maguire     James Giesbrecht

**Abstract**—This paper describes a method for time-domain electromagnetic transients modeling of Voltage Source Converter ( VSC ) bridges in a real time digital simulator using a short time-step (  $< 2\ \mu\text{sec}$  ). The method supports the modeling of many valves in one lumped connected network. The model of the VSC bridge is interfaced into the time-domain simulation of a main network that uses a larger time-step (  $\sim 50\ \mu\text{sec}$  ).

The representation of each valve in the EMT type program is provided by a fixed conductance in parallel with a current source. The calculation of the parallel current source is modified to facilitate the representation of the ON and OFF states of the valve.

**Keywords:** Voltage Source Converter, VSC, electromagnetic transient simulation, real time simulation

## I. INTRODUCTION

Modeling of voltage source converters (VSC) in real-time digital simulators has always been challenging. In association with VSC modeling, it is often required to include large networks containing many lines, machines and buses in the simulation. To do this without using an overly large amount of real-time hardware, it is necessary that a time-step in the range of  $50\ \mu\text{sec}$  should be used for modeling the main network. However, to properly simulate the operation of the VSC bridges, the turn-on/turn-off resolution for the valves must be in the order of a few  $\mu\text{sec}$ .

In non-real-time electromagnetic transient simulation programs, interpolation within the time-step is used to provide the firing resolution required by the VSC models. Whenever switching occurs within a time-step, the EMT program decomposes the network matrix according to the new switching state and proceeds from the point of interpolation. If several valves switch at different points during a single time-step, it is then necessary to decompose the network matrix several times during that interval. The occurrence of multiple decompositions per time-step can be expected because the turn-on of a valve often leads to the turn-off of others. Off-line non-real-time EMT programs can handle this without difficulty, but execution time is extended (i.e slowed down).

In real-time electromagnetic transients simulation, it is not

a practical option to interpolate and decompose the main network matrix several times during a single time-step. The difficulty becomes clear when considering the effect of a switching point that occurs very late in the time-step. There may not be enough time to complete the interpolation and decomposition before real time requires that the simulation move to the next time-step. Therefore, interpolation as a general method has limitations when applied to real time simulation.

This paper explores a new approach in VSC modelling implemented for the RTDS® simulator. The technique builds on past efforts, primarily by Hui and Christopoulos, to develop methods for fast time-domain simulation of switching networks [1]. The main advantage of the Hui and Christopoulos algorithm for real time simulation is that decomposition, or inversion, of the Dommel network conductance matrix [2] is not required during a simulation. The same Dommel branch conductance represents the valve in the “ON” state and the “OFF” state. The difference in state is completely represented by the Dommel history current injection. The reduction in computational load allows the simulation of VSC bridges to be conducted with time-steps less than two (2)  $\mu\text{sec}$  in real-time hardware. The small time-step VSC bridge simulation, implemented with the Hui and Christopoulos algorithm, is numerically interfaced to the main network solution running (typically) with a  $50\ \mu\text{sec}$  time-step. The basic concept for the interface can be drawn from early work on interfacing digital simulators with analog equipment [3].

The paper discusses valve representation and the selection of parameters. The paper also presents simulation results and discusses hardware implementation for real-time simulation including computational and I/O issues.

## II. VALVE REPRESENTATION

The valve is represented in the “ON” state as an inductor and in the “OFF” state as a series-connected RC branch as illustrated in Figure 1. The Dommel resistance of the inductor representation,  $R_L$ , must equal the Dommel resistance of the RC representation,  $R_{RC}$ , in order to avoid decomposing or inverting the Dommel conductance matrix during real-time operation when a valve switches state.

The desirability of a damping resistance,  $R$ , in series with the capacitance representation is mentioned by Pejovic and Maksimovic [4]. However, little guidance is provided as to selection of the  $R$ ,  $L$  and  $C$  values illustrated in Figure 1. Of

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course, it is required that the selected values should ensure that  $R_L = R_{RC}$ .

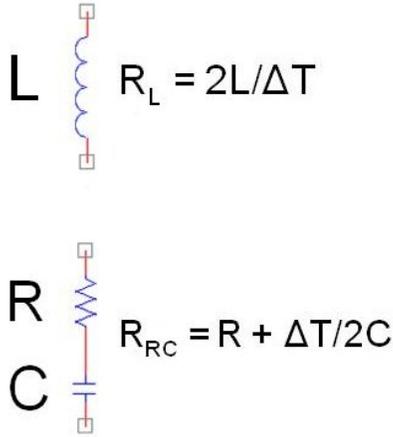


Fig. 1. Valve Representation

Clearly, the connection of valves in various simulations will have many topologies and  $2^N$  states where  $N$  is the number of switches in a particular simulation. Consequently, because of the many possible topologies, a heuristic approach has been taken to selecting the damping level provided by the series resistance in the “OFF” valve representation. The current response to an impulse of voltage applied to an RLC branch (such as one “OFF” valve in series with one “ON” valve) is given by (1).

$$H(S) = \frac{1}{L} \frac{S}{S^2 + \left(\frac{R}{L}\right)S + 1/LC} \quad (1)$$

The roots of the response will be the same for other disturbances. It is common to define damping factor  $\zeta$  and natural frequency  $\omega$  for an RLC series branch according to (2) and (3).

$$2\delta\omega = R/L \quad (2)$$

$$\omega = 1/\sqrt{LC} \quad (3)$$

In that case, (1) can be re-written in the usual form as (4).

$$H(S) = \frac{1}{L} \frac{S}{S^2 + 2\delta\omega S + \omega^2} \quad (4)$$

Having the same Dommel resistance for the  $L$  and  $RC$  branches requires that:

$$\frac{2L}{\Delta T} = R + \frac{\Delta T}{2C} \quad (5)$$

If  $R = 0$ , then damping factor  $\zeta = 0$  and  $\omega = 2/(\Delta T)$  where  $\Delta T$  is the small time-step size. If  $R > 0$ , then  $\zeta > 0$  and the natural frequency,  $\omega$ , is given by (6).

$$\omega = \left(\sqrt{\delta^2 + 1} - \delta\right) \frac{2}{\Delta T} \quad (6)$$

Based on (6), we can write:

$$L = \frac{(\Delta T \cdot F)^2}{C} \quad (7)$$

$$\text{where } F = \frac{1}{2\left(\sqrt{\delta^2 + 1} - \delta\right)} \quad (8)$$

It may be noted that  $F$  depends only on the selected damping factor  $\zeta$  and it is independent of  $\Delta T$  and the ultimate valve impedances in the “ON” and “OFF” states. Equation 7 provides one of two necessary equations relating selected values of  $L$  and  $C$ .

In the real world, switching losses are always a factor in designing power electronic apparatus. Switching losses are also a factor in selecting the  $L$  and  $C$  values used to represent the “ON” and “OFF” states of the valves. When a valve blocks, it is necessary to provide energy of  $Cv^2$  to charge the capacitor through the resistor  $R$ , where  $v$  is the switched voltage level. This energy is lost when the valve fires and the valve representation is provided by a small inductance. The energy required to charge the inductor is  $Li^2/2$  where  $i$  is the switched current. Close to minimum energy loss for a switching occurs when  $L$  and  $C$  are chosen such that:

$$Cv^2 = \frac{1}{2} Li^2 \quad (9)$$

It may be noted that (7) and (9) give two equations relating  $L$  and  $C$ . Consequently, we can solve for  $L$ ,  $C$  and  $R$  according to (10), (11) and (12).

$$L = \sqrt{2}(\Delta T \cdot F)v/i \quad (10)$$

$$C = \frac{(\Delta T \cdot F)^2}{L} \quad (11)$$

$$R = \frac{2L}{\Delta T} - \frac{\Delta T}{2C} \quad (12)$$

It can be shown that the ratio of the capacitor “OFF” impedance over the inductor “ON” impedance of the valve at any frequency is given by the ratio defined in (13). The ratio would be slightly higher if the resistance  $R$  was considered. When  $f = 60$  Hz;  $\zeta = 0.9$ ; and  $\Delta T = 1.5 \mu\text{sec}$ , (13) gives an OFF/ON impedance ratio of  $2.48 \times 10^6$ .

$$Ratio = \frac{1}{(2\pi f \cdot \Delta T \cdot F)^2} \quad (13)$$

It can also be shown that the inductor “ON” impedance and capacitor “OFF” impedance at any frequency,  $f$ , are given by (14) and (15). If we consider  $v/i$  in (10) to be a base impedance, then for the parameters above, ( $f = 60$  Hz;  $\zeta = 0.9$ ;  $\Delta T = 1.5$   $\mu$ sec),  $X_L = 0.0009$  per unit and  $X_C = 2,227.6$  per unit.

$$X_L = \sqrt{2} \left( \frac{v}{i} \right) (2\pi f \cdot \Delta T \cdot F) \text{ Ohms} \quad (14)$$

$$X_C = \frac{\sqrt{2} \left( \frac{v}{i} \right)}{(2\pi f \cdot \Delta T \cdot F)} \text{ Ohms} \quad (15)$$

A typical range for  $\zeta$  is  $0.85 < \zeta < 1.333$ , with resulting  $F$  of  $1.08 < F < 1.5$ . By way of example,  $\zeta$  was selected as 0.9 and  $\Delta T$  was 1.43  $\mu$ sec in the simulation of a two-level three-phase 60 Hz STATCOM operated with 21 pulse PWM firing. This resulted in switching losses of approximately 3.7 percent on the STATCOM rating. A higher  $\zeta$  increases the value of  $R$ ,  $L$  and  $C$  and results in higher switching losses in the valve representation. Higher switching frequencies will also lead to higher losses.

The  $R$ ,  $L$  and  $C$  values are chosen only according to the above described methods. Due to the lack of freedom in selecting these values, the series  $RC$ , representing the “OFF” state valve, often causes more switching losses than the actual valve snubber. Therefore,  $RC$  snubbers have not been included in parallel with the valve representations in the simulations.

The above equations provide a method for selecting the  $R$ ,  $L$  and  $C$  parameters used in representing a valve. In addition, it has been noted that the simulation is improved if the branch history current injection is set to zero in the first small time-step when a valve is to be switched from the “OFF” state ( $RC$  representation) to the “ON” state ( $L$  representation). The simulation is not improved by blanking the current injection in the first time-step when the valve is to be switched in the opposite direction.

It is possible to set up a normal large time-step EMT simulation in which there are numerical difficulties due to the presence of very large conductances and very small conductances in the same network  $G$  matrix. The use of a time-step which is less than 2  $\mu$ sec, instead of the typical time-step of 50  $\mu$ sec, increases the possibility of having large conductances (associated with capacitors) and small conductances (associated with inductors) in the same matrix. As a result, double-precision computer hardware is recommended when using this algorithm.

### III. HARDWARE IMPLEMENTATION

The digital computing hardware used for solving the VSC bridge simulations is shown in Figure 2.

The GPC card is the computing platform. It contains two (2) IBM 750GX double-precision RISC processors each operating at 1.0 GigaHertz. These processors are preferred because of low latencies (3 or 4 clocks) in the floating point pipeline and low power usage. Either one or both of the processors can be used for a VSC simulation depending on the size of the circuit. When two processors are used, each processor will solve roughly half of the individual component models and create nodal injections for them. Nodal injections that are created on one processor and required on the other processor are sent through the FPGA. Each processor then solves for the node voltages that are needed for the individual component models that are solved on the processor. The required voltage solutions are done using the associated rows of an inverse  $G$  matrix or using  $W$ -matrix techniques, depending on which method produces the shortest execution time for a particular circuit. The FPGA signals the beginning of each small time-step in order to maintain the synchronism of the small time-steps in the two processors.

The GTDI board is a 64-bit digital input board. It samples firing pulses from external controllers every 320 nanoseconds and sends the firing pulses through a 2 GigaHertz fiber-optic

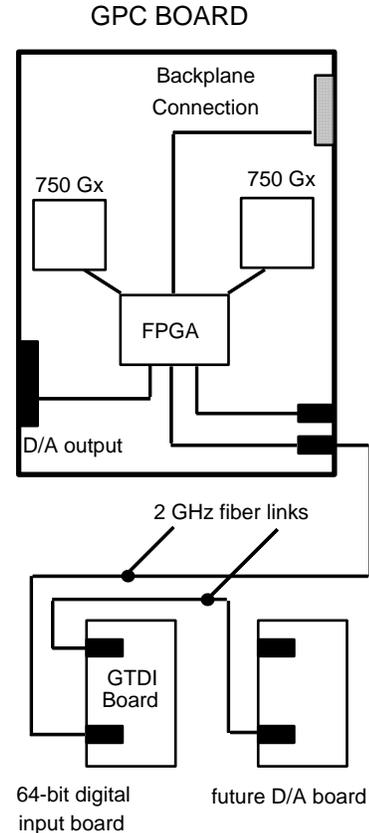


Fig. 2. Hardware Support

link to the FPGA on the GPC board as shown in Figure 2. The FPGA makes the two 32-bit words both available for reading by each of the two processors in each small time-step. Therefore, the latency between a firing pulse occurring and application of it in a simulation is about 2  $\mu\text{sec}$ . The small time-step simulation can update 24 12-bit D/A output ports on the front of each GPC card once in each small time-step. A 16-bit optically-isolated D/A board is planned which will also be updated once in each small time-step. Therefore, the total latency is about 4 to 5  $\mu\text{sec}$  from a new firing pulse being created by an external firing controller to the point where resulting D/A output waves are updated.

In our simulation case described below, we had no external physical controller. Therefore, the controls were modeled in the RTDS simulator on DSP computing boards (3PC card) using the usual RTDS controls modeling capability. Firing pulses were sent out of the digital output port on the back of a 3PC processor with an update interval of about 0.875  $\mu\text{sec}$ . A 3.5 microsecond dead-band was included in the firing for each leg of the bridge. These high-resolution firing pulses were passed by ribbon cable to the GTDI digital input board.

#### IV. DEMONSTRATION SIMULATION

The simulated circuit is shown in Figure 3. The simulated circuit is basically that illustrated in Figure. 1 of a paper by R.

Pena, J.C. Clare and G.M. Asher [5] relating to a “Doubly fed induction generator using back-to-back PWM converters and its application to variable-speed wind-energy generation”. However, instead of driving the VSC circuit from essentially an infinite bus, the VSC circuit in our simulation is interfaced to a large time-step simulation through an interface transformer. A high-pass filter, rated at 0.1 P.U. MVA and tuned to the 21 pulse PWM rate, is also included in the simulated apparatus.

The rotor q-axis current order,  $i_{rq}^*$ , controls the electrical torque which the induction machine will produce. Positive  $i_{rq}^*$  corresponds with positive electrical torque which corresponds to generation of power into the electrical system. In Figure 3, the  $i_{rq}^*$  order is shown as originating in the optimal power controller. However, the  $i_{rq}^*$  order could also be provided through a slider in the RTDS RunTime environment. Figure 4 shows the response of electrical torque to a step change in  $i_{rq}^*$  order from 0.0 p.u. to 1.414 p.u. which essentially provides a change in electrical torque order from 0.0 to 1.0 per unit. Figure 5 illustrates corresponding plots of the rotor currents. Prior to the change in  $i_{rq}^*$  order, the  $i_{rd}^*$  order was 1.0 p.u. which corresponds to 0.707 p.u. reactive excitation provided from the rotor side. The machine speed at the time was 1.2 per unit.

For validation purposes, an EMTDC simulation (version 1.41.1) of the circuit was also run with a 50 microsecond

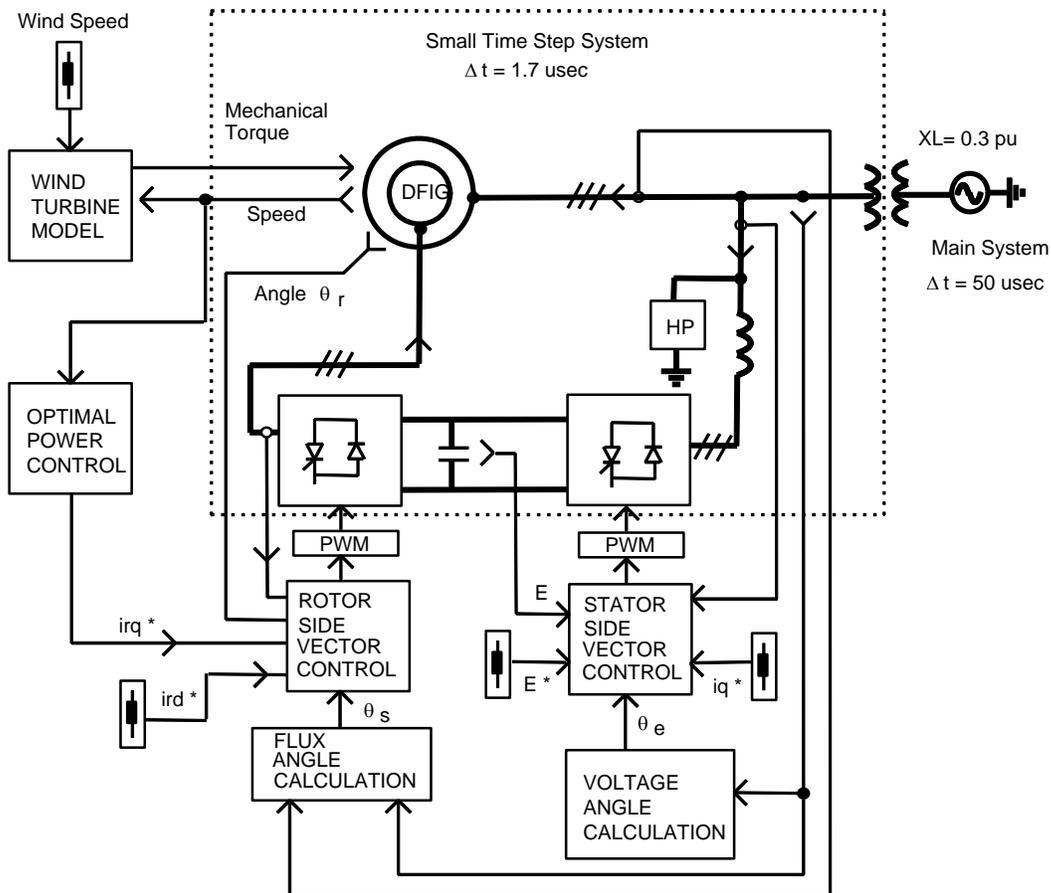


Fig. 3. Schematic of Simulated System

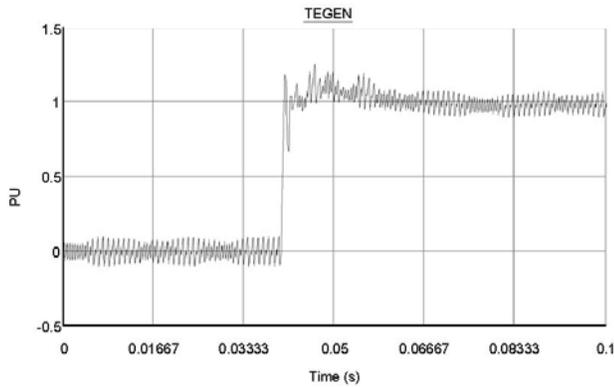


Fig. 4. RTDS - Machine Electrical Torque vs Time

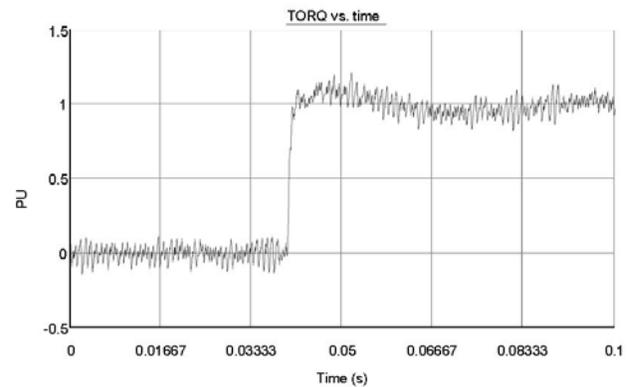


Fig. 6. EMTDC - Machine Electrical Torque vs Time

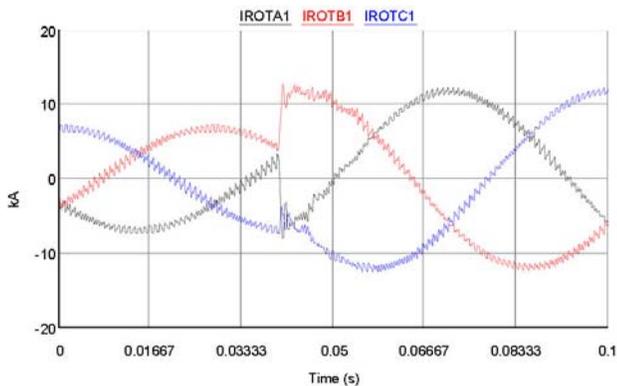


Fig. 5. RTDS - Machine Rotor Currents vs Time

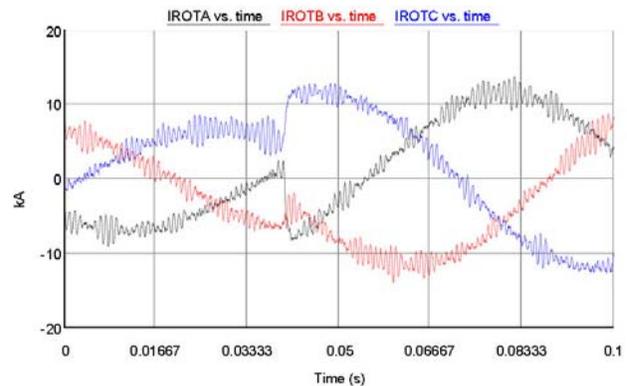


Fig. 7. EMTDC - Machine Rotor Currents vs Time

time-step and interpolation enabled. The same torque order change, described above for the RTDS simulation, was applied in the EMTDC simulation. The rotor currents and torque from the EMTDC simulation are shown in Figures 6 and 7. The basic magnitudes and dynamics of the waveshapes in the EMTDC simulation match those in the RTDS simulation. However, we could only eliminate the noise from the EMTDC simulation by reducing the time-step down from 50  $\mu\text{sec}$ .

Execution time in the small time-step VSC code is kept to a minimum by linking pre-created modules of machine code during the circuit compiling process. It is useful to know the execution times of various modules in order to judge what can be done in real-time simulation. Therefore, at this point, the execution times of various modules are presented. The simulated circuit contains a double-fed induction machine (DFIG) in the small time-step area. This model includes saturation and requires approximately 0.40  $\mu\text{sec}$  of execution time per time-step. Each of the six-valve two-level bridges requires approximately 0.22  $\mu\text{sec}$  of execution time. The three-phase high-pass filter bank requires approximately 0.09  $\mu\text{sec}$ . The three-phase RL branch requires about 0.05  $\mu\text{sec}$ . The capacitor branch requires about 0.025  $\mu\text{sec}$ . The three-phase interface transformer requires about 0.11  $\mu\text{sec}$ . The network solution requires approximately 0.2  $\mu\text{sec}$  on each processor. The overall VSC circuit including the machine is

simulated in real-time with a small time-step of 1.67  $\mu\text{sec}$ . These execution times should make it possible, in the absence of machine models, to simulate 36 switched devices in one lumped connected circuit in real-time. We have modeled a three-phase three-level bridge using this method of representing switches. However, we do not yet have controls arranged for a back-to-back three-level DC link and therefore verification of the 36 valve capability is left for future work.

## V. CONCLUSIONS

The paper has described a method for picking R, L and C parameters of fixed-conductance valve models applied in short time-step EMT simulation of power-level VSC bridges. The practicality of conducting real-time VSC simulations using the described valve models has been demonstrated through the development of supporting hardware and the conduct of a typical real-time VSC simulation.

It is expected that the described method of modeling VSC bridges will greatly reduce the time and expense presently expended in making analog models of power-level VSC bridges for testing physical controllers.

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## VII. BIOGRAPHIES



**Trevor Maguire** (M'1986, SM'2004) was born in Manitoba, Canada. He graduated from the University of Manitoba with B.Sc.EE, M.Sc.EE and Ph.D. degrees in 1975, 1986, and 1992 respectively.

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