Small Time-step (< 2µSec) VSC Machine Drives for the Real Time Digital Simulator

Trevor Maguire Paul Forsyth Rick Kuffel

Abstract: This paper describes a recently developed approach for representing Voltage Source Converter (VSC) bridges using real time electromagnetic transient (EMT) simulators. The fact that such simulators must provide continuous real time response introduces numerous challenges normally not faced in typical off-line EMT simulations.

The method presented in this paper utilizes a multiple time step approach in which time critical components are simulated with a small time step (< 2 µsec) while the remainder of the circuit is simulated with more typical time step (~ 50 µsec). The VSC bridge, which can include many valves within a single lumped circuit is interfaced to the time-domain simulation of the main network.

In an EMT simulation program, the representation of a valve is achieved by the combination of a conductance in parallel with a controlled current source. For the method described in this paper the ON and OFF states of any valve are achieved by modification of the current injection coming from the controlled source rather than changing the conductance value.

Keywords: Voltage Source Converter, VSC, electromagnetic transient simulation, real time simulation

I. Introduction

Over the past decade much development has taken place in the field of real time digital simulation. Already real time digital simulators have become powerful tools for power system engineers in areas such as closed-loop relay testing, control system development and testing, HVDC and FACTS research, and in more general system performance studies. Modeling of voltage source converters (VSC) in real-time digital simulators presents unique challenges that are not normally faced in off-line, non real time simulation programs. When simulating machine drives for example, it is often necessary to include VSC bridges which are best simulated using very small time steps in order to provide adequate firing resolution. Furthermore, the VSC bridge is often connected to a large network containing many transmission lines, transformers, generators, buses, etc. Which would be best simulated using a time step in the range of In order to simulate the overall network without using an overly large amount of real-time hardware.

In non-real-time EMT simulation programs, interpolation within the time-step is used to provide the firing resolution required by VSC models. Whenever switching occurs within a timestep, the EMT program decomposes the network matrix according to the new switching state and proceeds from the point of interpolation. If several valves switch at different points during a single timestep, it is then necessary to decompose the network matrix several times during that interval. The occurrence of multiple decompositions per timestep can be expected because the turn-on of a valve often leads to the turn-off of others. Off-line non-real time EMT programs can handle this without difficulty, but execution time is extended (i.e. slowed down).

In real-time EMT simulation, it is not a practical option to interpolate and decompose the main network matrix several times during a single time-step. The difficulty becomes clear when considering the effect of a switching point that occurs very late in the time-step. There may not be enough time to complete the interpolation and decomposition before real time requires that the simulation move to the next time-step. Therefore, interpolation as a general method has limitations when applied to real time simulation.

This paper explores a new approach in VSC modelling implemented for the RTDS® simulator. The technique builds on past efforts, primarily by Hui and Christopoulos, to develop methods for fast time-domain simulation of switching networks [1]. The main advantage of the Hui and Christopoulos algorithm for real time simulation is that decomposition, or inversion, of the Dommel network conductance matrix [2] is not required during a simulation. The same Dommel branch conductance represents the valve in the "ON" state and the "OFF" state. The difference in state is completely represented by the Dommel history current injection. With this approach, the reduction in computational load allows the real time simulation of VSC bridges to be conducted with time-steps less than two (2) µsec.

II. VSC Representation

Various approaches have been applied in order to try to make interpolation work adequately for real-time simulation. One approach has been to isolate the VSC bridges into sub-networks which are interfaced into the main network. With this approach, interpolation and decomposition become operations that are isolated in the sub-network. However, unless the

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number of valves in the VSC sub-network is small, multiple interpolations within a time-step of the sub-network can defeat real-time operation. Decomposition can be avoided in a VSC sub-network by pre-inverting and storing a matrix for each combination of switch states for the N switches. However, the need to store 2^N pre-inverted matrices also places a fairly low limit on the number of switches, N. The limitations of the interpolation algorithm have made it necessary to seek alternative algorithms for VSC sub-network solution.

Fortunately, there have been efforts in the past, primarily by Hui and Christopoulos, to develop methods for fast time-domain simulation of networks with switches [1]. The advantage of these methods is that decomposition or inversion of the Dommel network conductance matrix during a simulation is not required because the same Dommel branch conductance represents the valve in the "ON" state and the "OFF" state. In the "OFF" state, the valve is represented as a series RC branch with Dommel resistance of $R_b = R_{RC} = R + \Delta T/2C$ Ohms. In the "ON" state, the valve is represented as an inductor with $R_b = R_L = 2L/\Delta T$. Figure 1 illustrates the branch configurations for the ON and OFF states respectively.

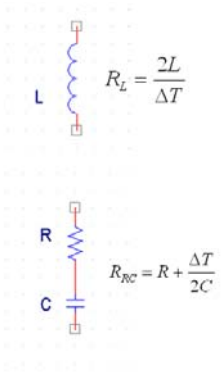

Fig. 1. Valve Representation

In order to avoid the need for matrix decomposition, the algorithm requires that $R_L = R_{RC}$ (i.e. $R + \Delta T/2C = 2L/\Delta T$). In order to get a high-impedance RC branch and a low-impedance L branch from the same branch resistance Rb, it is necessary that the time-step ΔT must be quite short. In fact, the time-step must be less than about two microseconds to obtain an impedance ratio in excess of 1.0e6 between the "ON" and "OFF" states. The difference between an "ON" valve and an "OFF" valve is completely represented in the small time step solution algorithm by the Dommel history current injection parallel to the Dommel conductance

The desirability of a damping resistance, R, in series with the capacitance representation is mentioned by Pejovic and Maksimovic [3]. However, little guidance is provided as to selection of the R, L and C values illustrated in Figure 1. Of course, it is required that the selected values ensure $R_L = R_{RC}$. Recent work [4] to be published later this year reveals that appropriate values for L, C and R can be found using Equations (1), (2) and (3) below:

$$L = \sqrt{2}(\Delta T \cdot F)v/i \quad (1)$$

$$C = (\Delta T \cdot F)^2 / L \quad (2)$$

$$R = \frac{2L}{\Delta T} - \frac{\Delta T}{2C} \quad (3)$$

where $$F = \frac{1}{2\left(\sqrt{\delta^2 + 1} - \delta\right)}$$

v = switched voltage
i = switched current
δ = damping factor

The approach described above does not remove the need to create an interface between the main network solution, which runs at approximately 50 μsec and the VSC sub-network which runs at approximately 2 μsec. Fortunately, the basic concept can be drawn from early work on interfacing digital simulators with analog equipment [5] as illustrated in the top of Figure 2. Interfacing to a short time-step VSC sub-network is very much like interfacing to an analog model. The similarity can be seen clearly by comparing the top of Figure 2 with the bottom. However, the digital-to-digital interface eliminates the D/As, amplifiers, current transducers and A/Ds normally needed in the digital-to-analog interface. Eliminating these components reduces the closed-loop interface delay and makes the digital-to-digital interface more accurate and stable.

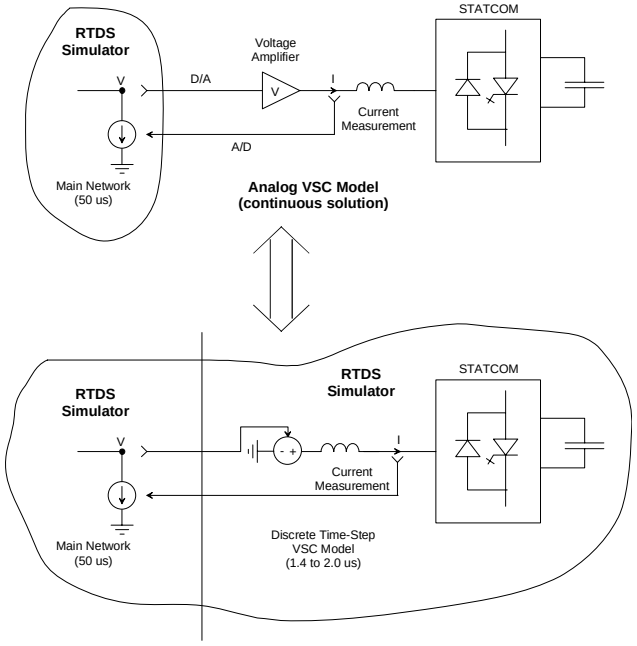

Fig. 2. VSC Interface to Main Network Solution

III. Real time Hardware Implementation

An advanced processing card has recently been developed and introduced by RTDS Technologies for simulation of very complex devices including VSC bridges. The so-called Giga-Processing Card (GPC) contains two (2) IBM 750GX double-precision RISC processors each operating at 1.0 GHz. These processors are preferred because of low latencies (3 or 4 clock cycles) in the floating point pipeline and low power usage. Figure 3 shows the GPC card.

Fig. 3. The GPC Card

Either one or both of the processors on the GPC can be used for a VSC simulation depending on the size and configuration of the circuit. When two processors are used, each processor will solve approximately half of the individual component and create nodal injections for each. The nodal injections for computing voltages that are created on one processor and required on the other processor are sent through an on-board FPGA. The FPGA also signals the beginning of each small time-step in order to maintain the synchronism of the small time-steps in the two GPC processors.

Figure 4 shows a real time oscilloscope recording of node voltage VLOADA from the simulation of the 3-level bridge illustrated in Figure 5.

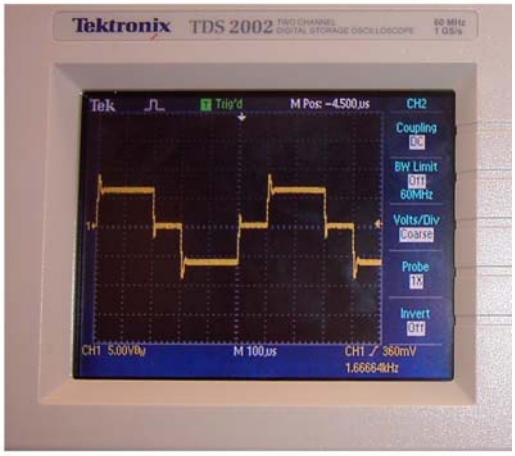

Fig. 4. Three-Level Bridge Voltage Waveform

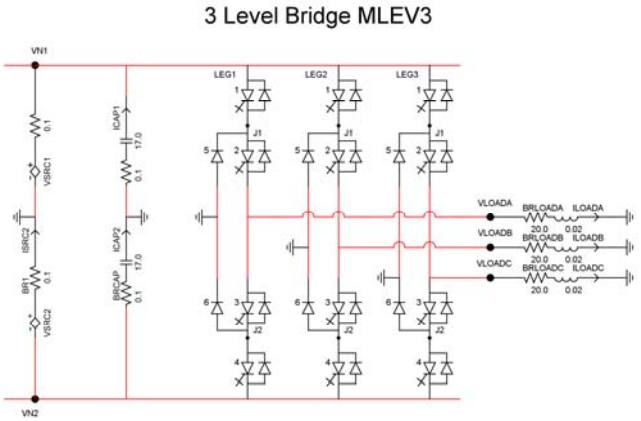

Fig. 5. Three-Level Bridge Circuit

In practical applications it may be necessary to interconnect the simulated VSC bridge(s) to external control systems. In order facilitate the interconnection of physical controls the GPC card has been designed to work together with several specialized I/O components.

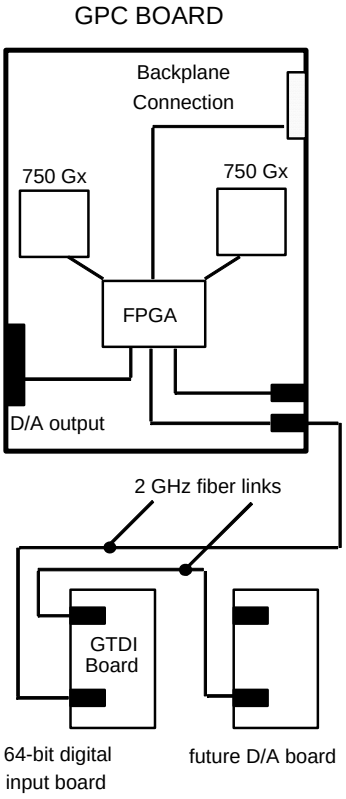

Fig. 6. Hardware Interface

The GTDI board is a 64-bit digital input board. It samples firing pulses from external controllers every 320 nanoseconds and sends the firing pulses through a 2 GHz fiber-optic link to the FPGA on the GPC board as shown in Figure 6. The FPGA makes all 64 bits available for reading by either of the two processors in each small time-step. Therefore, the latency between a firing pulse occurring and application of that firing

pulse in a simulation is less than 2 μsec.

The small time-step simulation can also update twenty four 12-bit D/A output ports on the front of each GPC card once in each small time-step. A twelve channel, 16-bit optically-isolated D/A board is currently under development which will also be updated once in each small time-step. Therefore, the total latency is about 4 microseconds from a new firing pulse being created by an external firing controller to the point where resulting D/A output waves are updated.

In the simulation case described below, there was no external physical controller available. The controls were therefore modeled internally within the RTDS simulator on separate DSP computing boards (3PC card) using the usual RTDS controls modeling capability. Firing pulses were sent out of the digital output port on the back of a 3PC processor with an update interval of about 0.875 μsec. These high-resolution firing pulses were passed by ribbon cable to the GTDI digital input board.

IV. Demonstration Simulation

The simulated circuit is shown in Fig. 7. The simulated circuit is basically that illustrated in Fig. 1 of a paper by R. Pena, J.C. Clare and G.M. Asher [6] relating to a "Doubly fed induction generator using back-to-back PWM converters and its application to variable-speed wind-energy generation". However, instead of driving the VSC circuit from essentially an infinite bus, the VSC circuit in the demonstration case is interfaced to a large time-step simulation through an interface transformer. A high-pass filter, rated at 0.1 P.U. MVA and tuned to the 21 pulse PWM rate, is also included in the simulated apparatus.

The rotor q-axis current order, irq*, controls the electrical torque which the induction machine will produce. Positive irq* corresponds with positive electrical torque which corresponds to generation of power into the electrical system. In Figure 7, the irq* order is shown as originating in the optimal power controller. However, the irq* order could also be provided

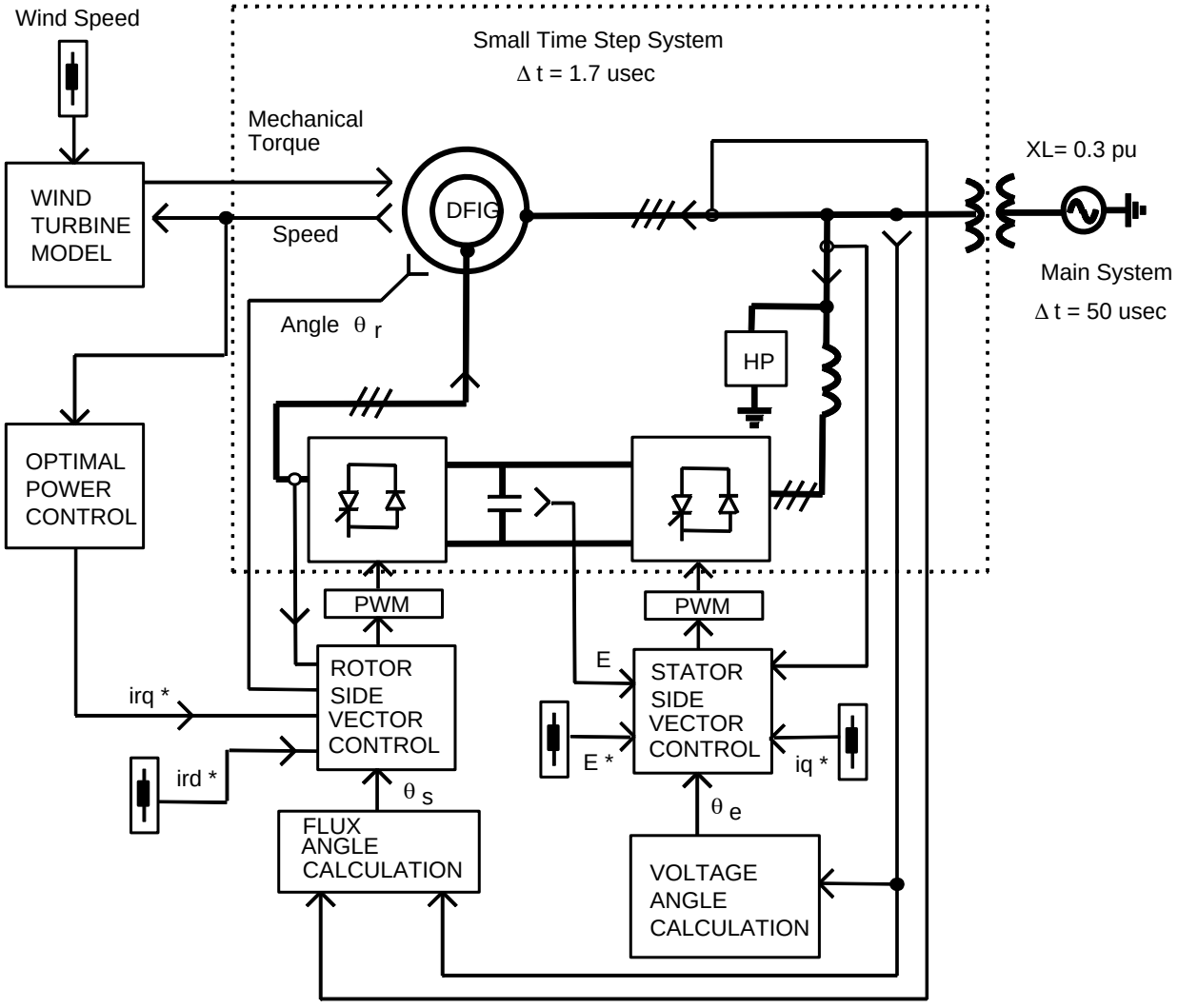

Fig. 7. Schematic of Simulated System

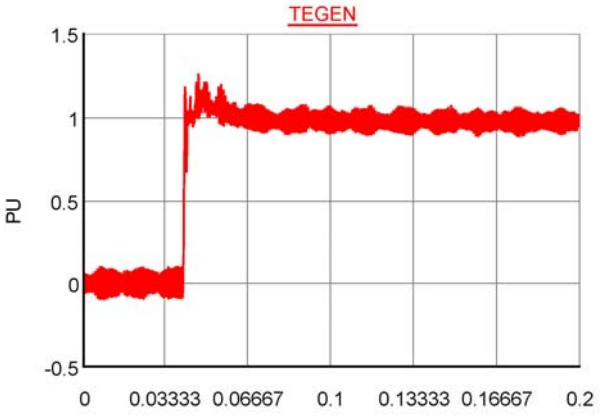

Fig. 8. Machine Electrical Torque vs Time

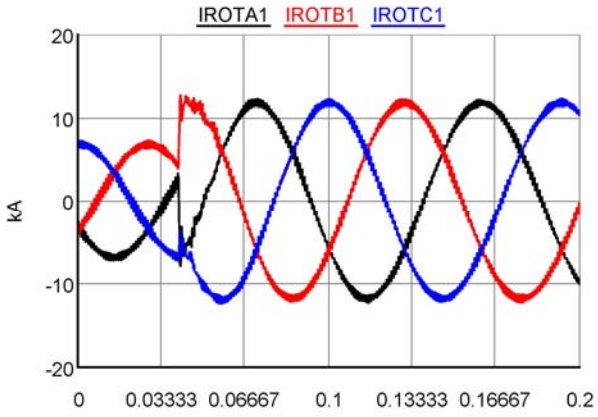

Fig. 9. Machine Rotor Currents vs Time

through a slider in the RTDS RunTime environment. Figure 8 shows the response of electrical torque to a step change in irq* order from 0.0 p.u. to 1.414 p.u. which essentially provides a change in electrical torque order from 0.0 to 1.0 per unit. Figure 9 illustrates corresponding plots of the rotor currents. Prior to the change in irq* order, the ird* order was 1.0 p.u. which corresponds to 0.707 p.u. reactive excitation provided from the rotor side. The machine speed at the time was 1.2 per unit.

Execution time in the small time-step VSC code is kept to a minimum by linking pre-created modules of machine code during the circuit compiling process. It is useful to know the execution times of various modules in order to judge what can be done in real-time simulation. Therefore, at this point, the execution times of various modules are presented. The simulated circuit contains a double-fed induction machine (DFIG) in the small time-step area. This model includes saturation and requires approximately 0.40 µsec of execution time per time-step. Each of the six-valve two-level bridges requires approximately 0.22 µsec of execution time. The three-phase high-pass filter bank requires approximately 0.09 µsec. The three-phase RL branch requires about 0.05 µsec. The capacitor branch requires about 0.025 µsec. The three-phase interface transformer requires about 0.11 µsec. The network solution requires approximately 0.2 µsec on each processor. The overall VSC circuit including the machine is simulated in real-time with a small time-step of 1.67 µsec. These execution times should make it possible, in the absence of machine models, to simulate 36 switched devices in one lumped connected circuit in real-time. However, we do not yet have controls arranged for a back-to-back three-level DC link and therefore verification of the 36 valve capability is left for future work.

V. Conclusions

The paper has described a method for picking R, L and C parameters of fixed-conductance valve models applied in short time-step EMT simulation of power-level VSC bridges. The practicality of conducting real-time VSC simulations using the described valve models has been demonstrated through the development of supporting hardware and the conduct of a typical real-time VSC simulation.

It is expected that the described method of modeling VSC bridges will greatly reduce the time and expense presently expended in making analog models of power-level VSC bridges for testing physical controllers.

VI. References

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VII. BIOGRAPHIES

Trevor Maguire graduated from the University of Manitoba with B.Sc.EE, M.Sc.EE and Ph.D. degrees in 1975, 1986, and 1992 respectively.

Relevant employment experience includes time with Manitoba Hydro (1975-76), Manitoba HVDC Research Centre (1986-1994), and RTDS Technologies, Inc. (1994-present). He is a founding principal of RTDS Technologies, Inc. with a special interest in real-time simulation model development and also real-time simulation digital hardware development. He participated in creating the world's first commercial real time digital power system simulator.

Paul Forsyth graduated from the University of Manitoba with B.Sc.EE in 1988. After graduating he worked for several years in the area of reactive power compensation and HVDC at ABB Power Systems in Switzerland. He also worked for Haefely-Trench in both Germany and Switzerland before returning to Canada in 1995. Since this time he has been employed by RTDS Technologies where he currently holds the title of Marketing Manager / Simulator Specialist.

Rick Kuffel graduated from the University of Manitoba with B.Sc. EE and M.Sc.EE in 1984 and 1986 respectively. After graduating he worked at BBC in Switzerland and Teshmont Consultants in Winnipeg before moving to the Manitoba HVDC Research Centre in 1989. There he worked mainly on the development of the real time simulator and in 1994 became a founding principal of RTDS Technologies.