

REAL TIME DIGITAL SIMULATION



RTDS® Southern Africa Users' Group Meeting

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Real-Time Simulations Using a Synchrophasor-Based Wide Area Monitoring, Protection, and Control (WAMPAC) Testbed

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- Background
- Objectives
- Methodology
- Experimental Results
- Conclusion
- Bibliography



- **Background**
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Power System Operations

- Provide reliable supply of electricity
- Efficient and secure operation

■ Current trend

- Large/complex interconnections
- Loads continue to increase
- Long distance between gens. & loads
- Lack of new power stations

■ Implications

- Power systems are stressed
- Systems are operating closer to their stability limit



■ Power System Stability

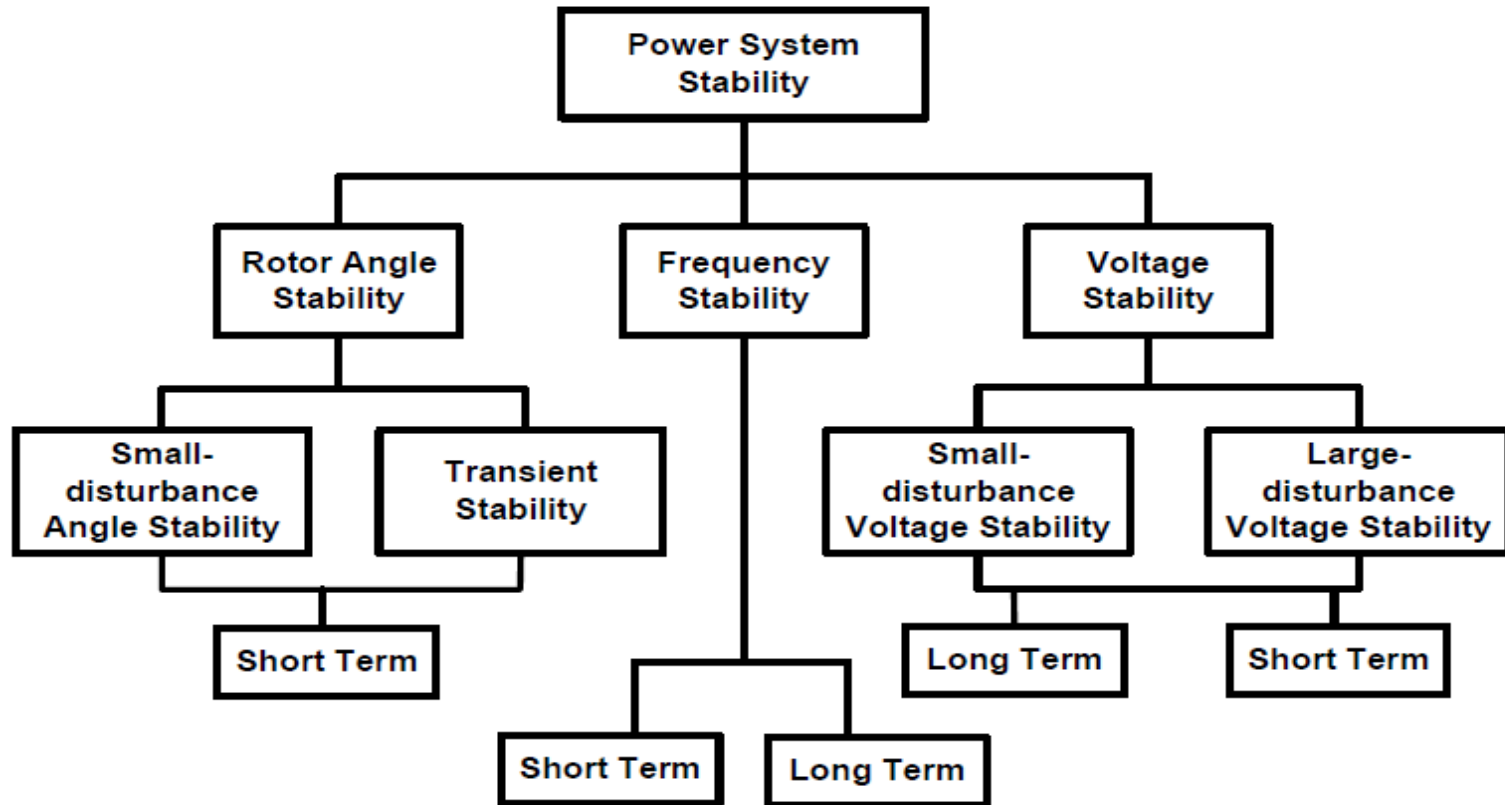


Figure 1: Power system stability (Kundur, 1994)

Voltage Stability Assessment (VSA)

Ability to maintain acceptable voltage profile during steady state conditions & after a disturbance

Causes of voltage instability:

- Small disturbances: Gradual increase in system loading
- Large disturbances: Loss of lines/generators, faults, transformer and generator controls (OLTCs/OXLs)
 - Lack of reactive power support
 - Loss of voltage control



Analysis:

- The proximity of the system to voltage collapse
- Mechanism of voltage collapse (how?, why?, what, where the voltage weak areas are? effective RAS.

System Integrity Protection Schemes for VSA (RAS, SPS, SIPS)

Functions

- Monitor
- Detect abnormal system conditions
- Initiate remedial action(s)
- Preserve system integrity

SIPS Elements

- System monitoring element
- System protection element
- Execution element

System Integrity Protection Schemes for VSA (RAS, SPS, SIPS)

Table 1: Remedial actions for power system instability

SIPS/RAS/SPS	Transient instability	Small-signal instability	Frequency instability	Voltage instability
Generation rejection	×	×	×	×
Remote load shedding	×	×		
HVDC controls	×	×	×	
Braking resistor	×	×		
Under-frequency load shedding			×	
Turbine fast valving	×	×	×	
Automatic shunt switching	×	×		×
Under-voltage load shedding				×
Tap-changer blocking			×	×
AGC controls		×		×
Gas turbine start-up			×	×

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OBJECTIVES

Proposed algorithms and methods for WAMPAC

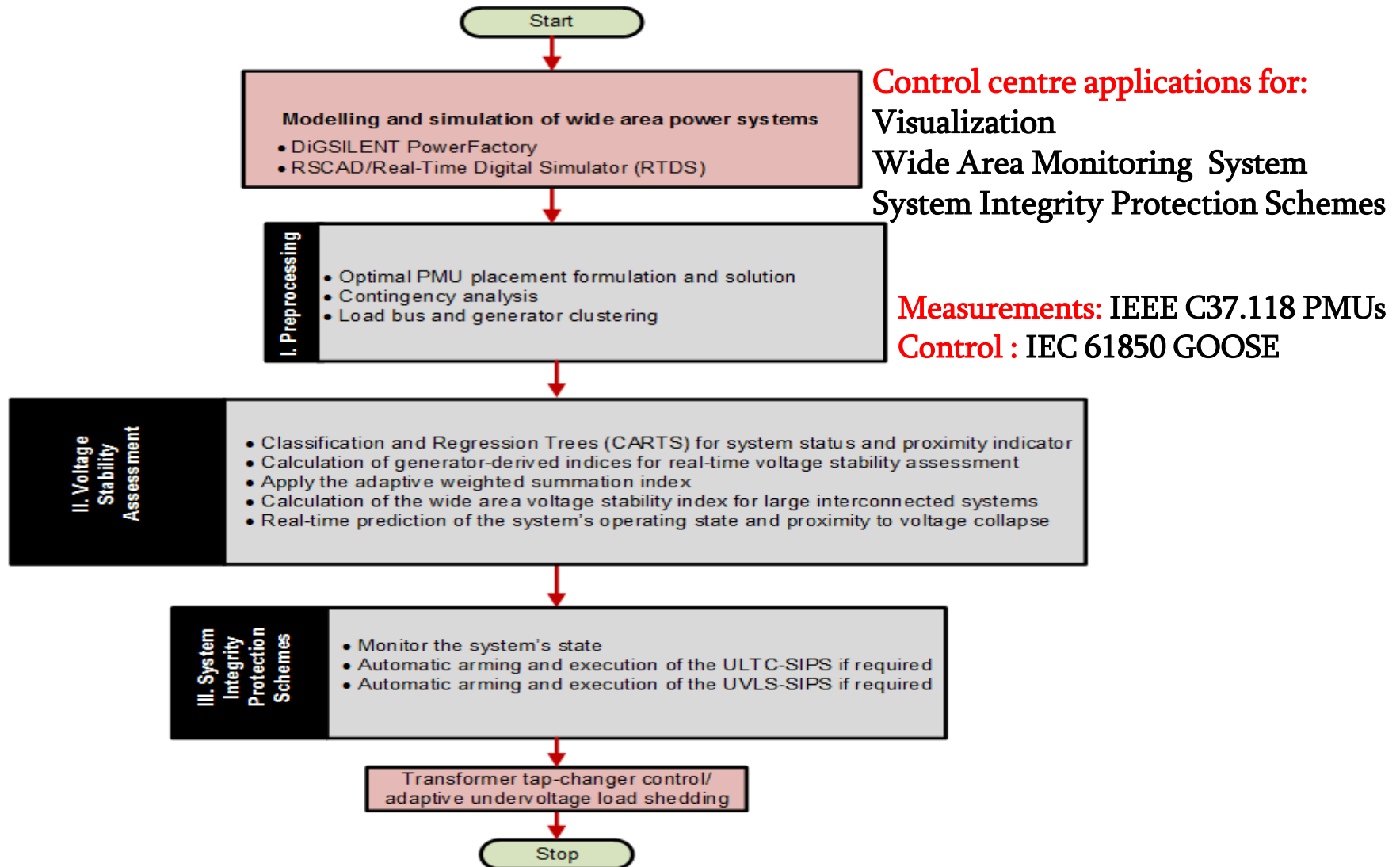
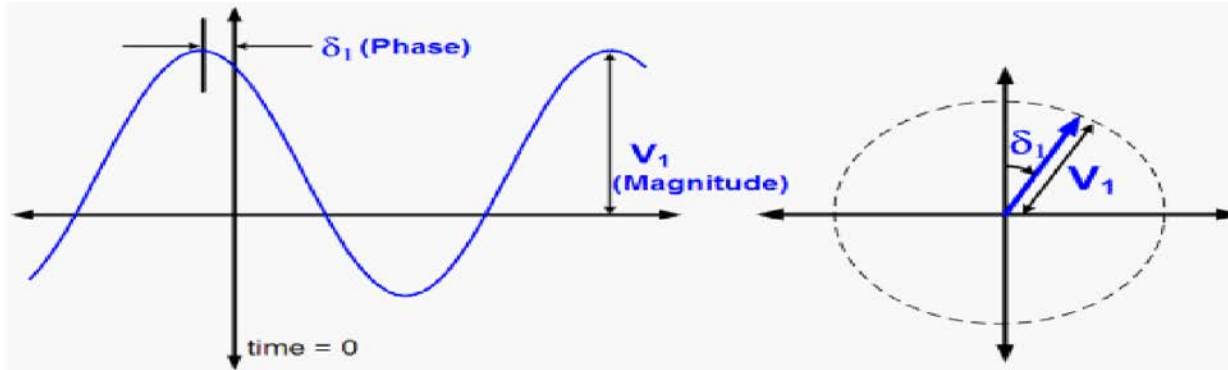


Figure 2: Proposed methods and algorithms for Wide Area Monitoring, Protection, and Control (WAMPAC) © 2016 Adewole, Adeyemi Charles All Rights Reserved

■ What are synchrophasors?



Voltage phasors
Current phasors
Sequence components
Frequency
ROCOF
Analogue measurements
Digital statuses



Features

- 1 μ s synchronization to the GPS,
- Reporting rates up to 200 fps for 50 Hz systems
- Accuracy of 1% TVE
- Compliance with IEEE C37.118 Std.

OBJECTIVES



Applications of synchrophasors

- Situational awareness
- Wide area monitoring systems
- Linear state estimation,
- Decision support
- Real-time analysis
- Protection and control
- Model validation

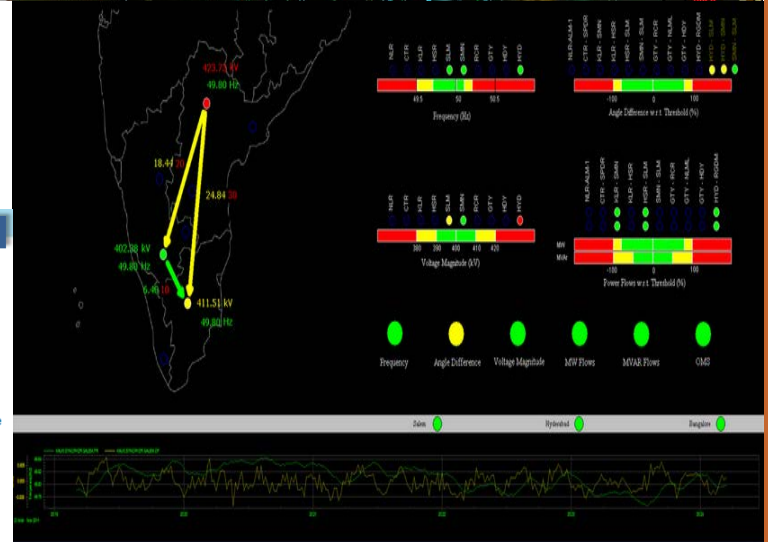
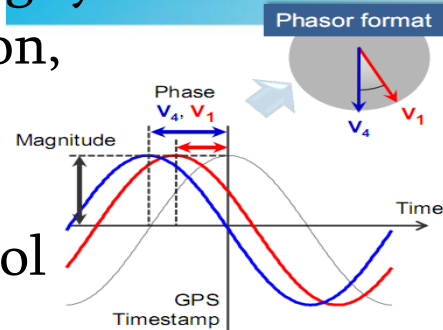


Table 2: Comparison with existing technology

Existing Technology	Emerging Technology
SCADA Data	Phasor Measurement -PMU
Refresh rate = 2-10 seconds	Refresh rate = 200 samples per second (50 Hz)
Magnitude only	Magnitude & phase angle
Measurements are not time synchronized	Measurements are time synchronized
Legacy communication technology	Modern communication technology
Not suitable for rapidly changing system conditions	Suitable for capturing dynamic changes
X-ray	MRI

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- Derivations of real-time voltage stability indices
 - Generator reactive power reserve
- Derivation for centralized SIPS (undervoltage load shedding scheme)
 - MVAR mismatch, Voltage Control Areas (VCA), volt deviation
- Development of a 'proof-of-concept' testbed
- Modelling of the test system
 - New England 39-bus test system
- Real-time hardware-in-the-loop simulations of case studies
 - Case studies: Load increase, generator contingencies, line contingencies

Proposed Real-Time Voltage Stability Indices (RVSA) indices

- Derivation from generator maximum reactive power reserve

$$Q_{g \max} = -\frac{V_g^2}{X_s} + \sqrt{\frac{V_g^2 I_{fd \max}^2}{X_s^2} - P_{g \max}^2} \quad RVSA_{Q,i} = \left(1 - \frac{Q_{gki}}{Q_{g \max i}^c} \right) \times 100\% \quad (1)$$

- Generator field current derivation from $Q_{g \max}$

$$-\frac{V_g^2}{X_s} + \sqrt{\frac{V_g^2 I_{fd \max}^2}{X_s^2} - P_{g \max}^2} = -\frac{V_g^2}{X_s} + \sqrt{\frac{V_g^2 I_{fdk}^2}{X_s^2} - P_{gk}^2} \quad RVSA_{Ifd,i} = \left(1 - \frac{I_{fdki}}{I_{fd \max i}^c} \right) \times 100\% \quad (2)$$

- Generator stator current derivation

$$Q_{ga \max} = \sqrt{V_g^2 I_{a \max}^2 - P_{ga \max}^2} \quad RVSA_{Ia,i} = \left(1 - \frac{I_{aki}}{I_{a \max i}^c} \right) \times 100\% \quad (3)$$

Proposed RVSA indices for large interconnected power system

- Reactive power reserve on system generators

$$RVSA_{Q,sys} = \min_{i \in sys} \{ RVSA_{Q,i} \} = \min_{i \in sys} \left\{ \left(1 - \frac{Q_{gki}}{Q_{g \max i}^c} \right) \times 100\% \right\} \quad (4)$$

- Field current reserves on system generators

$$RVSA_{Ifd,sys} = \min_{i \in sys} \{ RVSA_{Ifd,i} \} = \min_{i \in sys} \left\{ \left(1 - \frac{I_{fdki}}{I_{fd \max i}^c} \right) \times 100\% \right\} \quad (5)$$

- Stator current reserves on system generators

$$RVSA_{Ia,sys} = \min_{i \in sys} \{ RVSA_{Ia,i} \} = \min_{i \in sys} \left\{ \left(1 - \frac{I_{aki}}{I_{a \max i}^c} \right) \times 100\% \right\} \quad (6)$$

Derivations for undervoltage load shedding scheme

- Total reactive power mismatch

$$\Delta Q_{gik} = Q_{gik} - Q_{gi0}, \quad i = \overline{1, N_g}, \quad k = 0, 1, 2, \dots \quad (7)$$

- Total load to shed

$$Q_{shed,k} = \beta_K \cdot \sum_{i=1}^{N_g} \Delta Q_{gik}, \quad k = 0, 1, 2, \dots \quad (8)$$

- Total load to shed per VCA

$$\Delta Q_{shed,VCAjk} = \left(\frac{100 - vcaRVSA_{jk}}{100n - \left(\sum_{j=1}^n vcaRVSA_{jk} \right)} \right) \times Q_{shed,k} \quad j = \overline{1, n}, \quad k = 0, 1, 2, \dots \quad (9)$$

- Total load to shed per VCA per load bus

$$\Delta Q_{shed,jBp} = W_j \Delta VB_p \times \Delta Q_{shed,VCAjk} \quad (10)$$

SIPS elements for undervoltage load shedding

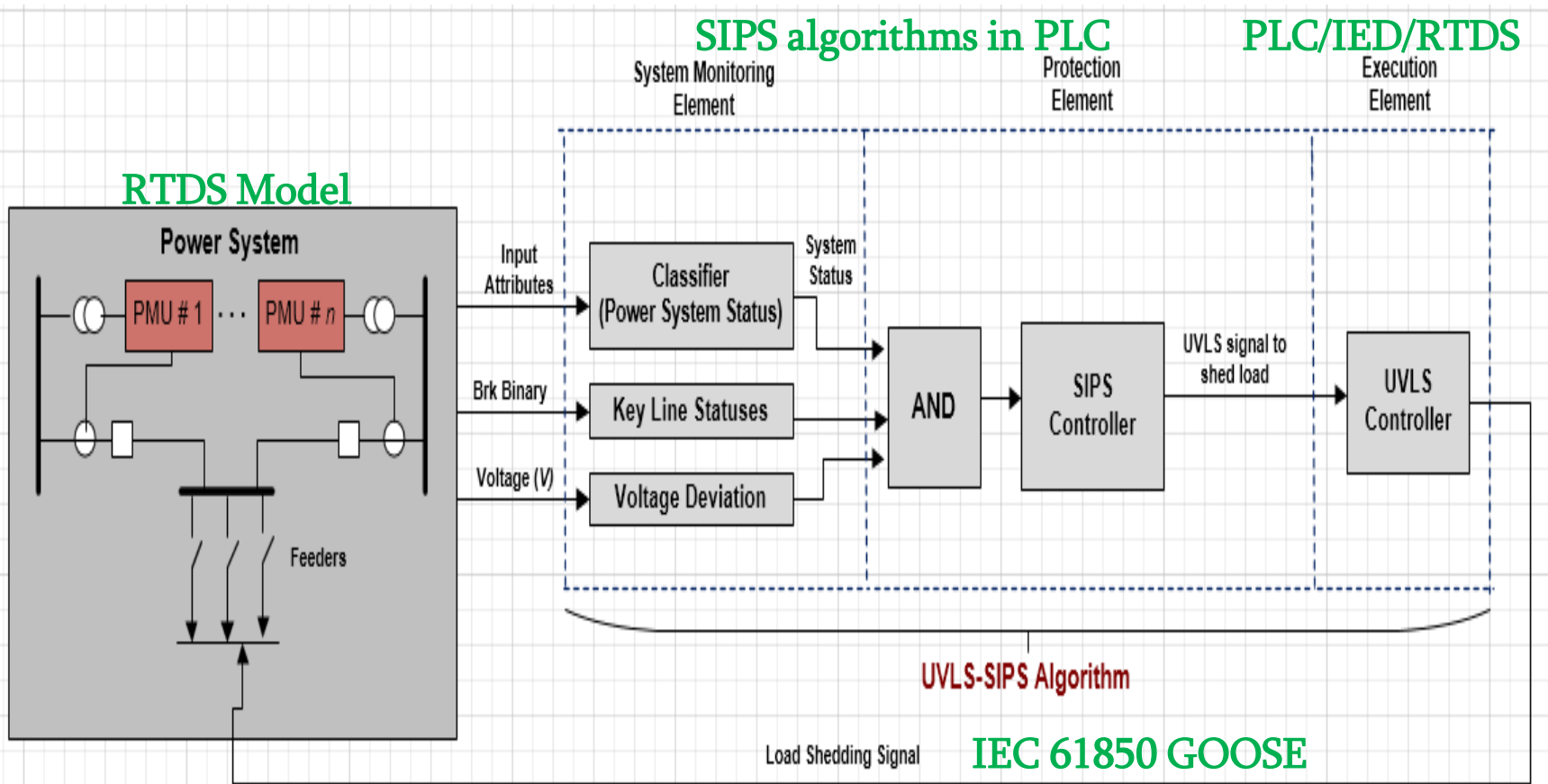


Figure 3: System Integrity Protection Scheme (SIPS)

METHODOLOGY

Testbed used at CSAEMS-CPUT

- RTDS, PMUs, PDCs, IEDs, GPS Clocks, PLC, Network Switches



Figure 4: Implemented WAMPAC testbed

Table 3: RTDS Resources at CPUT (4 Racks)

S/N	RTDS Card	Function	Nr.
1	PB5	Processor card	6
2	GPC	Processor card	3
3	GTWIF	Work station interface	4
4	GTNET	Communication protocols (PMU, GSE, SV, DNP3)	5
5	GTNET X2	Communication protocol X2 (GSE, SKT)	1
6	GYSYNC	Time synchronization	2
7	GTAO	Analogue output card	2
8	GTAI	Analogue input card	1

Test System Model

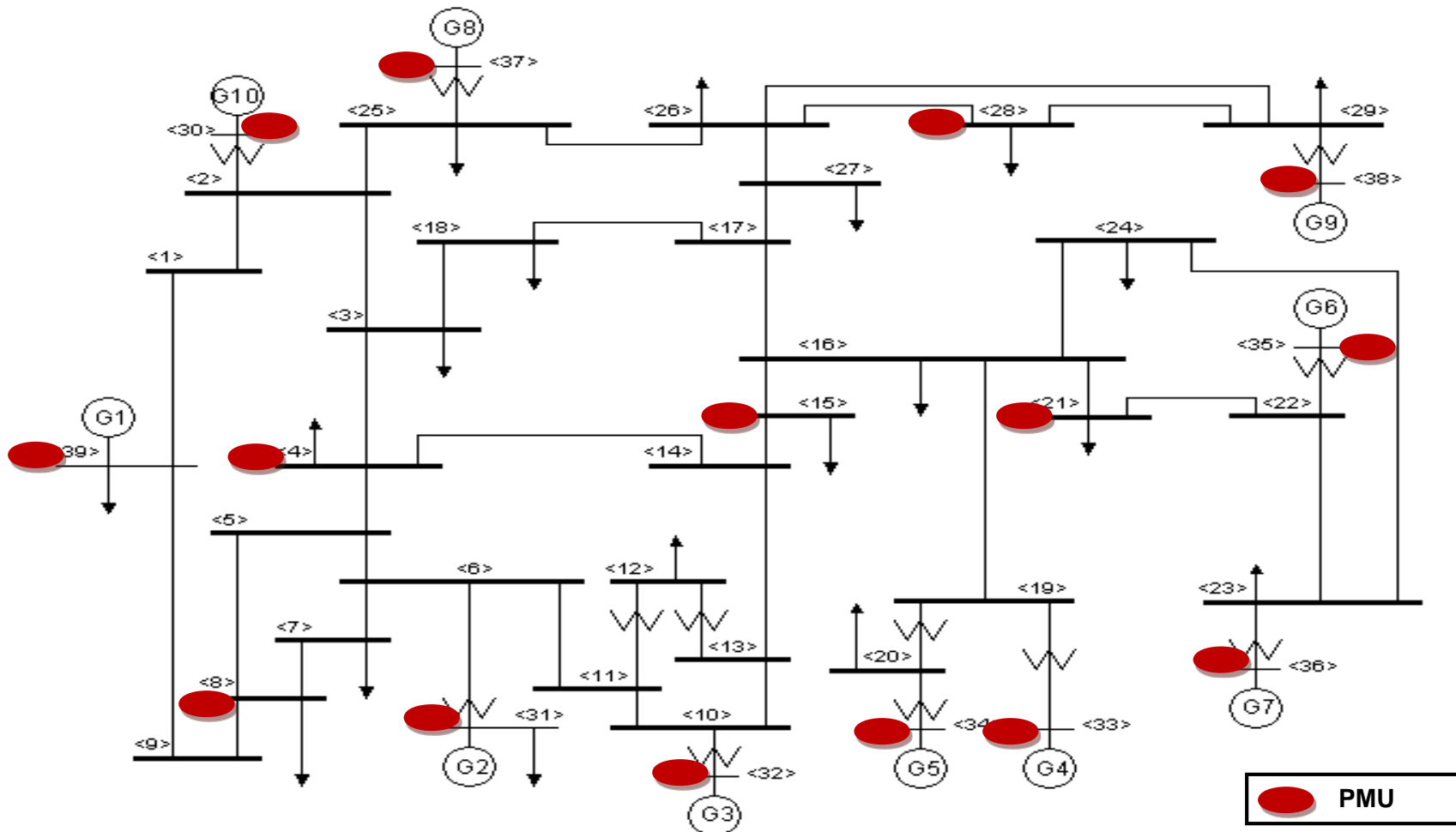


Figure 5: New England 39-bus test system

METHODOLOGY

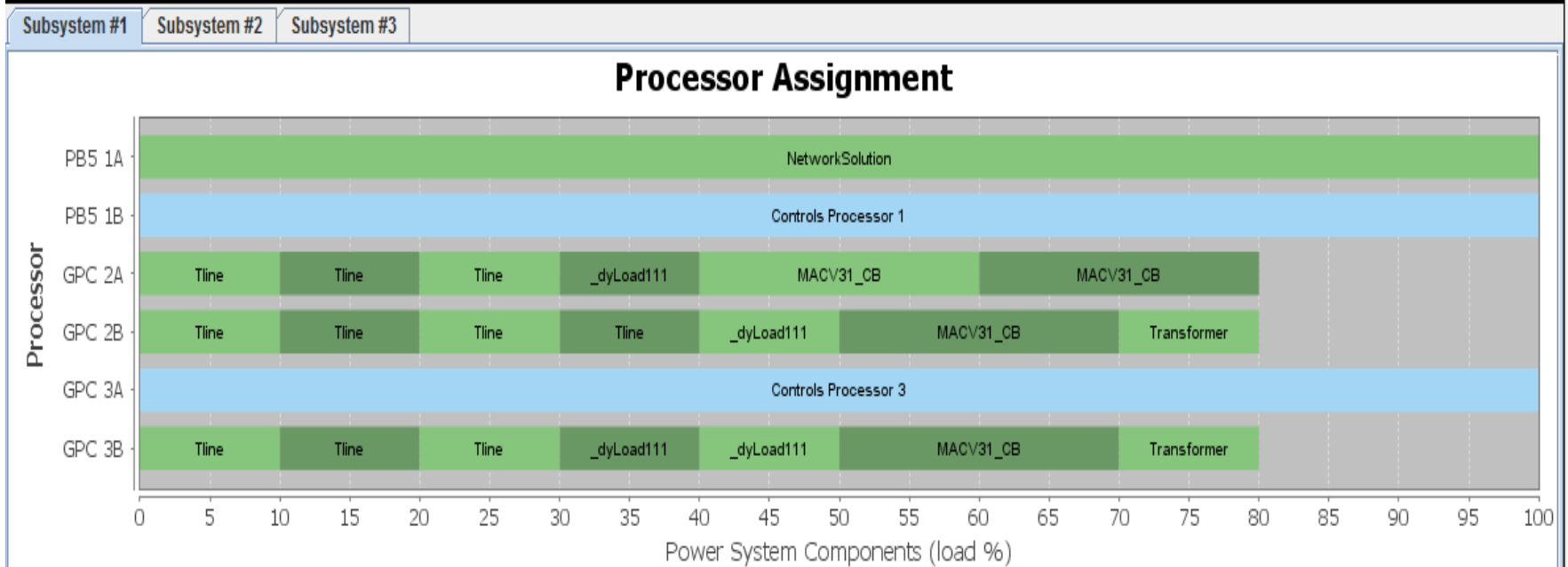
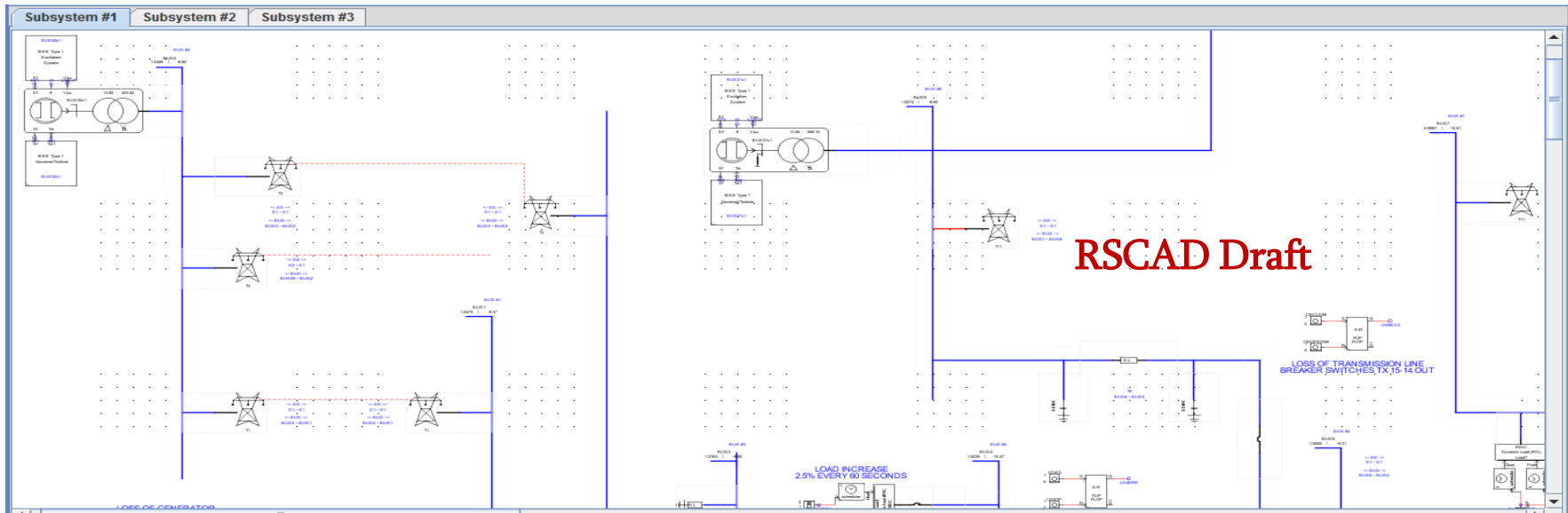


Figure 6: (a) RSCAD draft; (b) processor assignment

METHODOLOGY

_rtds_GTNET_PMU_v5.def									
PMU13 CONFIG		PMU14 CONFIG		PMU15 CONFIG		PMU16 CONFIG			
PMU9 CONFIG		PMU10 CONFIG		PMU11 CONFIG		PMU12 CONFIG			
PMU5 CONFIG		PMU6 CONFIG		PMU7 CONFIG		PMU8 CONFIG			
CONFIGURATION		PMU1 CONFIG		PMU2 CONFIG		PMU3 CONFIG		PMU4 CONFIG	
Name	Description	Value	Unit	Min	Max				
eC37data	Enable output of C37.118 data using GTNET	Yes		0	1				
Name	GTNET Component Name	PMUCharlie							
pmutype	PMU Model Type	Annex...		0	0				
cfgtype	Configuration frame format	Confia 2		0	1				
freq	Base Frequency (Hz)	60.0		0	1				
nPMU	Number of PMUs (maximum 24)	16		0	34				
adv	Delay Input Signal to align V & I	V bv 1dt		0	1				
eAngM	Enable Angle Difference Meter	NO		0	1				
nAngDiff	Angle Difference Meter Name (PMUx-PMUy)	angdiff		0	0				
sfx	Plot Signal Suffix								
calib_const	Common calibration offset applied to all PMU inputs	0	degrees	-360.0	360.0				
dt_adj	Time-step adjustment to all input signals	-3	dt	-500	500				
ePri	Enable Primary Signals	YES		0	1				
GT_SOC	GTSYNC advance TIME signal name	ADVSECD		0	0				
GT_STAT	GTSYNC advance STAT signal name	ADVSTAT		0	0				
phs_rot	Phase Rotation	ABC		0	1				
Port	GTIO Fiber Port Number	1		1	8				
Card	GTNET_PMU Card Number	1		1	8				
Proc	Assigned Controls Processor	3		1	40				
Pri	Priority Level	1		1					

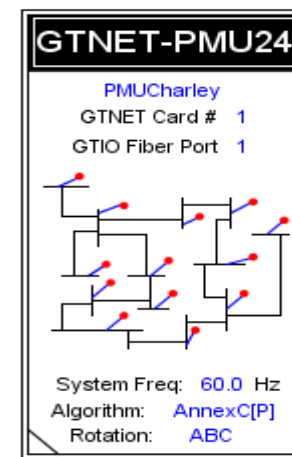
Figure 7: RSCAD-PMU component

PMU Parameters:

- IEEE C37.118.1-2011
- P-Class
- Positive sequence phasors V_1 & I_1
- Analogue measurement and digital word
- Polar format, real values, 60 fps, CFG-2
- IRIG-B time sync from the GTSYNC card

GTNET-PMU Card

PMU RSCAD Draft GTNET-PMU Component



METHODOLOGY

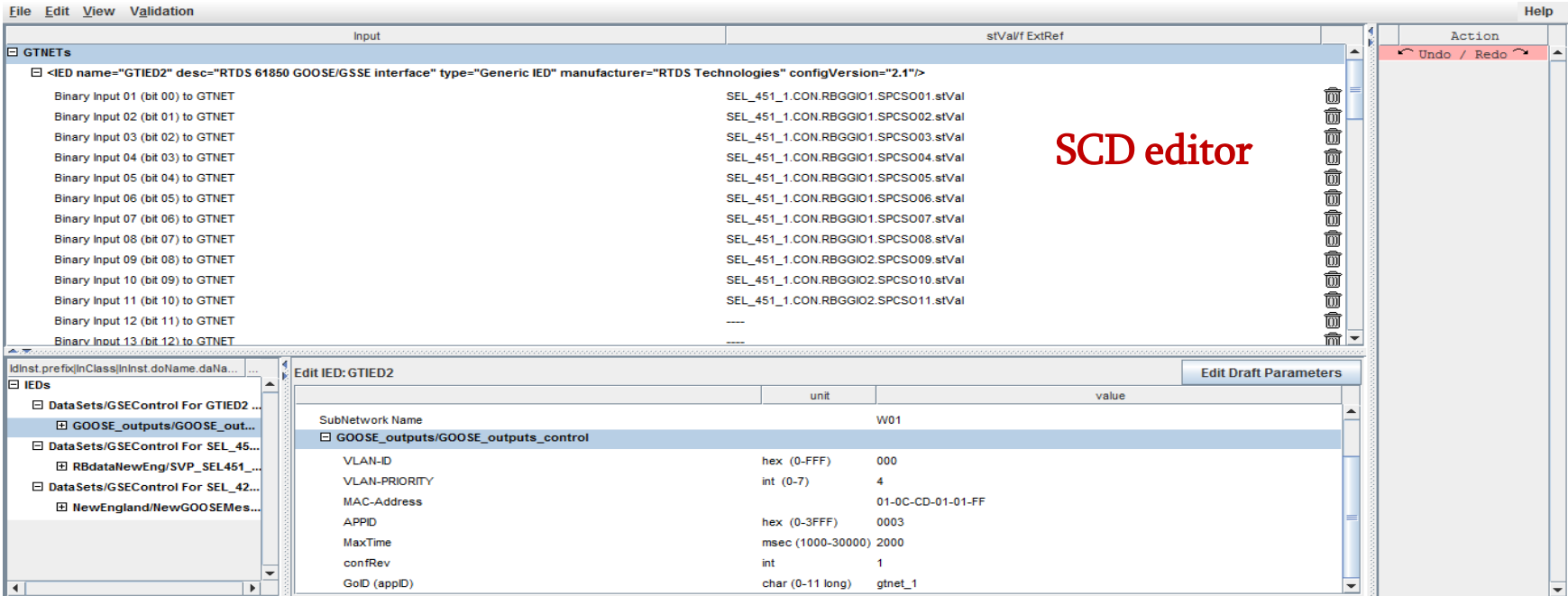
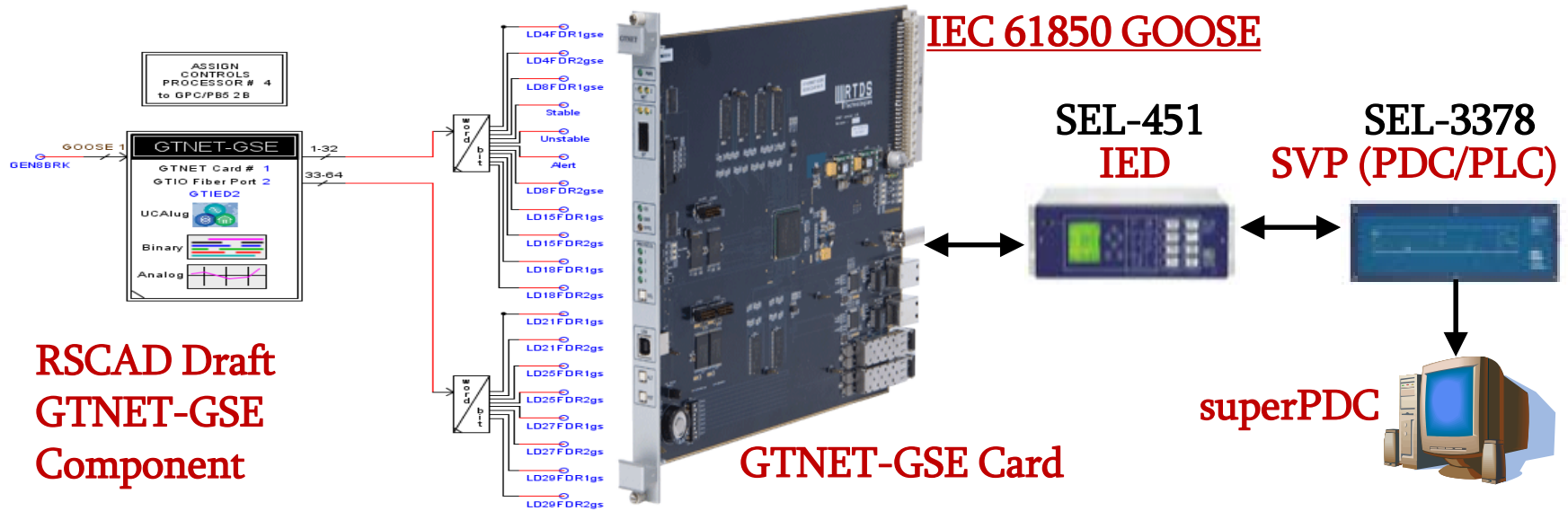


Figure 8: (a) RSCAD-GSE component; (b) RSACD SCD editor

METHODOLOGY

RSCAD Runtime

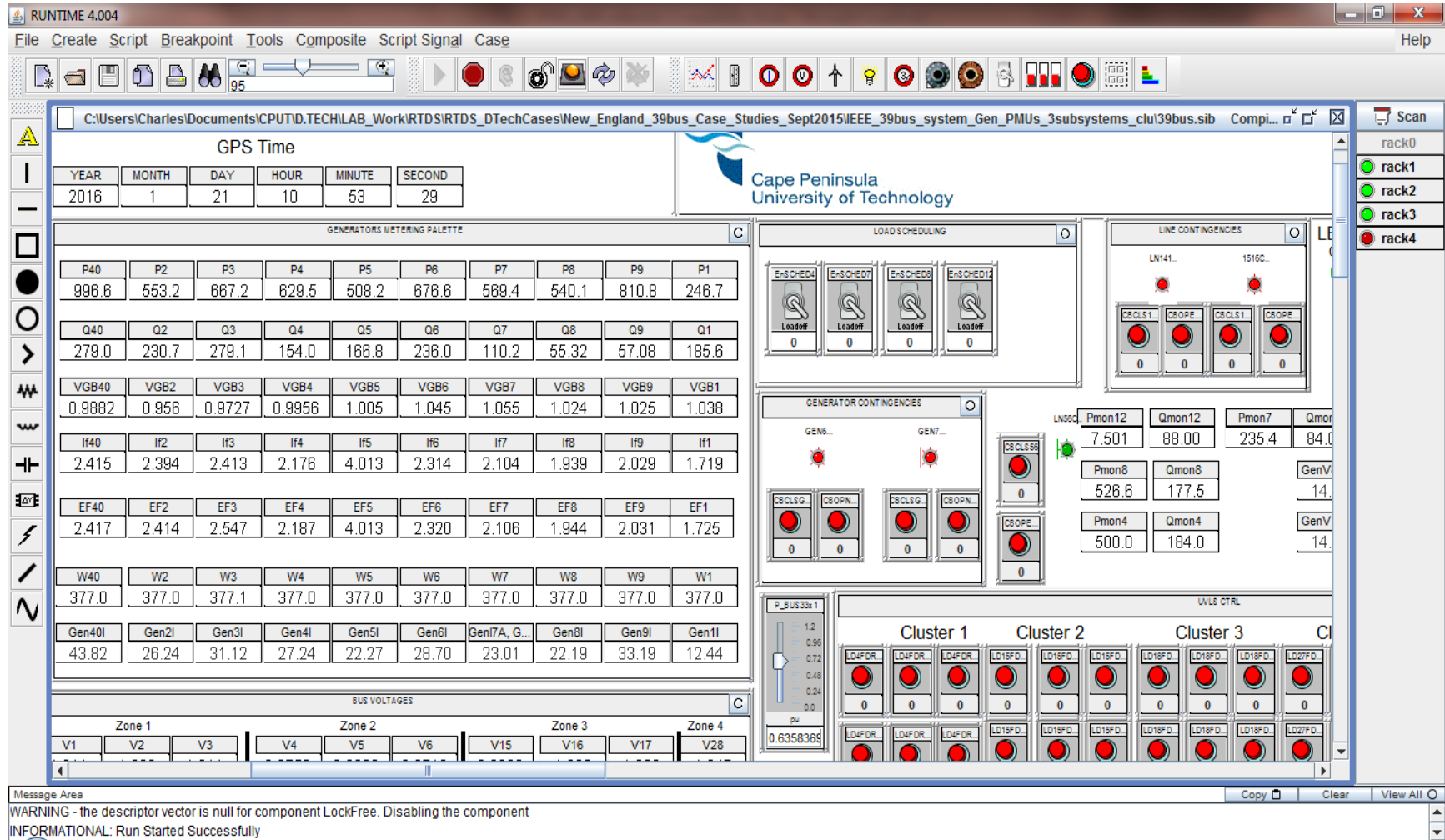
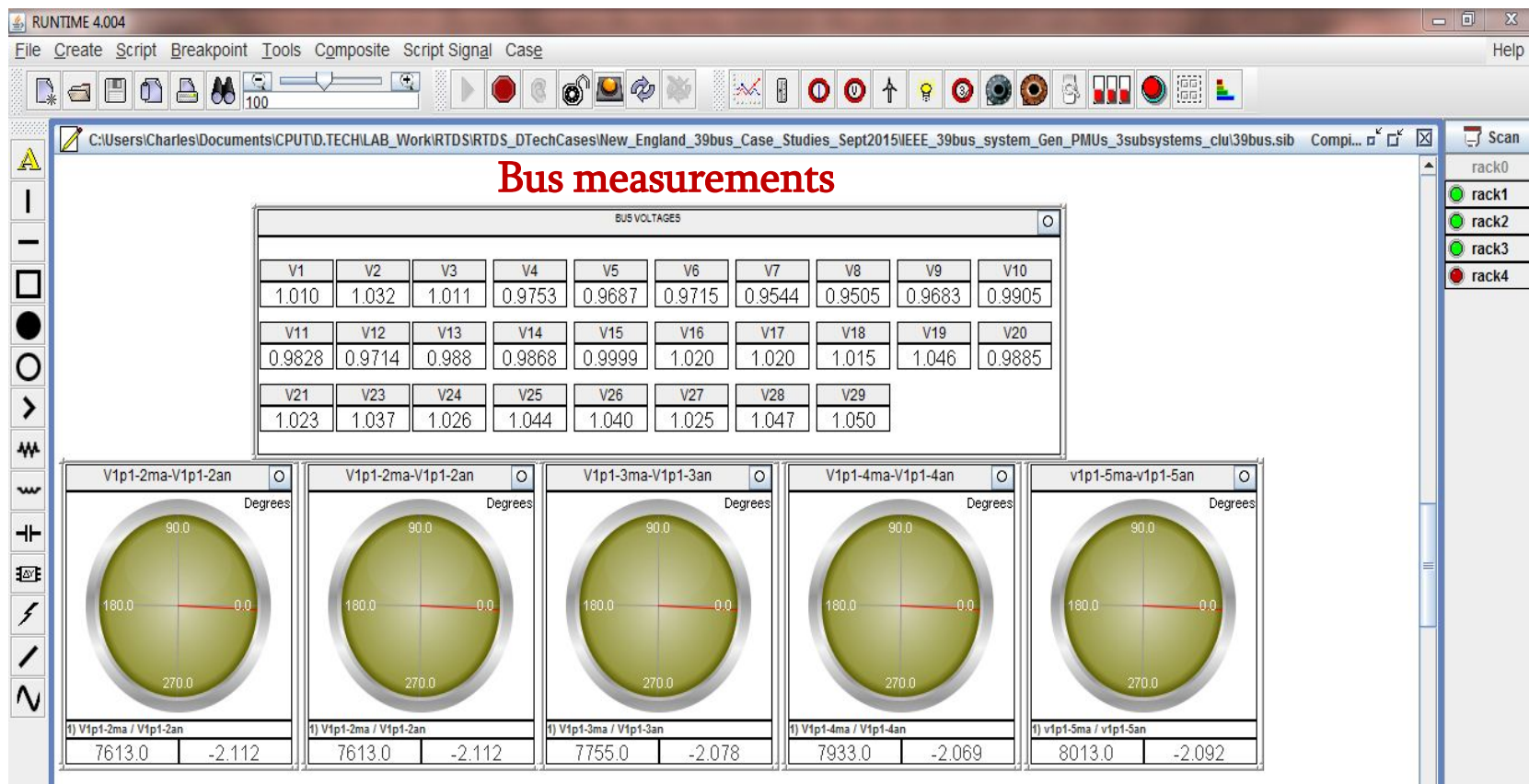


Figure 9: Runtime module with meters and controls

RSCAD Runtime



PMU vector plots

Figure 10: Runtime module with meters and PMU vector plots

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EXPERIMENTAL RESULTS

Simulation: Dynamic Analyses using the RTDS

Combinations of small disturbances & large disturbances

Case Studies:

- Case Study 1: Increased system loading
- Case Study 2: $N-2$ line contingencies + load increase
- Case Study 3: $N-2$ generator contingencies + load increase
- Case Study 4: Load increase + transformer ULTC & Generator OXL dynamics

Dynamic Load Scheduling

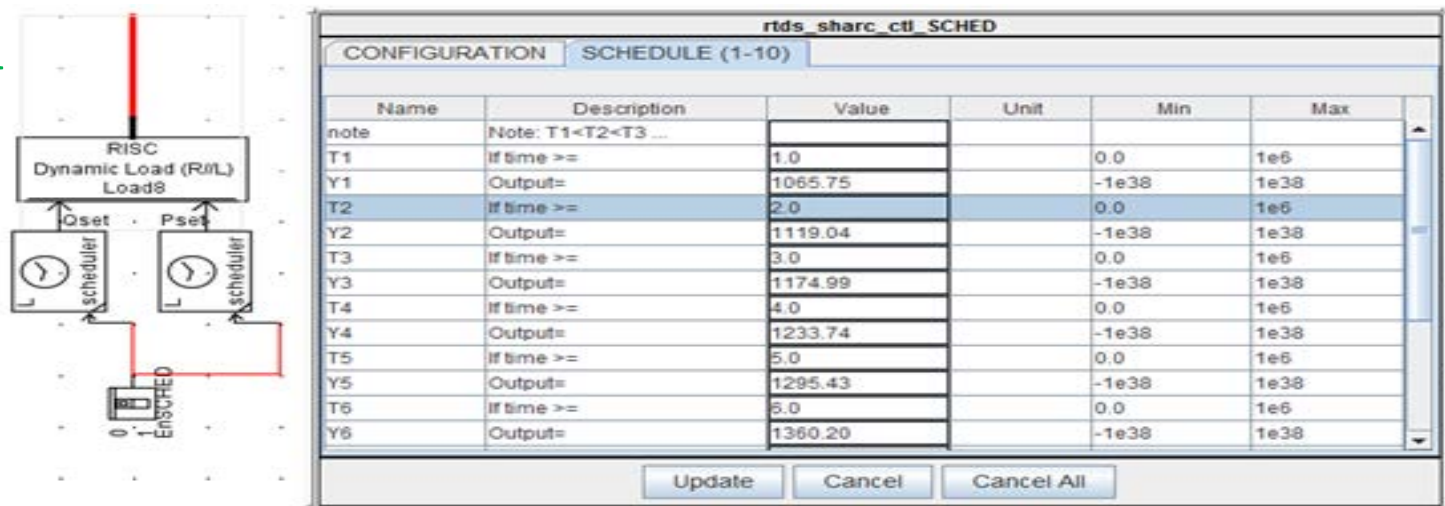


Figure 11: Real-time dynamic load scheduling

EXPERIMENTAL RESULTS

Testing with PMU Connection Tester

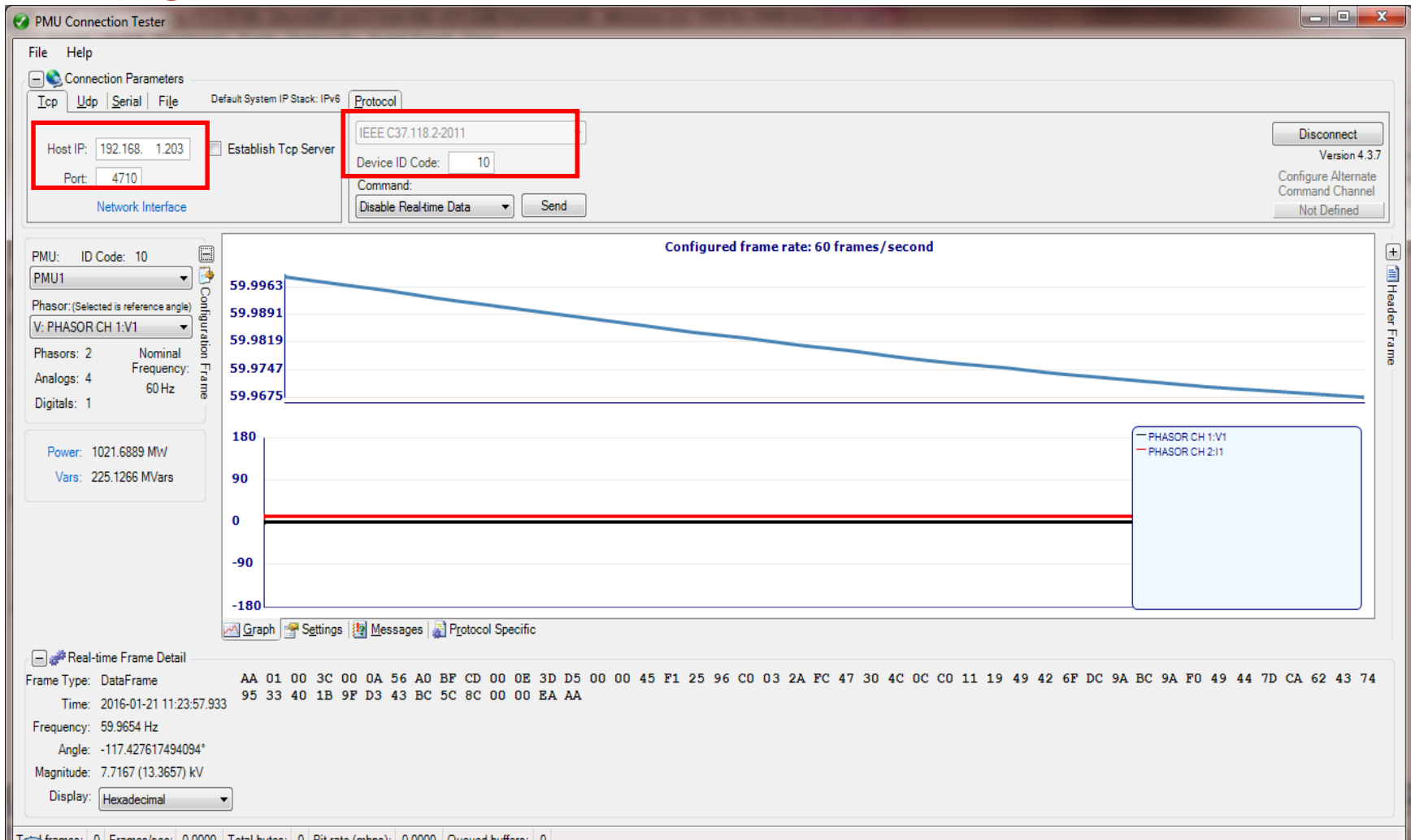
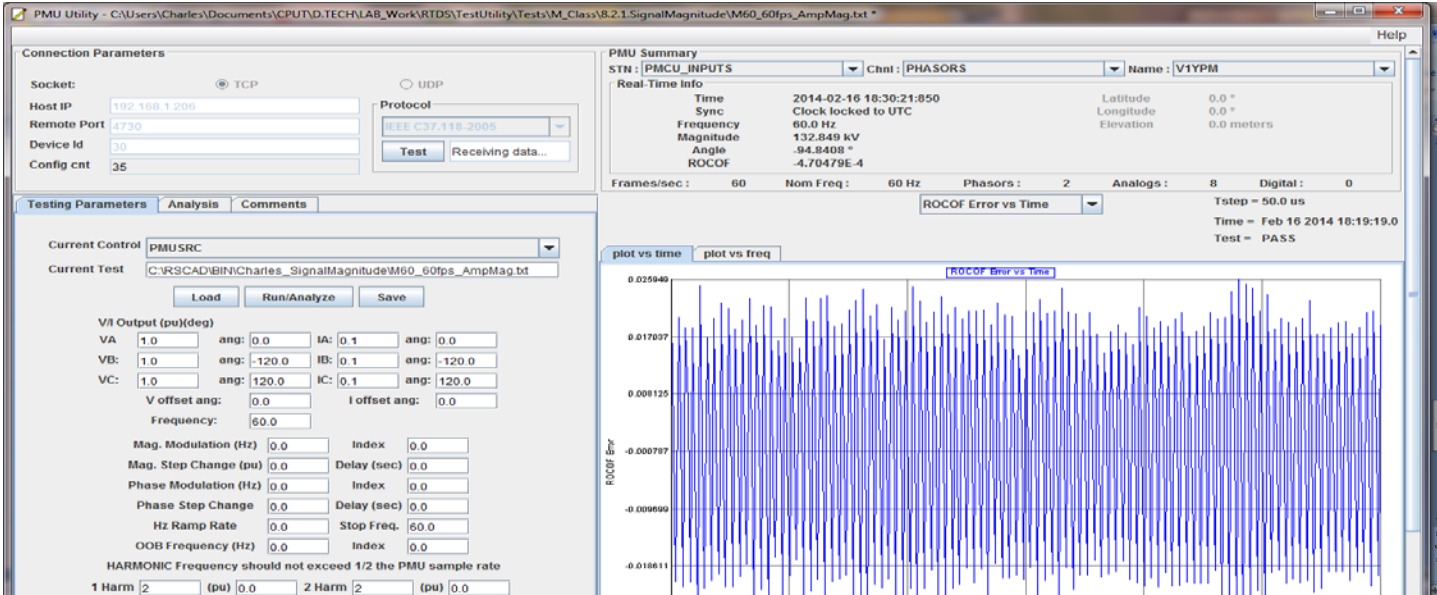


Figure 12: PMU connection testing

EXPERIMENTAL RESULTS

Testing with RTDS PMU Utility



TVE: 1%
FE: 0.005 Hz
RFE: 0.01 Hz/s

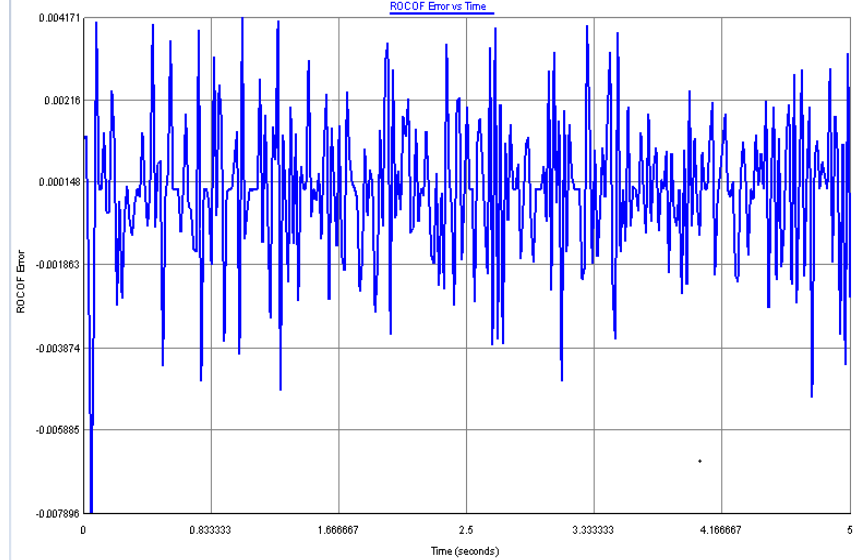
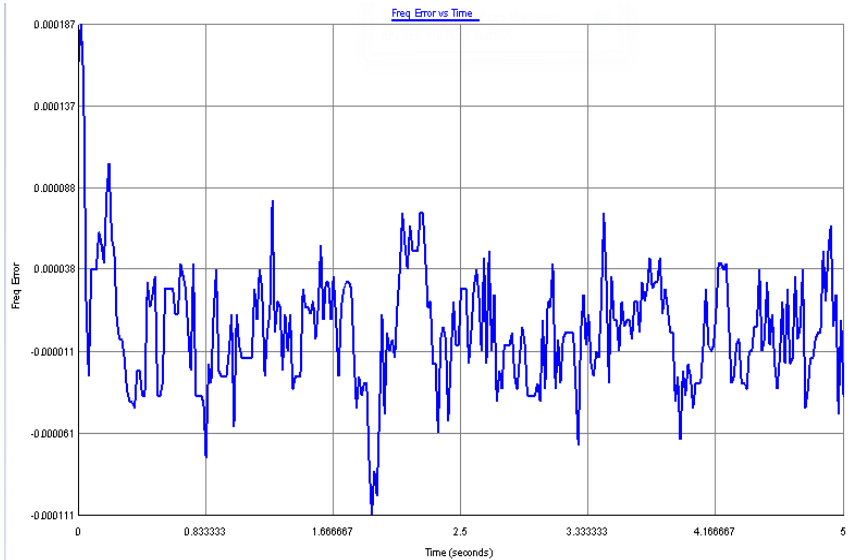


Figure 12: PMU connection testing

EXPERIMENTAL RESULTS

Ethernet Capture using Wireshark Network analyzer

RTDS_Synchrophasor_Wireshark.pcapng [Wireshark 1.8.1 (SVN Rev 43946 from /trunk-1.8)]

Filter: **synphasor** Expression... Clear Apply Save

No.	Time	Source	Destination	Protocol	Length	Info
2385	11.693849000	192.168.1.33	192.168.1.203	SYNCHRC	72	Command Frame, data transmission off
2408	12.693284000	192.168.1.33	192.168.1.203	SYNCHRC	72	Command Frame, send CFG-2 frame
2410	12.942782000	192.168.1.203	192.168.1.33	SYNCHRC	488	Configuration Frame 2
2411	12.946393000	192.168.1.33	192.168.1.203	SYNCHRC	72	Command Frame, data transmission on
2424	14.441348000	192.168.1.203	192.168.1.33	SYNCHRC	114	Data Frame
2427	14.461351000	192.168.1.203	192.168.1.33	SYNCHRC	114	Data Frame
2430	14.481333000	192.168.1.203	192.168.1.33	SYNCHRC	114	Data Frame
2432	14.501305000	192.168.1.203	192.168.1.33	SYNCHRC	114	Data Frame
2434	14.521360000	192.168.1.203	192.168.1.33	SYNCHRC	114	Data Frame

Frame 2540: 114 bytes on wire (912 bits), 114 bytes captured (912 bits) on interface 0

- Ethernet II, Src: RtdsTech_05:92 (00:50:c2:4f:95:92), Dst: CompalIn_59:e8:6f (1c:75:08:59:e8:6f)
- Internet Protocol Version 4, Src: 192.168.1.203 (192.168.1.203), Dst: 192.168.1.33 (192.168.1.33)
- Transmission Control Protocol, Src Port: 4710 (4710), Dst Port: btprjctrl (2803), Seq: 4275, Ack: 55, Len: 60
- IEEE C37.118 Synchronophasor Protocol, Data Frame
 - Synchronization word: 0xaa01
 - Framesize: 60
 - PMU/DC ID number: 10
 - SOC time stamp (UTC): 2016-01-21 11:18:50
 - Time quality flags
 - Fraction of second (raw): 50000
 - Measurement data, using frame number 2410 as configuration frame
 - Station: "PMU1"
 - Flags
 - Phasors (2)
 - Phasor #1: "PHASOR CH 1:V1 ", 7452.73V/_-113.48°
 - Phasor #2: "PHASOR CH 2:I1 ", 47999.03A/_-124.93°
 - Actual frequency value: 60.065163Hz
 - Rate of change of frequency: -0.067328Hz/s
 - Analog values (4)
 - Digital status words (1)

0000 1c 75 08 59 e8 6f 00 50 c2 4f 95 92 08 00 45 00 .u.Y.o.P .O....E.
0010 00 64 21 7d 40 00 40 06 94 da c0 a8 01 cb c0 a8 .d!}@.@.
0020 01 21 12 66 0a f3 be ff a4 98 e1 a6 41 98 50 18 .!.f.... .A.P.
0030 40 00 19 7b 00 00 aa 01 00 3c 00 0a 56 a0 be 9a @..{... <...V...
0040 00 00 c3 50 00 00 45 e8 e5 df bf fd 83 c1 47 3b ...P..E.G;
0050 7f 08 c0 0b 8b 80 42 70 42 b2 bd 80 c2 12 44 82 ..P.P.D

Figure 13: Synchronophasor packet sniffing using Wireshark

EXPERIMENTAL RESULTS

Aggregation using the SEL-5070 PDC

The screenshot displays the SEL PDC Assistant software interface. The main window is titled "Unnamed Connection - PDC Assistant" and features a menu bar with options: New, Open, Save, Save As, Close, Send Settings, Connect, Disconnect, and Local Services. A sidebar on the left contains navigation tabs for Home, Settings (Inputs, Outputs, Calculations, Archives, Loggers, Globals), Status (Real-time, Diagnostic Logs), Data (Retrieve Archives), and Administration (Device, User Accounts, General Security, LDAP).

The central area is titled "Real-time Status" and includes the following sections:

- Input Connections:** A table showing the connection for SVP (PDC ID: 6554, State: Receiving Data, Time Quality: Normal, Received Data Frames: 598).
- Input PMUs:** A table showing the PMU for SVP (PMU ID: 6554, State: Found, Status: OK, Unlock Time: Locked). A red box highlights the "Input PMUs" section.
- Timestamp:** 01/21/2016 11:44:44.416
- Frequency:** 60.015 Hz
- df/dt:** -0.038 Hz./s

Below these sections are three data tables:

- Phasors:** A table with columns Name, Magnitude, and Angle. It lists measurements for PO_V and PO_I from [001] to [010].
- Analogs:** A table with columns Name and Value. It lists measurements for AO from [001] to [025].
- Digitals:** A grid of digital status indicators for DWO (Digital Word Output) bits. The first two rows (DWO[001] and DWO[002]) show bits 01-04 in pink (value 1) and bits 05-08 in green (value 0). The remaining rows (DWO[003] to DWO[002]) show all bits in green (value 0).

At the bottom of the interface, there are three status indicators: "Project Status - No Errors", "PDC Sync - Synchronized", and "PDC Connectio".

Figure 14: Aggregation of PMU measurements using the PDC

EXPERIMENTAL RESULTS

Case Study 1

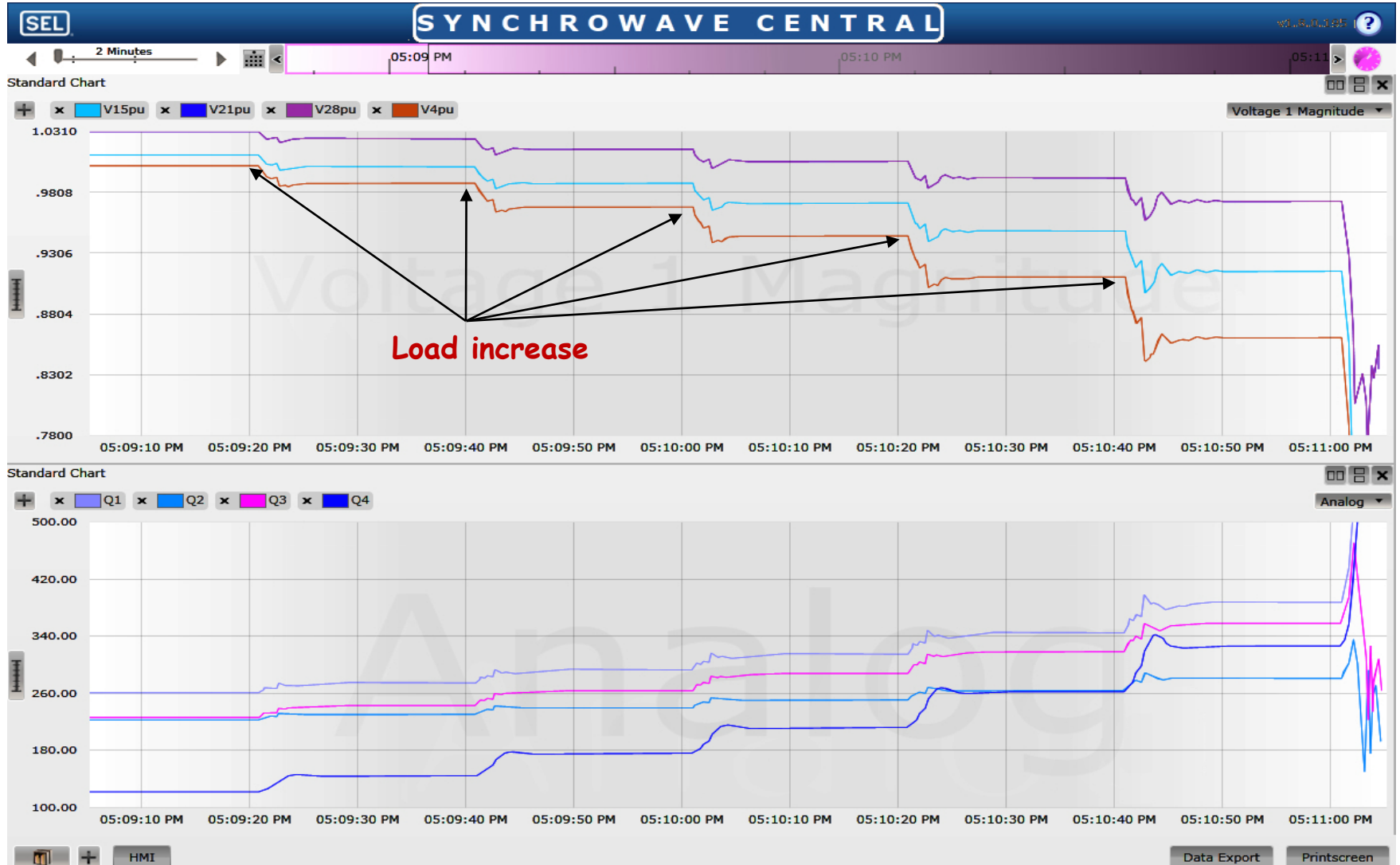


Figure 15: Case Study 1: Real-time plots of voltage phasors and generator MVar for increased system loading

EXPERIMENTAL RESULTS

Case Study 2

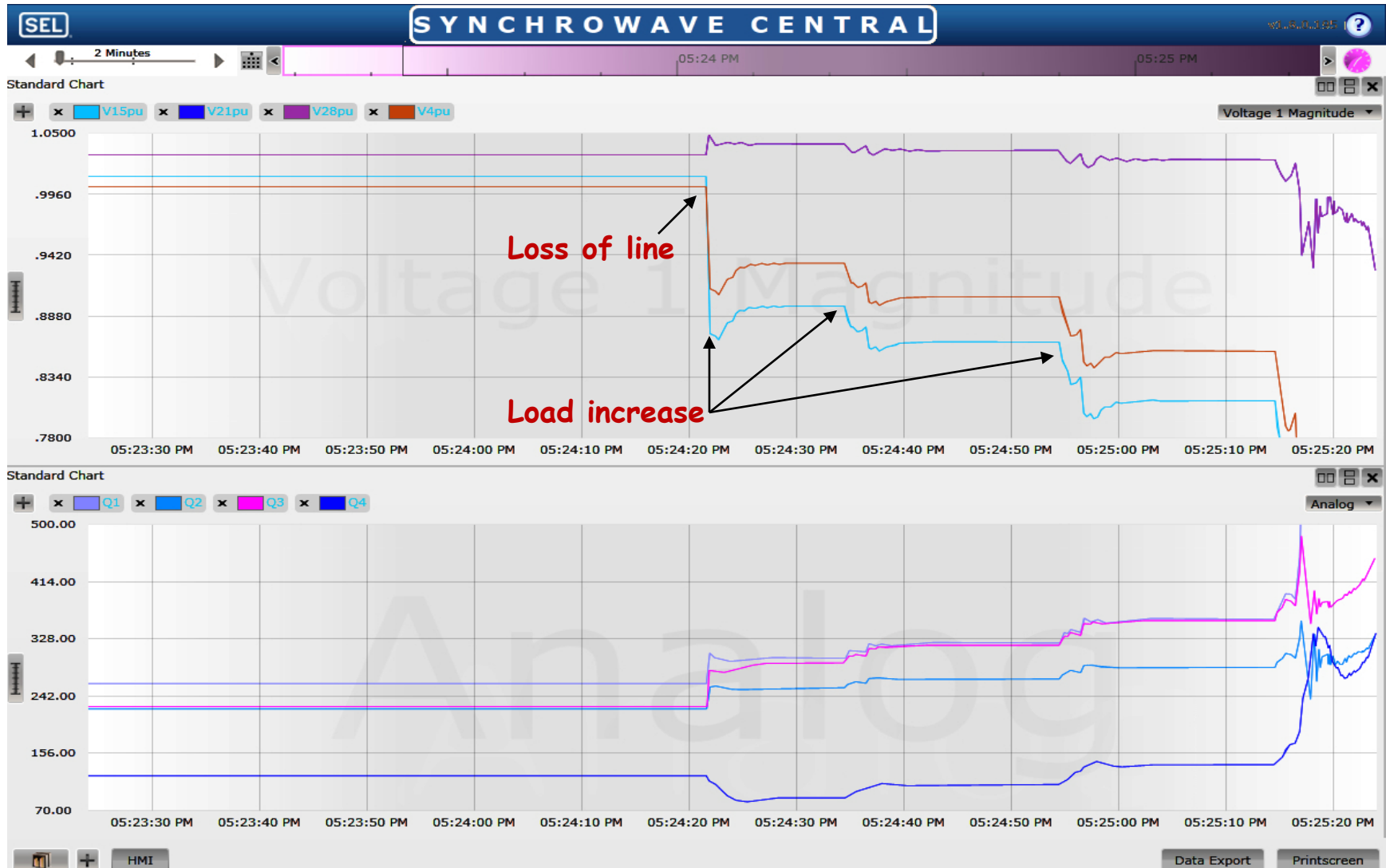


Figure 16: Case Study 2: : Real-time plots of voltage phasors and generator MVar for $N-2$ Line contingency and increased system loading

EXPERIMENTAL RESULTS

Case Study 3

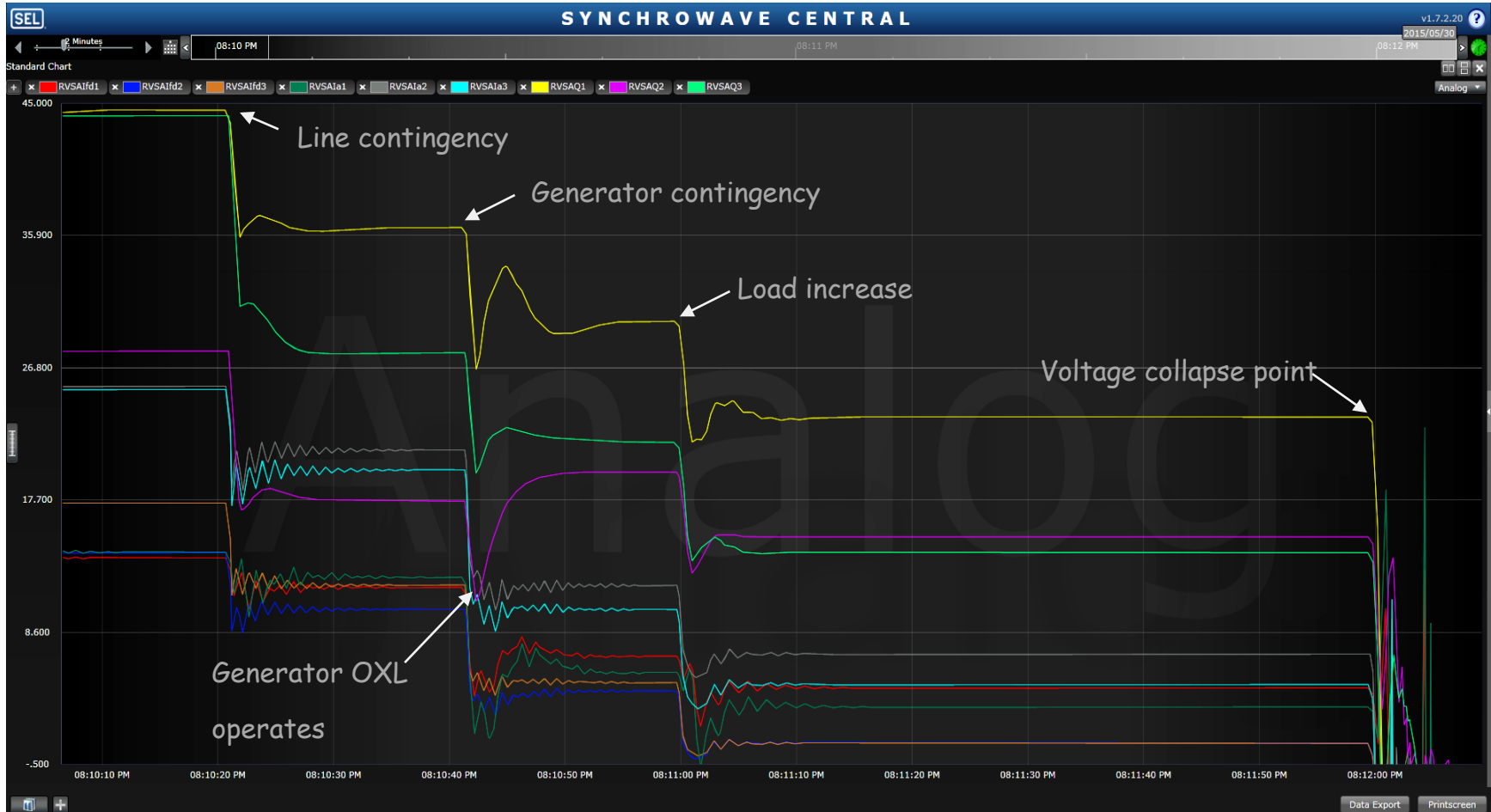


Figure 17: Case Study 3: Real-time plots of generator-derived indices for increased loading conditions, line - generator contingencies, and OXL operation

EXPERIMENTAL RESULTS

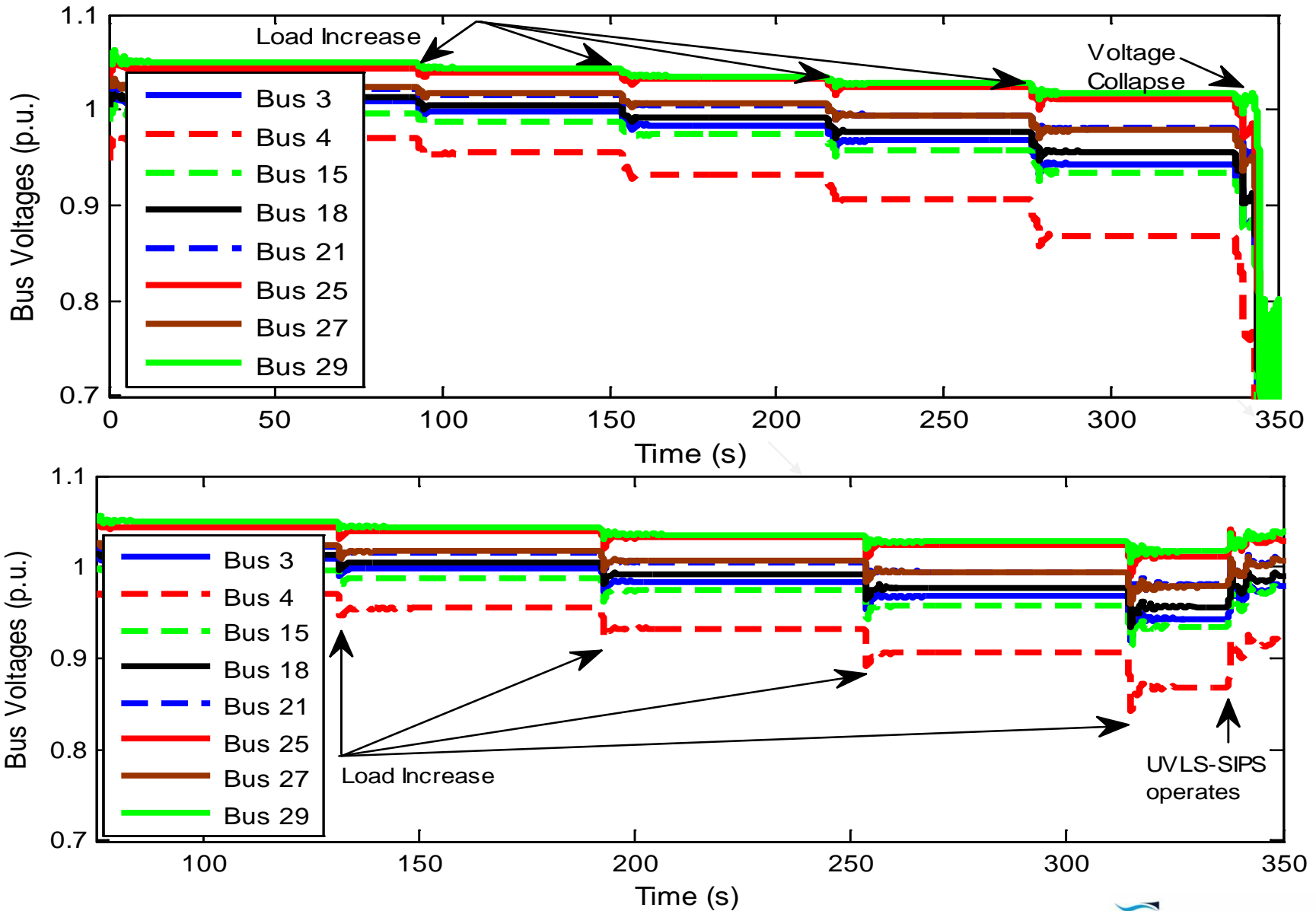


Figure 18: Increased loading (a) Without SIPS; and (b) with SIPS

EXPERIMENTAL RESULTS

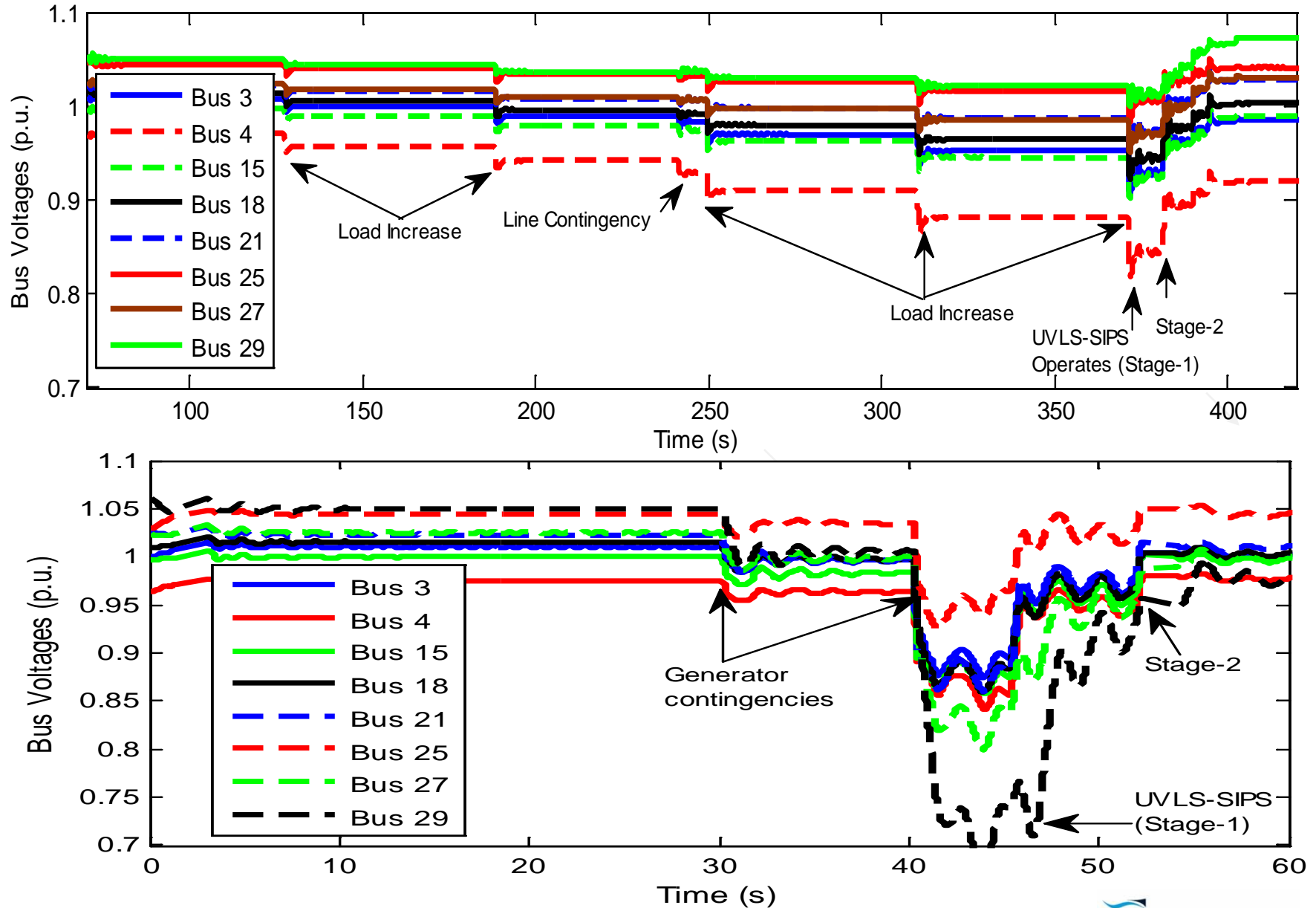


Figure 19: (a) Load increase and line contingency; (b) generator contingencies

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- Three generator-derived RVSA indices based on PMU measurements
- Comparison of the various RVSA indices.
 - EGSCR index gave the best performance
 - Less sensors, less measurements,
 - ease of practical implementation
- SIPS using undervoltage load shedding
- A real-time ‘proof-of-concept’ testbed was implemented
- Future work: Impact of pervasive network conditions and cyber security in wide area applications



- A.C. Adewole, R. Tzoneva. (2014) Real-time deployment of a novel synchrophasor-based voltage stability assessment algorithm. *International Review of Electrical Engineering*. 9(5), pp. 1021-1033.
- A.C. Adewole, A.C., R. Tzoneva. (2015) Wide Area Voltage Stability Assessment Based on Generator-Derived Indices Using Phasor Measurement Units. *Industrial and Commercial Use of Electricity (ICUE) Conference*, 17-19 August 2015, Cape Town, South Africa, pp. 291-298.
- A.C. Adewole, R. Tzoneva. (2015) Synchrophasor-Based Online Coherency Identification in Voltage Stability Assessment. *Advances in Electrical and Computer Engineering (AECE)*, 15, (4), pp. 33-42.
- A.C. Adewole, R. Tzoneva. (2015) Using generator-derived indices to assess wide area voltage stability. *Energize Magazine*, October 2015, pp. 21-26.
- B. Avramovic, L. K. Fink. (1992). Real-time reactive security monitoring, *IEEE Transactions on Power Systems*, 7, pp. 432–437.
- IEEE Standard for synchrophasor measurement for power systems, IEEE Standard C37.118.1-2011.
- P. Kundur. (1994). *Power system stability and control*. McGraw-Hill.
- V. Madani, D. Novosel, S. Horowitz, M. Adamiak, J. Amantegui, D. Karlsson, S. Imai, A. Apostolov. (2010). IEEE PSRC Report on Global Industry Experiences With System Integrity Protection Schemes (SIPS), *IEEE Transactions on Power Delivery*, 25, (4), pp. 2143-2155.
- O.A. Mousavi, M. Bozorg, R. Chekaoui. (2013) Preventive reactive power management for improving voltage stability. *Electric Power System Research*. 96, pp. 36-46.
- R. A. Schlueter. (1998). A voltage stability security assessment method, *IEEE Transactions on Power Systems*, 13, pp. 1423–1438.
- C.W. Taylor, R. Ramanathan. (1998) BPA reactive power monitoring and control following August 10, 1998, power failure. *In proc. VI Symp. Specialists Elect. Oper. Expansion Planning, Salvador, Brazil*.

Thank you

Questions?