









Advanced Power Hardware in Loop Test Setup for Evaluation of Utility Applications of Emerging Power Electronic Apparatus

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Agenda

Introduction

- Industry challenges with new technologies
- SDG&E Integrated Test Facility (ITF)
- Hardware in Loop (HIL) test setups at ITF
- Power HIL inverter test setup versus Traditional testing
- Smart inverter testing
- Dynamic load balancer testing

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- Test cases and results
- Summary



Industry Challenges – Emerging Technologies

Renewable Generation	Energy Storage	Microgrids	PMUs
 High penetration issues (PQ, stability and protection) Smart inverter controls Fault Current 	 Performance evaluation Control functions Integration 	 Design & Protection Safety Control & Operation 	 Application evaluations Communications infrastructure (especially for Distribution)

Modeling, Analysis, Testing, and Diagnostics is required prior to field deployment of a new technology or wide scale utilization





Integrated Test Facility (ITF)





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- Opened January 2014
- Seven Labs
 - Power System (10 RTDS racks)
 - DER (various DG and Energy Storage)
 - Smart Garage
 - Home Area Network
 - Information Security
 - Foundational/Communication
 - Situational Awareness

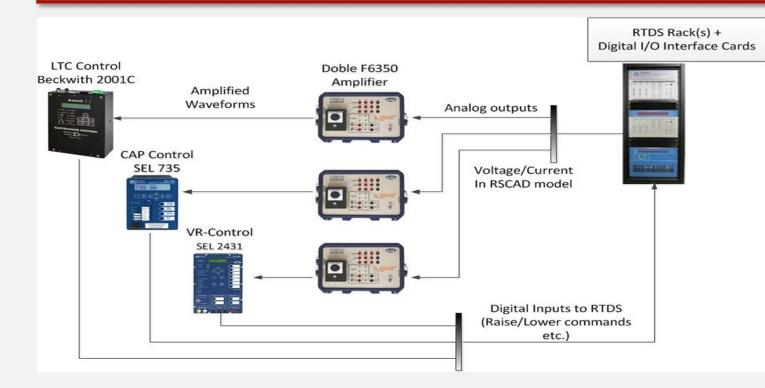


ITF Purpose and Utilization

- Purpose
 - Allows for internal development and retention of institutional knowledge
 - A true cross-functional effort, designed to help projects from different departments at SDG&E coordinate and integrate, increasing SDG&E's knowledge of power system and advanced technologies
- Projects
 - EPIC
 - Borrego/DERMS
 - Energy Storage Integration
 - Volt/VAR Optimization
 - Smart Inverter Pilot
 - Resilient GPS Spoofing
 - Power Your Drive



CHIL Test Setup for Integrated Volt/VAR Control



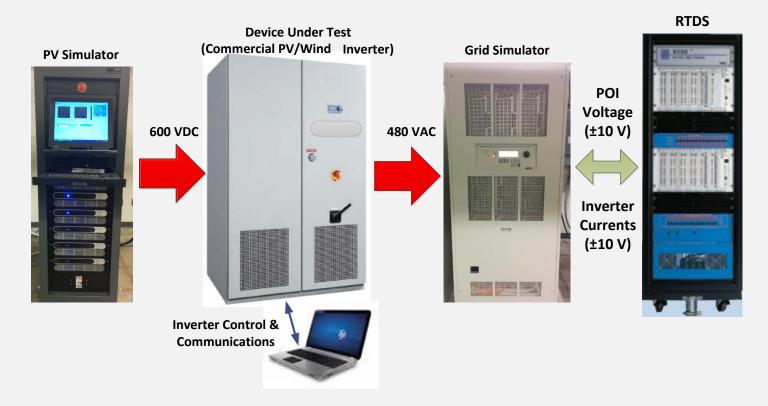
Device under test: Under load tap changer (LTC), Capacitor controllers (SEL 735), Line voltage regulator controller (SEL 2431)





Power Hardware in Loop Testing (PHIL)

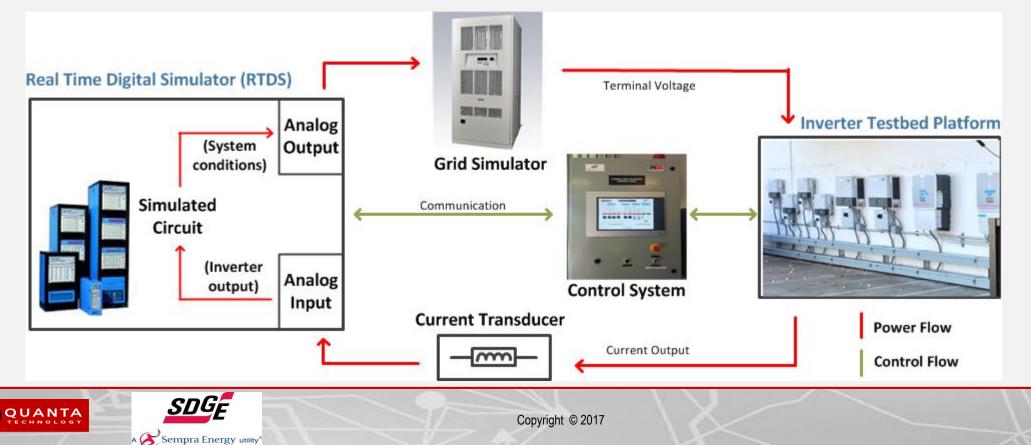
- High power amplifiers (grid simulator): in kVA range (e.g. 90 kVA), and up to 480 V
- Power Electronic device under test (inverter, converter, FATCS device)



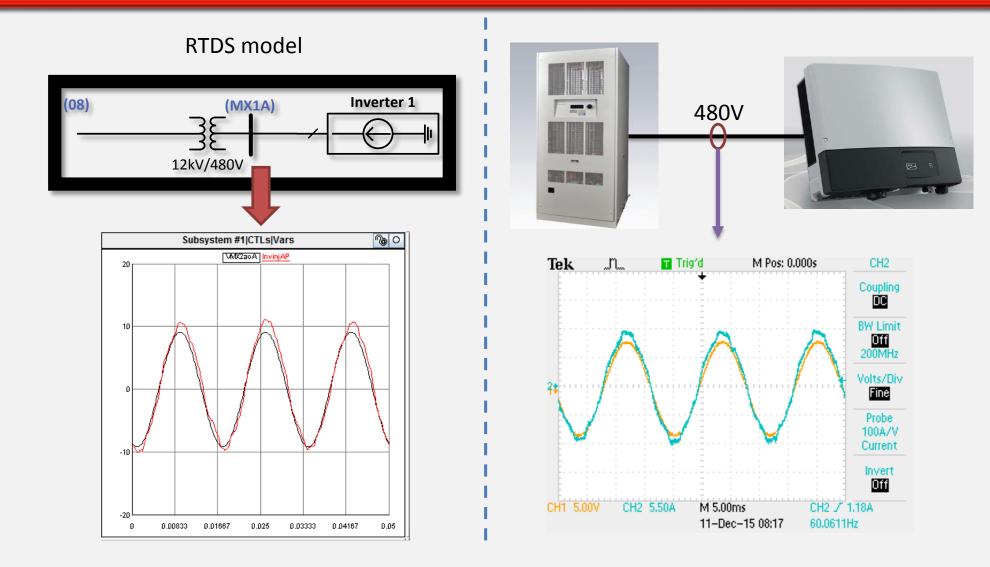


Test Setup for Smart Inverter Testing - PHIL

- Power system (distribution circuit) is represented in Real Time Digital Simulation (RTDS) environment
- Voltage at PCC of inverter is measured and applied to inverter through power amplifiers
- Inverter output (current injection from inverter) is measured and injected to the simulated circuit at PCC
- Inverter output changes the voltage and power flow at PCC and interacts with the circuit



Waveform Comparison: RTDS & Real World





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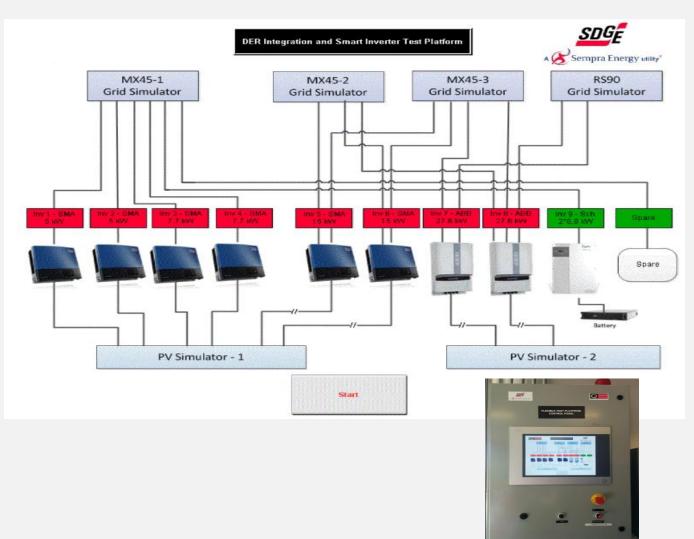
Smart Inverter Test Bed – Example Project





Control and DC feed





Smart Inverter Test Bed – ITF Setup

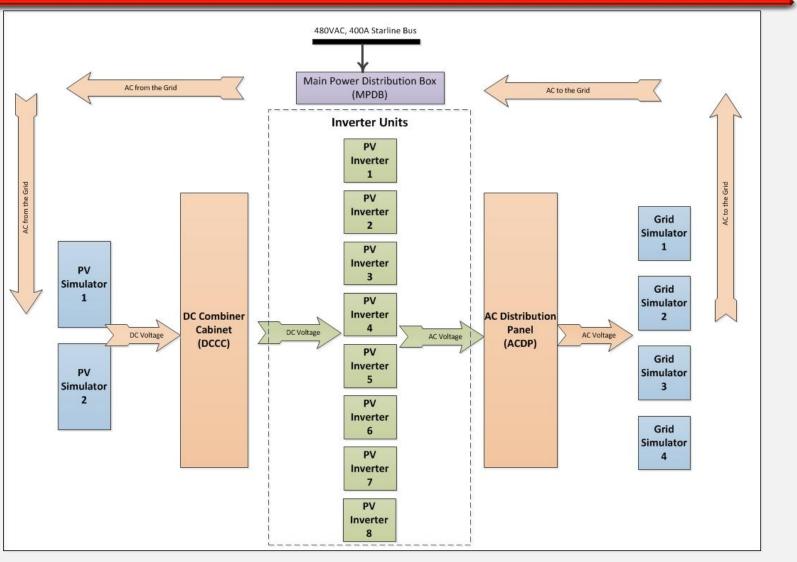
- Multiple inverters from various vendors
 - Three phase & single phase inverters
 - Grid-tie & grid forming inverters
- Flexibility in changing the setup configurations
 - Two or four inverters in parallel
 - Groups of two inverters at one location

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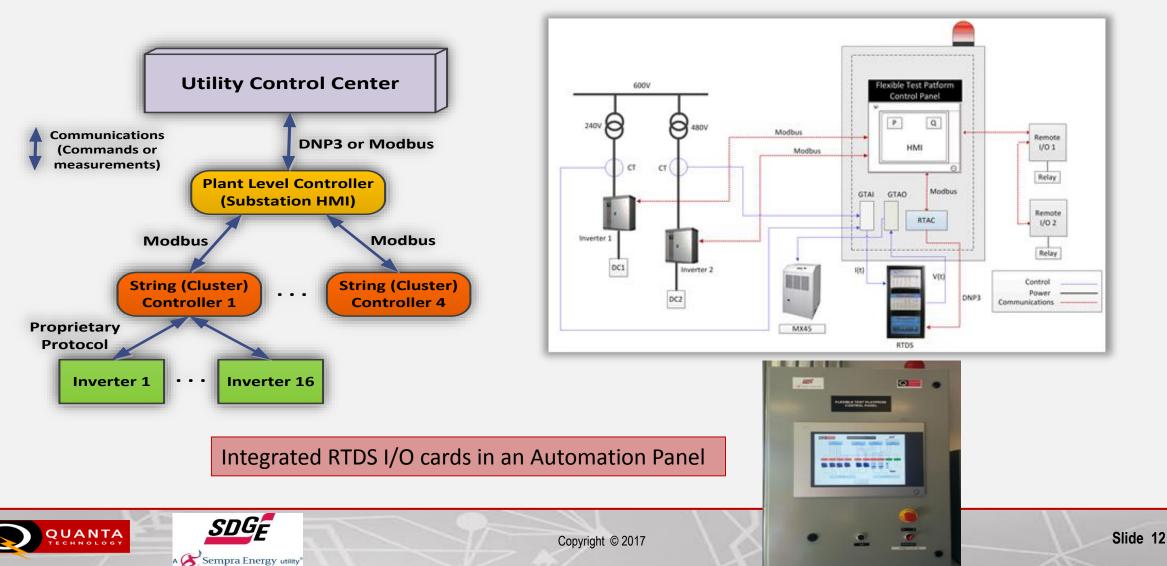
- Mix of 1Ph and 3Ph
- Control through various communication schemes (Modbus, DNP3, IEC 61850)

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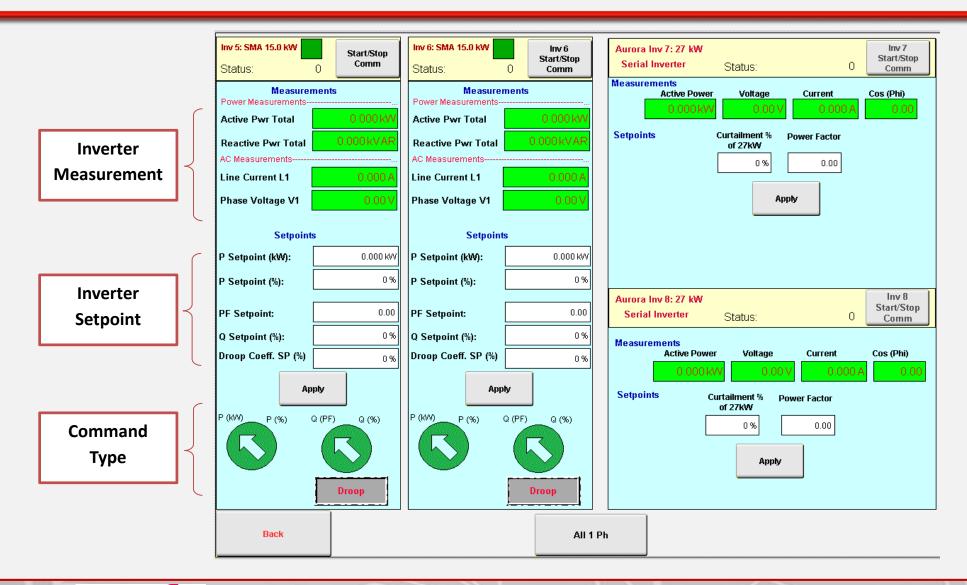


DG Dispatch: Inverter Controls & Communications

Representing Utility approach in communications and controls of PV inverters (Dispatch)



Site Controller and HMI for Inverter Controls





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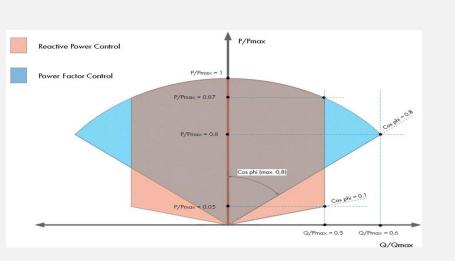
Typical Smart Inverter Test Cases

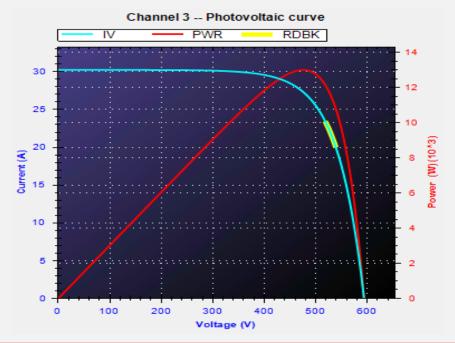
- Voltage and Frequency Variations (Ride-through)
- Fault Current and Protection Analysis (e.g. anti-islanding, faults on adjacent circuits)
- Inverter Dynamic Response to change in DC resources (intermittency) and P/Q setpoints
- Power Conversion Analysis (Efficiency, Waveform Quality, Harmonics)
- Advanced Communications and Controls
- Inverter Characteristics (P & Q Curves)

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- Load Rejection
- MPPT Accuracy







P-Q Characteristics of PV Inverters

P(kW)

- Testing the reactive power capability curve of the inverter
 - P = about rated kW

Q(kvar)

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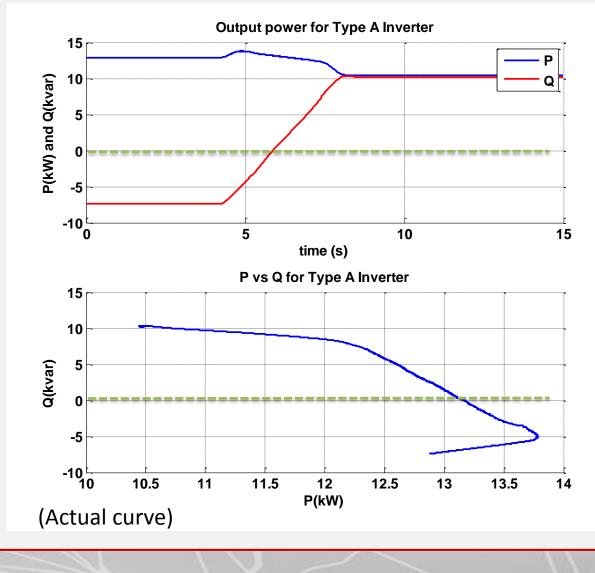
Changing Q from -5 kvar to +10 kvar

(Theoretical curve)

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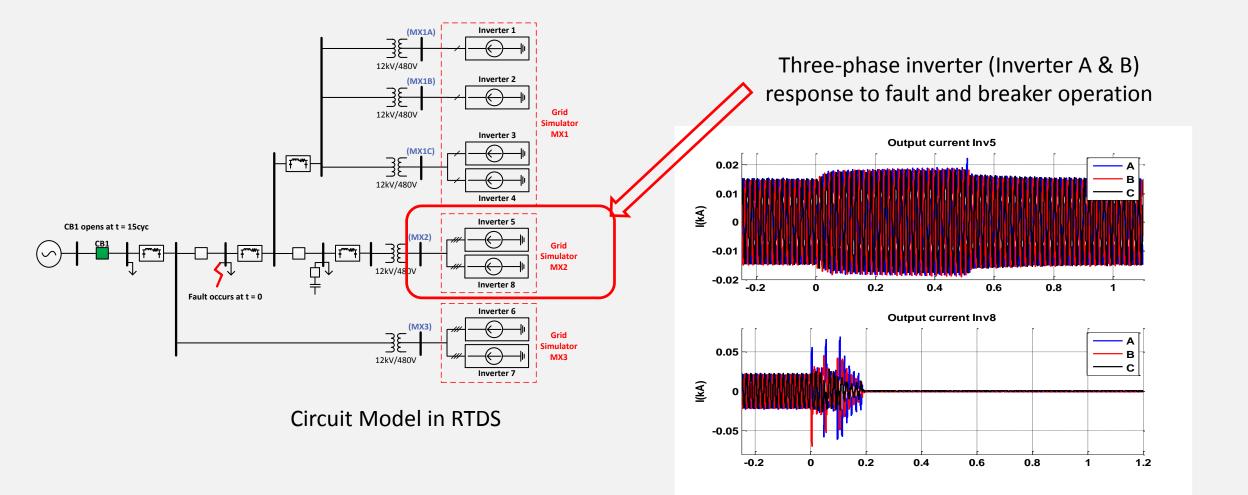
P has dropped (priority on Q)



Fault Response Tests

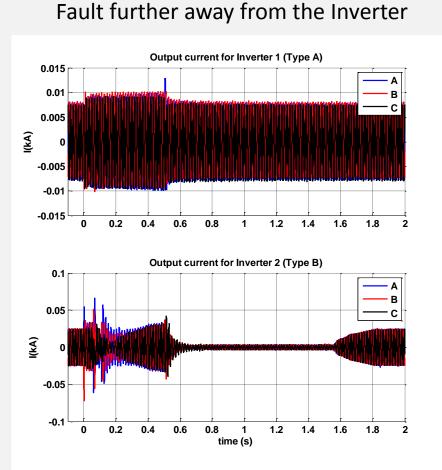
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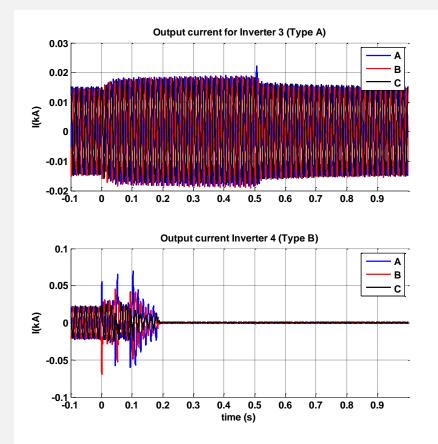




Fault Ride Through Tests



Fault Close to the Inverter

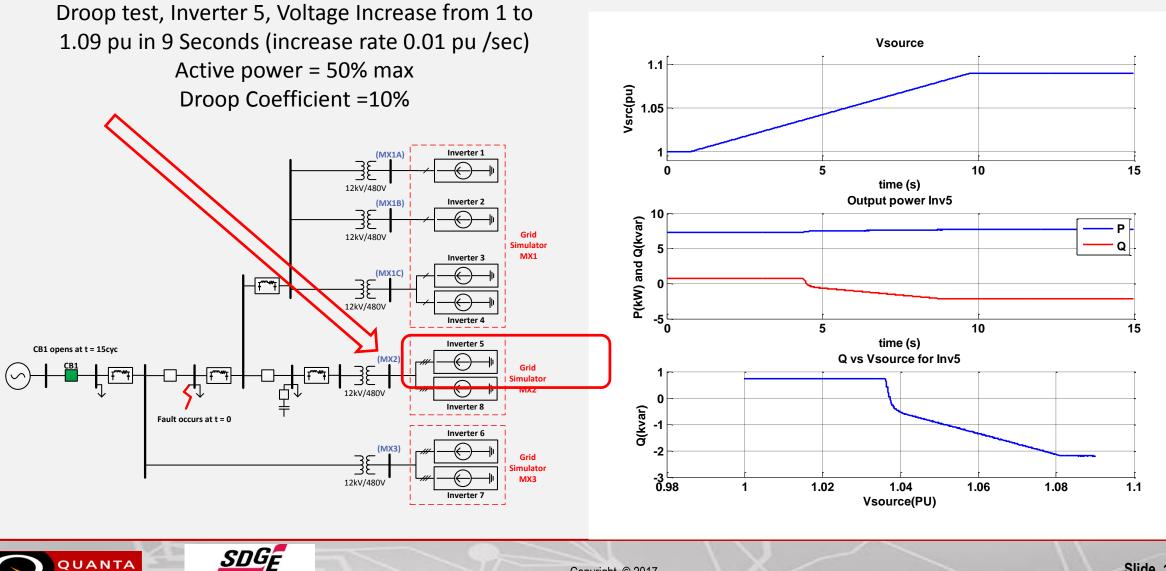


SLG Fault, 30 cycles

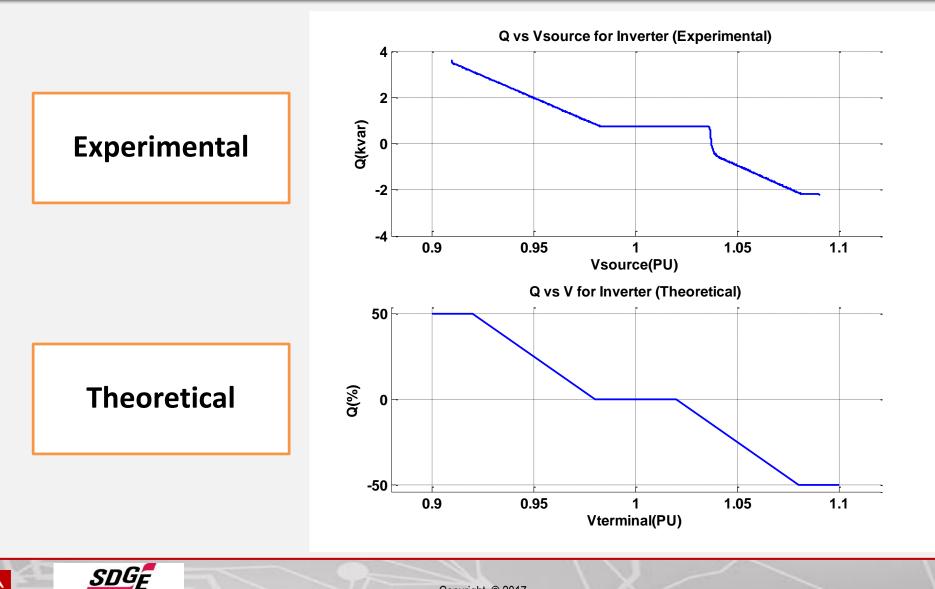


Q-V Droop Characteristic Tests

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Q-V Droop Characteristics – Comparison





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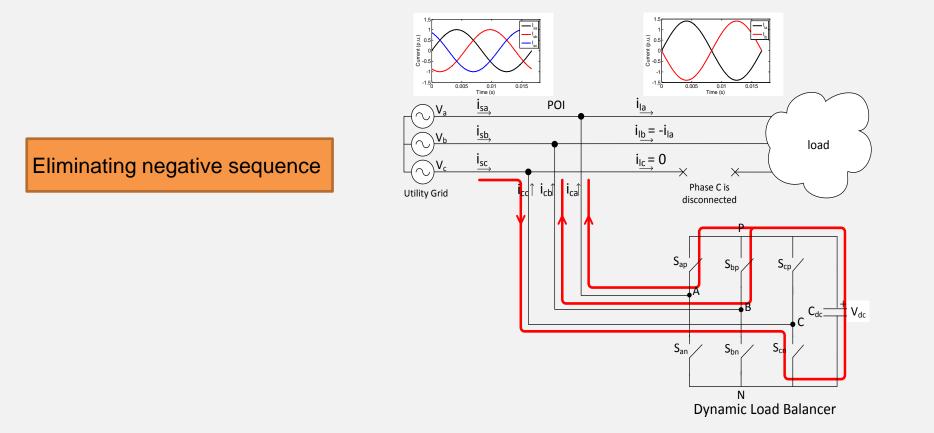
New Technology Evaluation with PHIL

Dynamic load balancing concept (DLB)

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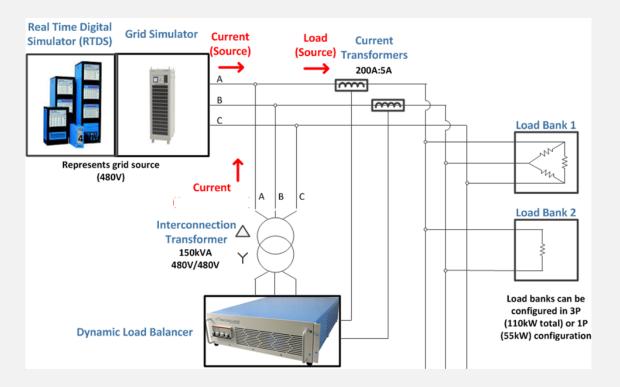
• Using power electronic converters to balance the load on distribution circuits from upstream view





150 kVA Hardware Testbed and DLB rack

RTDS is used to reflect the changes in the voltage at the point of connection to the device under test

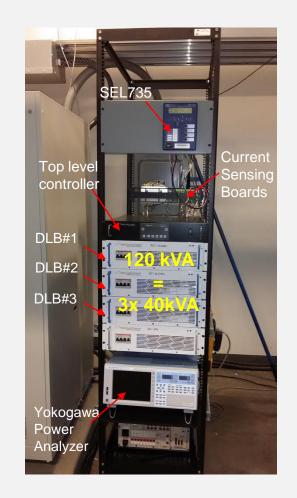


120 kVA Power Hardware in loop Testbed

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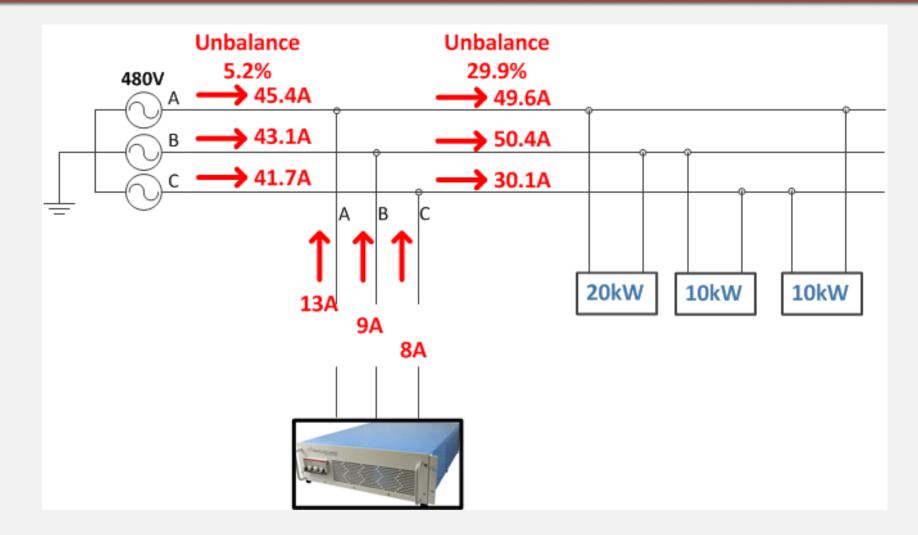
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DLB rack

Example 480V – Resistive Load Test





25 kW 3-Ph Balanced Load

Integ(EL1):Reset Integ(EL1):Reset Normal Mode(Trg) Normal Mode(Trg) Peak Over YOKOGAWA Peak Over YOKOGAWA Scaling Line Filter Scaling Line Filter= AVG Freq Filter= PLL1: U1 60.001 | PLL2: U1 60.001 | PLL1: U1 60.008 PLL2: U1 60.008 Freq Filter CF:3 CF:3 300.0 A 300.0 A 300.0 A 11 300.0 A 12 300.0 A 15 300.0 A $\Sigma A(3P3W)$ ΣA(3P3W) Element Element 600V 50mA 600V A 50mA Imb = 2.7%Imb = 3.6%Sync: 11 Integ:Re Sync: 11 Integ: Res _ Element 2 _ HR _Element 2_H U2 600V AUTO 12 50mA U2 600V MUI 12 50mA Sync: 12 Integ:Res Sync: 12 Integ:Res ΣB(3P3W) Element 3 HRM1 U3 600V 1000 I3 2A ΣB(3P3W) Element 3_HRM U3 600V 1000 2A Sync: 13 Integ:Reset Element 4_HRM1 U4 600V I4 2A Sync: 12 Integ:Reset Sync: 13 Integ:Reset Element 4 HRM U4 600V 14 2A Sync: 12 Integ:Reset Element 5 HRM Element 5 HRM US 1.5V AUG 15 50mA Sync: 15 Integ:Reset US 1.5V IS 50mA Sync: IS Integ:Reset Element 6 HRM1 U6 1.5V 2000 16 10mA 2000 Sync: 10 Integ:Reset Element 6 HRM U6 1.5V AUTO 16 10mA AUTO Sync: 10 Integ:Reset I range = +/- 300 A I range = +/-300 A -300.0 A -300.0 A -300.0 A -300.0 A -300.0 A -300.0 A 0.000s << 1602 (p-p) >> 100.000ms << 1602 (p-p) >> 100.000ns 2015/07/21 10:00:08 2015/07/21 10:00:54 Update 36 (200msec) Update 83 (200msec)

DLB is ON

DLB is OFF

		IS (A)				I	STHD (?	⁄₀)	IDLB (A)		
Test #	DLB	ISA	ISB	ISC	% Imb	ISA THD	ISB THD	ISC THD	IDLBA	IDLBB	IDLBC
•	OFF	31.1	30.5	30.1	2.7	5.5	4.7	4.3	x	Х	Х
A	ON	32.2	31.0	30.5	3.6	7.8	7.3	5.4	3.0	2.0	3.0



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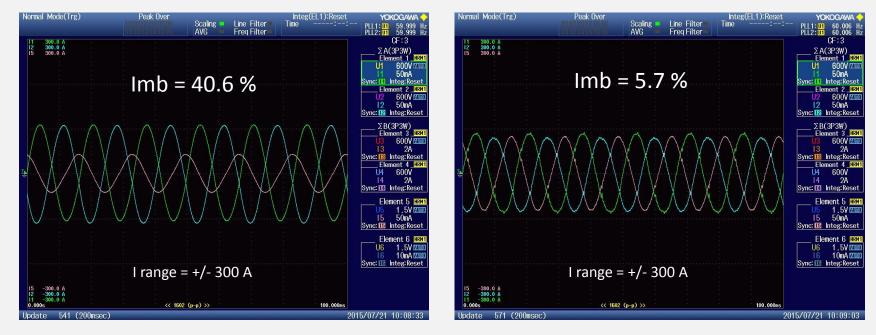
25 kW 3-Ph Balanced Load and 25 kW 1-Ph Load Between Phase A and B

DLB is OFF

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DLB is ON



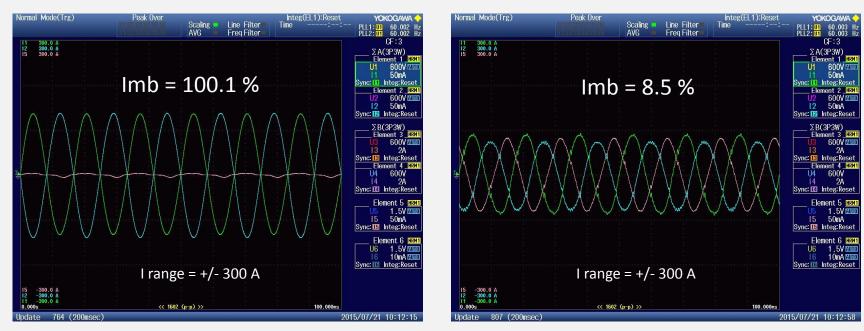
			IS (A)				1	S THD (%	%)	IDLB (A)		
	Test #	DLB	ISA	ISB	ISC	% Imb	ISA THD	ISB THD	ISC THD	IDLBA	IDLBB	IDLBC
Γ	Г	OFF	62.4	63.5	30.1	40.6	2.8	2.2	4.4	Х	Х	Х
	Г	ON	54.2	50.6	49.4	5.7	5.4	4.9	4.2	21.0	16.0	15.0



45 kW 1-Ph Load Between Phase A and B

DLB is OFF

DLB is ON



		IS (A)				IS	S THD (%	6)	IDLB (A)		
Test #	DLB	ISA	ISB	ISC	% Imb	ISA THD	ISB THD	ISC THD	IDLBA	IDLBB	IDLBC
Н	OFF	94.4	97.3	3.1	100.1	1.9	1.5	48.3	Х	Х	х
п	ON	62.6	54.6	56.1	8.5	6.3	5.4	5.6	57.0	50.0	51.0



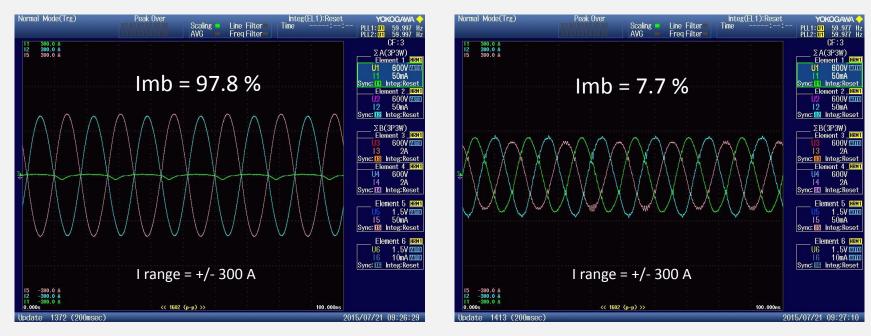
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45 kW 1-Ph Load Between Phase B and C

DLB is OFF

DLB is ON



			IS (A)				IS	STHD (%	%)	IDLB (A)		
	Test #	DLB	ISA	ISB	ISC	% Imb	ISA THD	ISB THD	ISC THD	IDLBA	IDLBB	IDLBC
	0	OFF	3.7	93.1	97.6	97.8	57.4	1.9	1.5	Х	Х	Х
	G	ON	57.6	61.2	54.1	7.7	5.0	5.7	3.9	51.0	51.0	57.0



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Summary and Conclusions

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- Growing introduction of Power Electronics and New Technologies in distribution systems as advanced mitigation solutions require in-depth testing and evaluations
- Traditional methods of testing approaches with the use of load bank and controlled sources may not be sufficient enough for comprehensive evaluation of technologies and integrated control/communication functionalities
 - Need to incorporate realistic system conditions and transient events
 - Flexibility in changing power system parameters and using validated circuit models
 - Applying large number of test cases involving contingencies and ability to repeat the tests
- PHIL & CHIL tests have been successfully utilized with superior results to alternative testing approaches and have been able to avoid high cost of experimenting in the field



Thank YOU



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