High Speed Digital Distance Relaying Scheme using FPGA and IEC 61850

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Outline

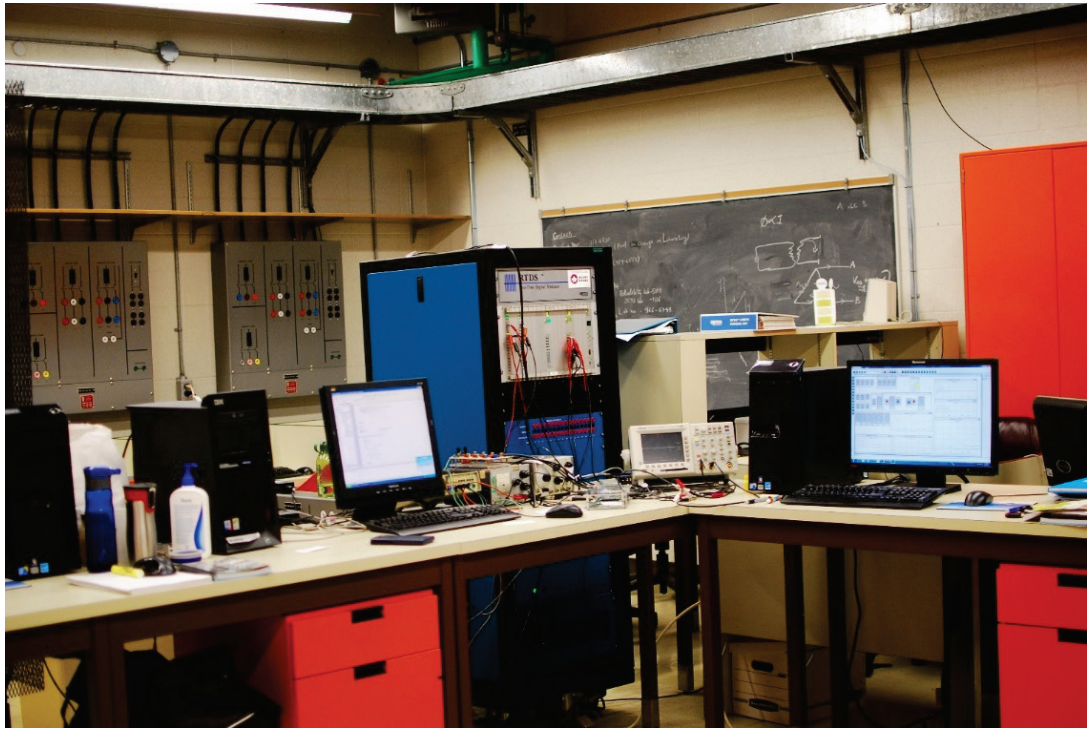
- Introduction
- Phaselet-based Distance Relay
- Hardware Implementation
- Test Platform
- Results
- Summary

Real Time Simulation Lab

Group Lead: Prof. Rama Gokaraju

Real Time Digital Simulator (RTDS)

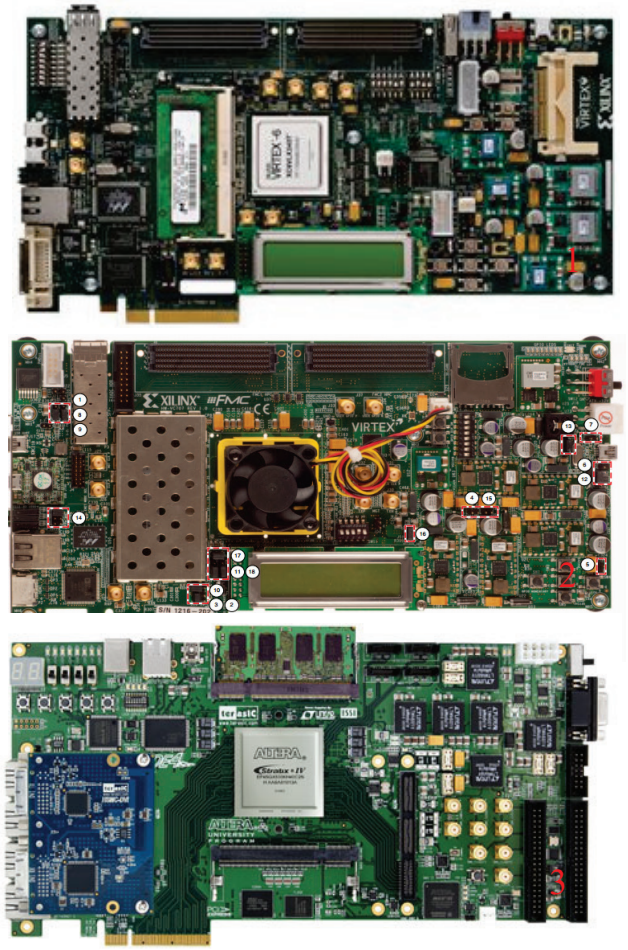
- 6 Processor Cards (4 GPC + 2 PB5)
- 2 GTNET Network Interface Cards
- Support: IEC 61850 (SV, GOOSE), DNP3, PMU(24 units max), Playback
- GTFPGA Firmware
- GTAI/GTAO



IEDs & Others

1.SEL 411L Advanced Line Differential Relay
2.GE L90 Line Differential Relay
3.GE D60 Line Distance Relay
4.GE F60 Feeder Protection Relay
5.SEL 2407 GPS Clock
6.Techron Amplifier

Field Programmable Gate Arrays (FPGA)



1.Xilinx Virtex-6 FPGA ML605 Evaluation Board

2.Xilinx Virtex-7 FPGA VC707 Evaluation Board

3.Altera DE4 Development Board

Current Projects

- **High Speed Digital Protection**
- Power System Stability Analysis Using Wide Area Measurement System
- Wind Generator Modeling
- Fault Location in PV system/Wind Farm

Introduction: Motivation

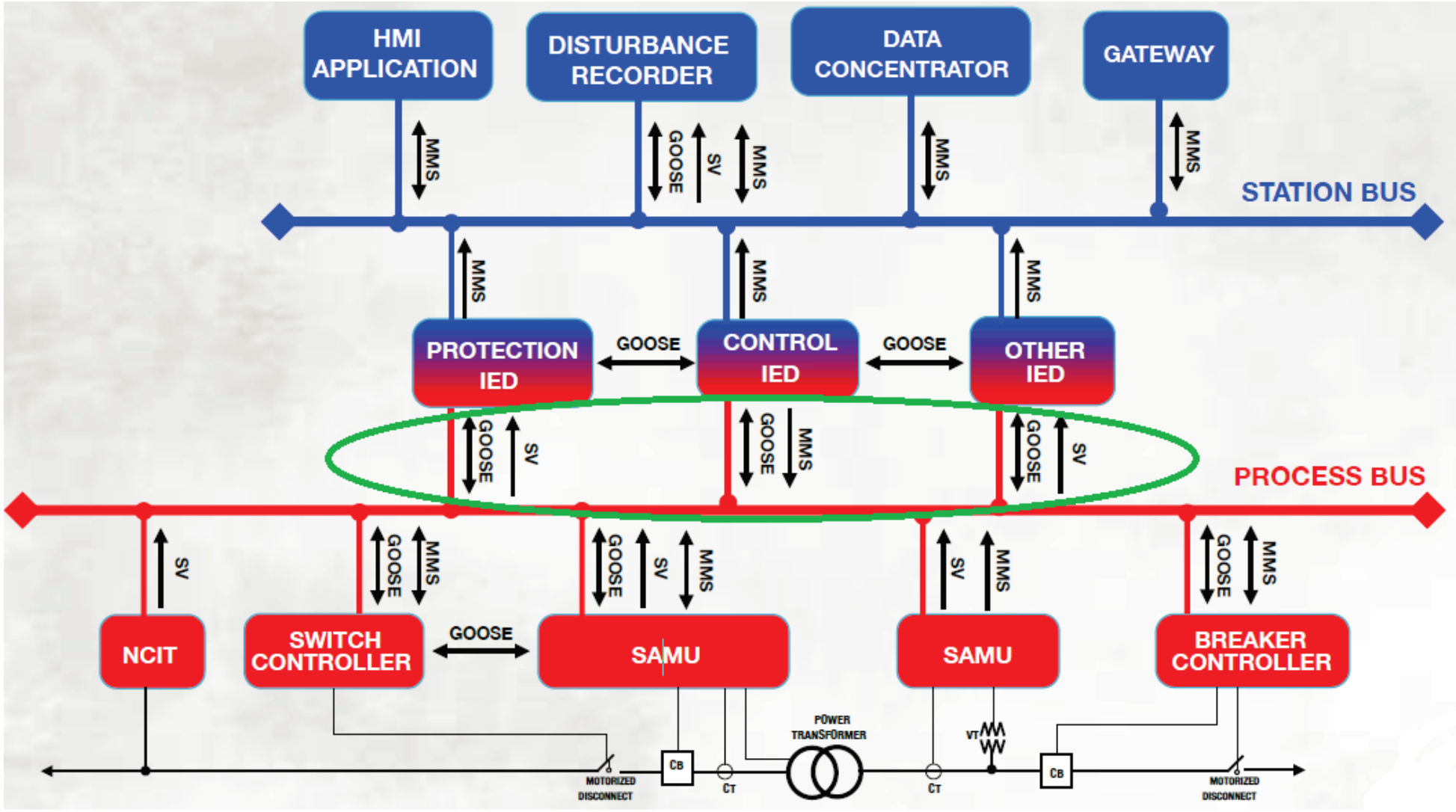
State-of-art numerical relay: 1 power cycle (16.667 milliseconds)

Gap

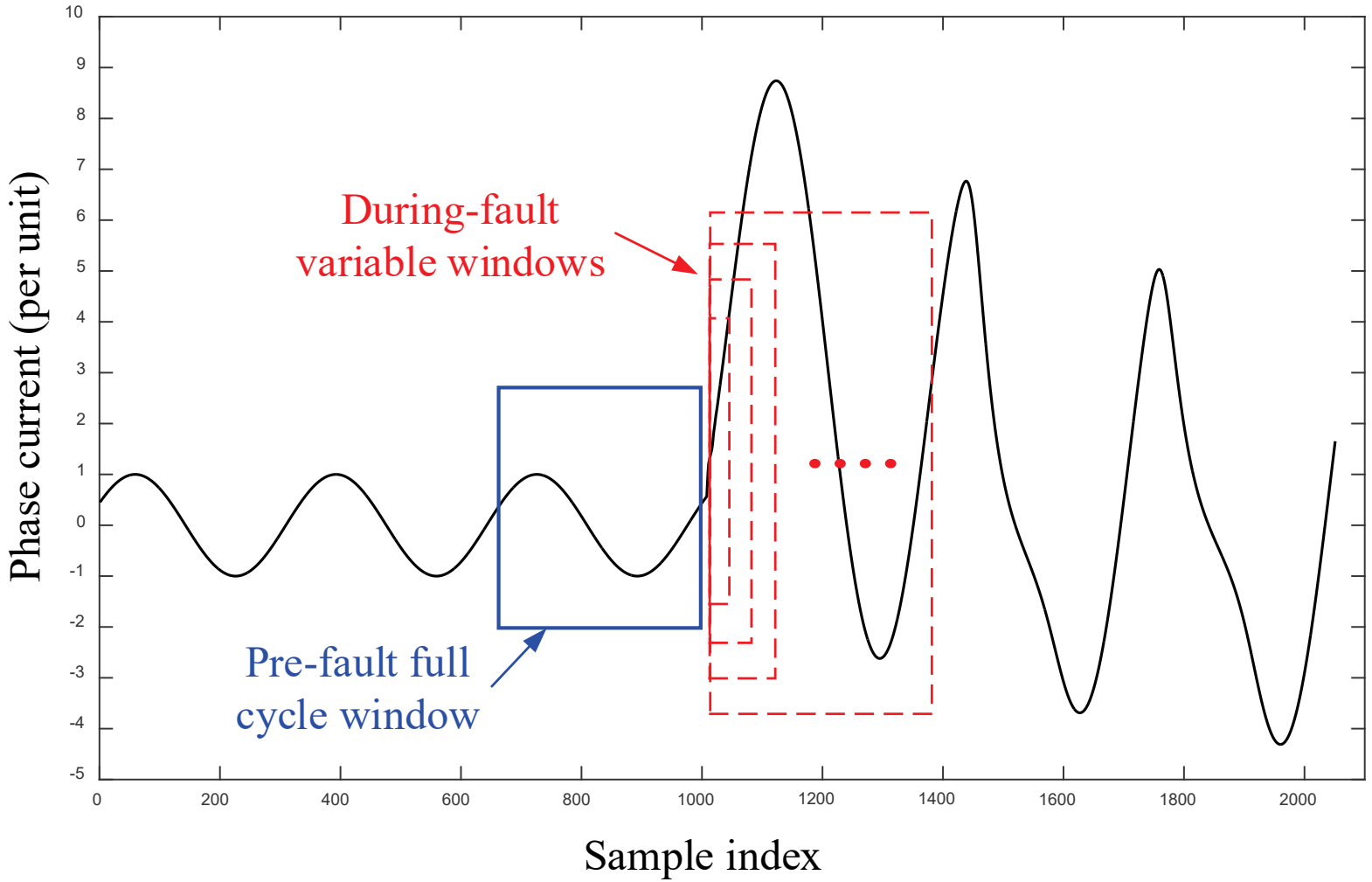
- Extra high voltage EHV/EHV transmission system requires sub-cycle (~10 milliseconds)
- 1 ms early detection: stability limit goes up by ~15 MW[1]
- Solid state relay: 0.25~0.5 cycle
- Circuit breaker technology: 0.5~1 cycle

[1] E. O. Schweitzer, B. Kasztenny, A. Guzm?an, V. Skendzic, and M. V. Mynam, "Speed of line protection - Can we break free of phasor limitations?" in 68th Annual Conference for Protective Relay Engineers, pp. 448-461, 2015.

Introduction: Motivation



Algorithm: Variable Filtering Window



Algorithm: Phaselet

$$X_r = \frac{2}{N}\sum_{k=0}^{N-1} x(k) * \cos(2\pi\frac{k}{N}),$$

$$X_i = \frac{2}{N}\sum_{k=0}^{N-1} x(k) * \sin(2\pi\frac{k}{N}),$$

P is a factor of N.
For example: N=80 while P =4.

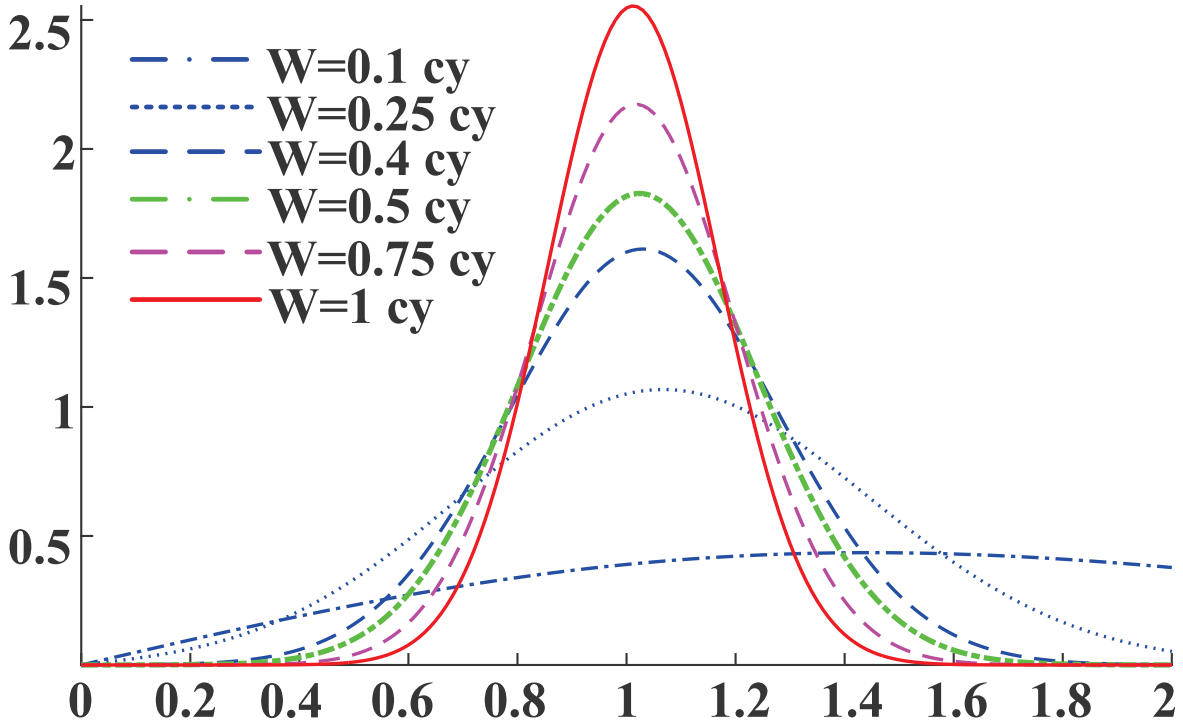
$$Pl_r = \frac{2}{\cancel{N}}\sum_{k=0}^{\boldsymbol{P}-1} x(k) * \cos(2\pi\frac{k}{N}),$$

$$Pl_i = \frac{2}{\cancel{N}}\sum_{k=0}^{\boldsymbol{P}-1} x(k) * \sin(2\pi\frac{k}{N}),$$

[1] M. Adamiak and W. Premerlani, “A new approach to current differential protection for transmission lines,” in Electrical Council of New England Protective Relaying Committee Meeting, October 1998.

Algorithm: Magnitude Error

Probability density function (PDF) for magnitude error: $f(r) = \frac{2r}{R} e^{\frac{-(r^2+\bar{r}^2)}{R}} I_0(\frac{2\bar{r}r}{R})^1$

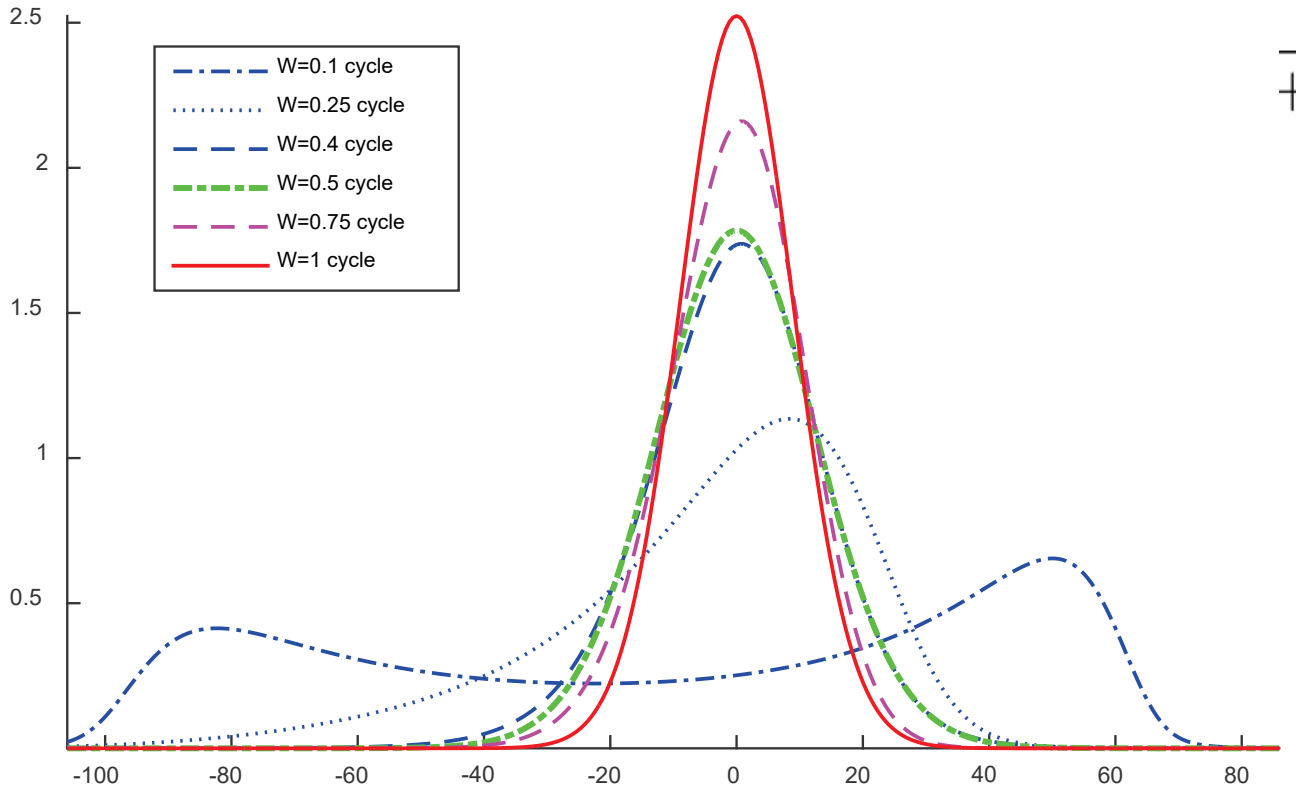


[1] S. Jin, R. Gokaraju, R. Wierckx, and O. Nayak, "High speed digital distance relaying scheme using FPGA and IEC 61850," IEEE Trans. on Smart Grid, early access, 2017 .

Algorithm: Phase Angle Error

Probability density function (PDF) for phase angle error: $f(\theta) = \frac{e^{-g}\left\{1+\sqrt{\pi}\xi e^{\xi^2}[1+erf(\xi)]\right\}^1}{4\pi\sigma_c\sigma_s\sqrt{1-\rho^2}}$

$$\frac{1}{+ucos2\theta+vsin2\theta},$$



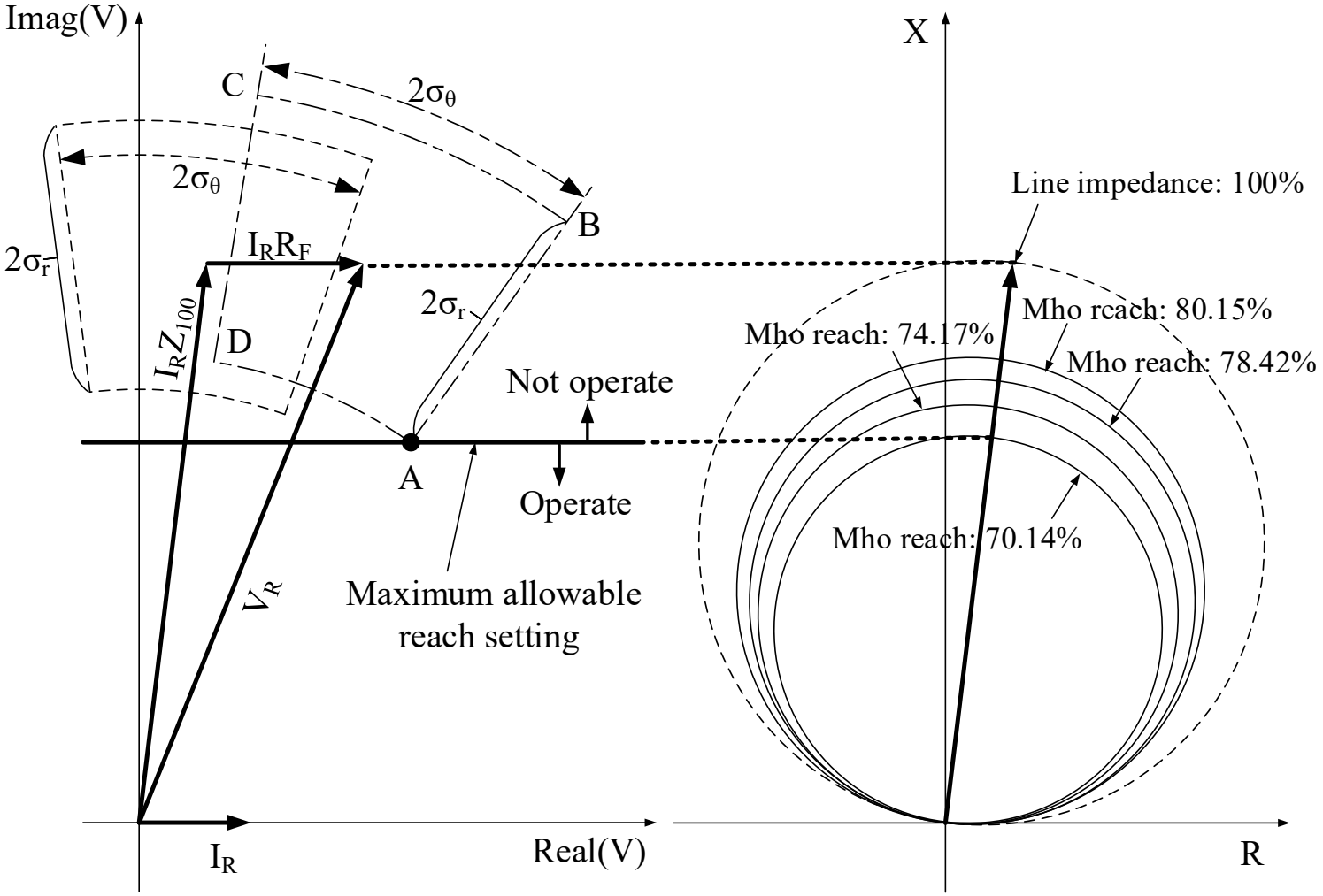
[1] S. Jin, R. Gokaraju, R. Wierckx, and O. Nayak, "High speed digital distance relaying scheme using FPGA and IEC 61850," IEEE Trans. on Smart Grid, early access, 2017 .

Algorithm: Standard Deviation

STANDARD DEVIATION AND REACH SETTING UNDER DIFFERENT FILTERING WINDOWS

$w(cy)$	0.45	0.5	0.6	0.7	0.8	0.9	1
$\sigma_r(n)$	22.9%	21.8%	20.3%	19%	17.7%	16.5%	15.6%
$\sigma_\theta(n)$	13.4^o	13.1^o	12.6^o	11.5^o	10.2^o	9.4^o	9.2^o
$reach$	70.1%	72.4%	74.2%	74.7%	76.3%	78.4%	80.2%

Algorithm: Combine Magnitude and Angle error



(a) Magnitude and angle error impact on current and voltage phasor (window=0.45 cycle)

(b) Resulting adaptive Mho characteristics

Algorithm: Adaptive Reach Setting

STANDARD DEVIATION AND REACH SETTING UNDER DIFFERENT FILTERING WINDOWS

$w(cy)$	0.45	0.5	0.6	0.7	0.8	0.9	1
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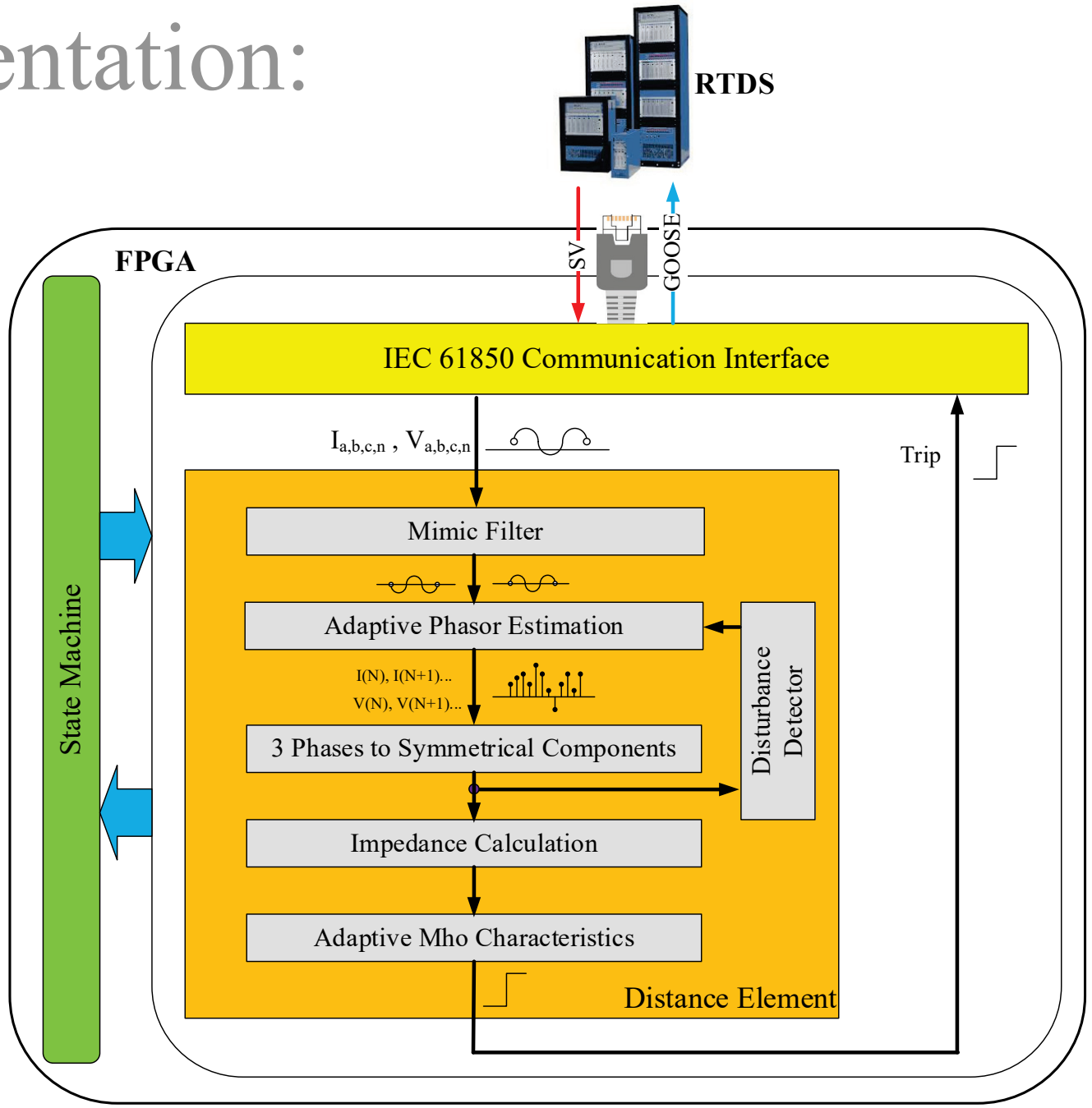
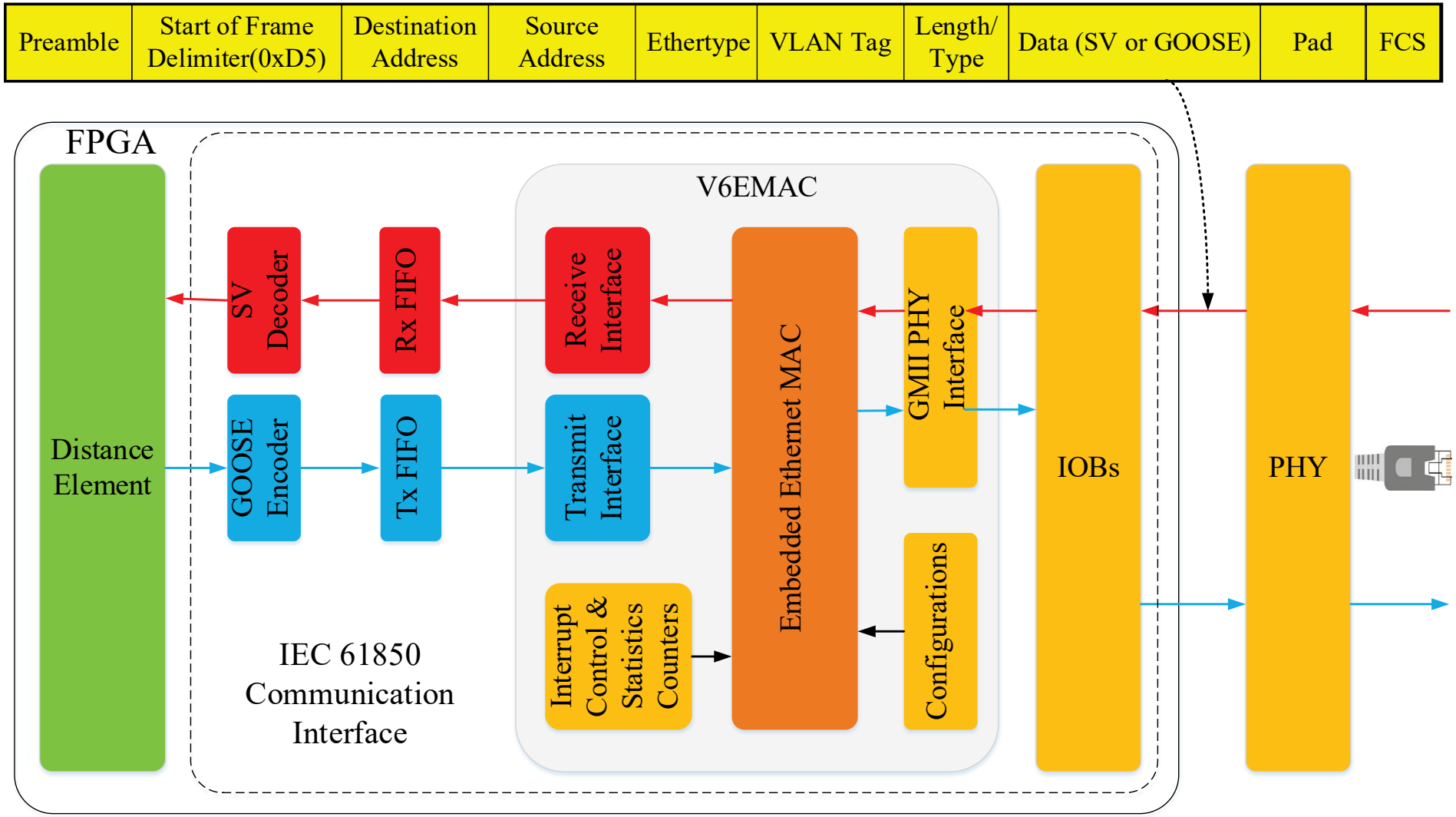
Hardware Implementation:
Overall

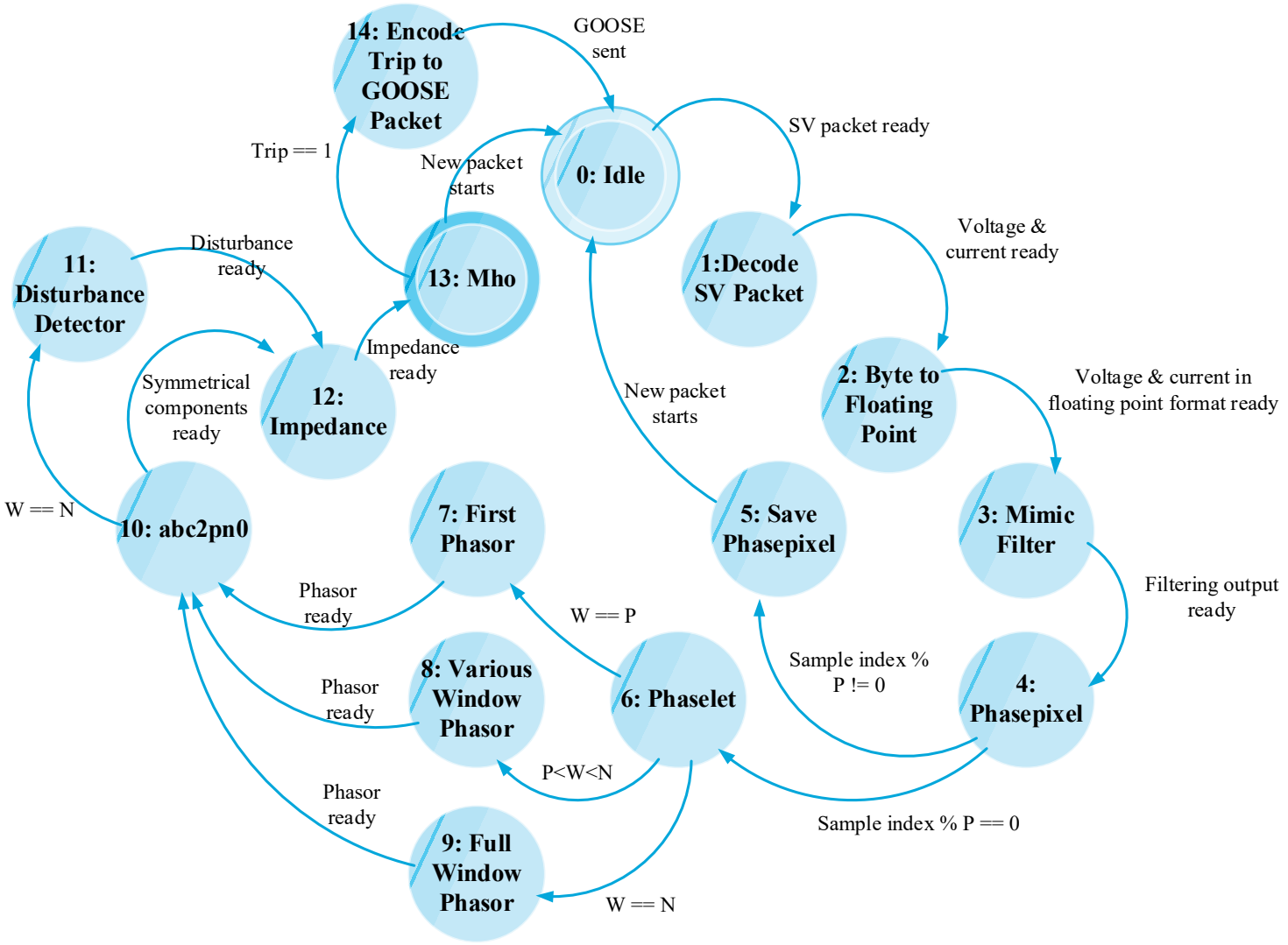
- IEC 61850 Communication
- Distance Element
- State Machine (global control)



Hardware Implementation: IEC 61850



Hardware Implementation: State Machine

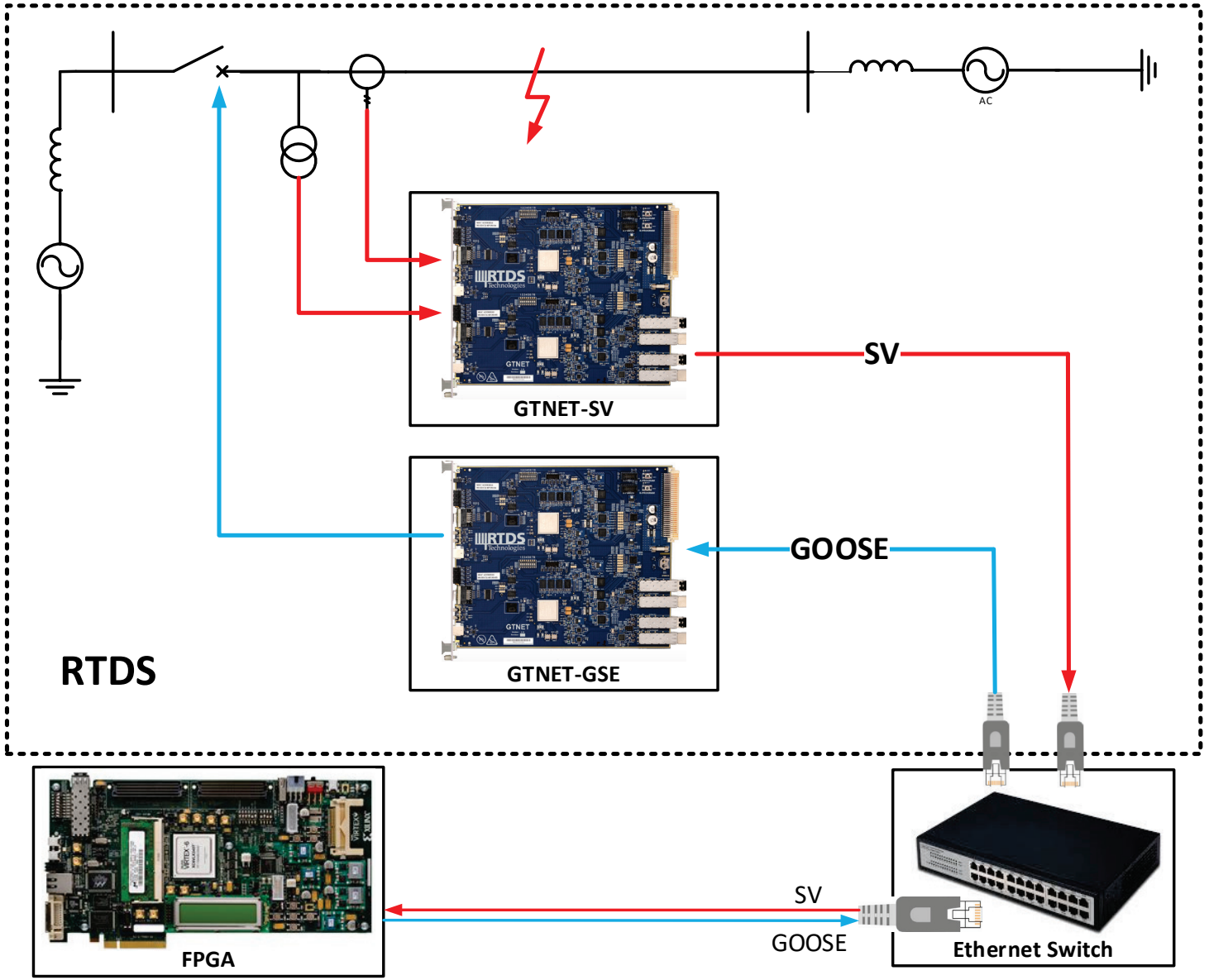


Hardware Implementation: Resource Utilization

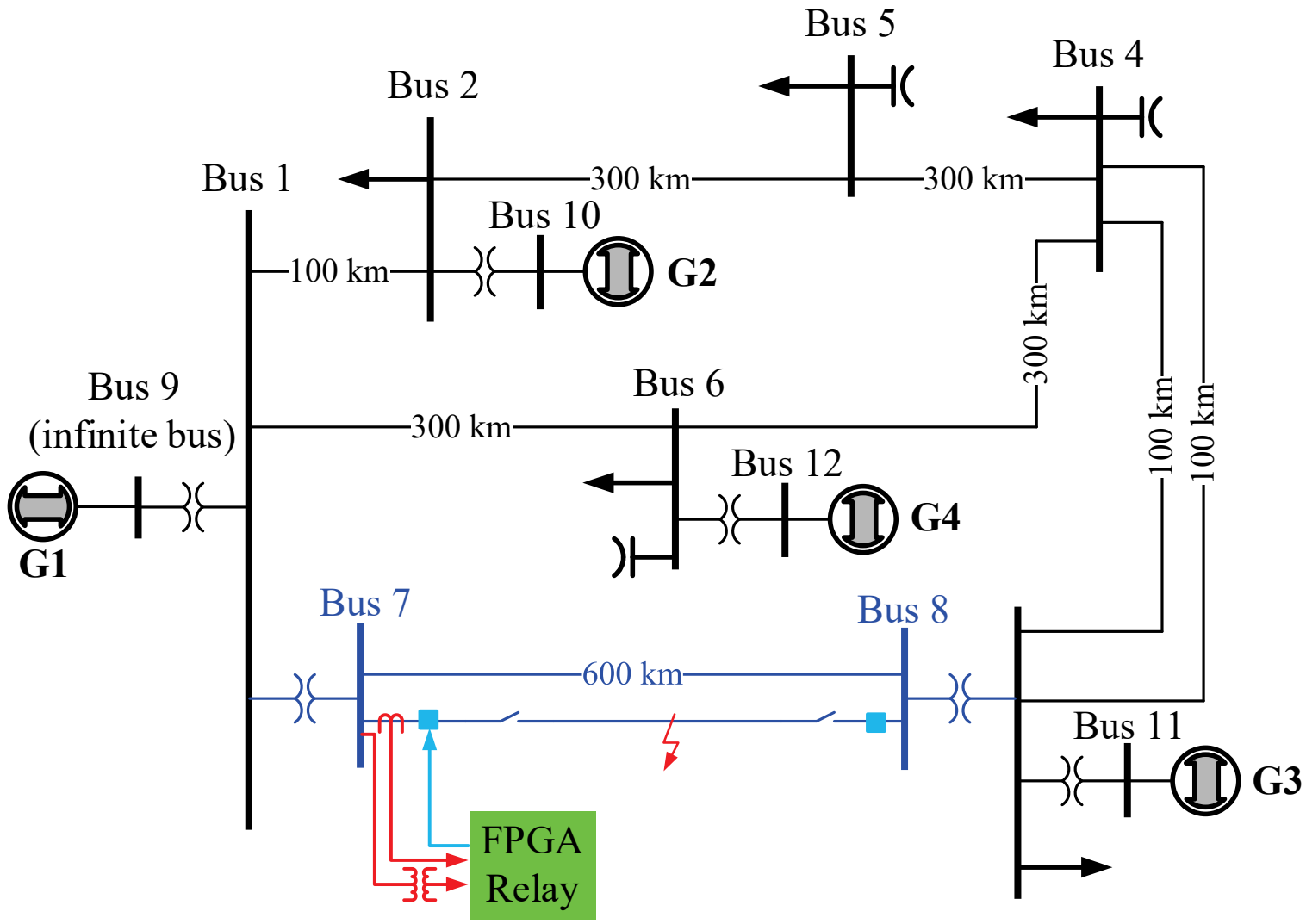
FPGA HARDWARE RESOURCES UTILIZATION

Resources	Slice Registers	Slice LUTs	DSP Blocks
Available	301440	150720	768
Usage	149279 (49.5%)	111258 (73.8%)	526 (68.5%)

Test Platform: Overview

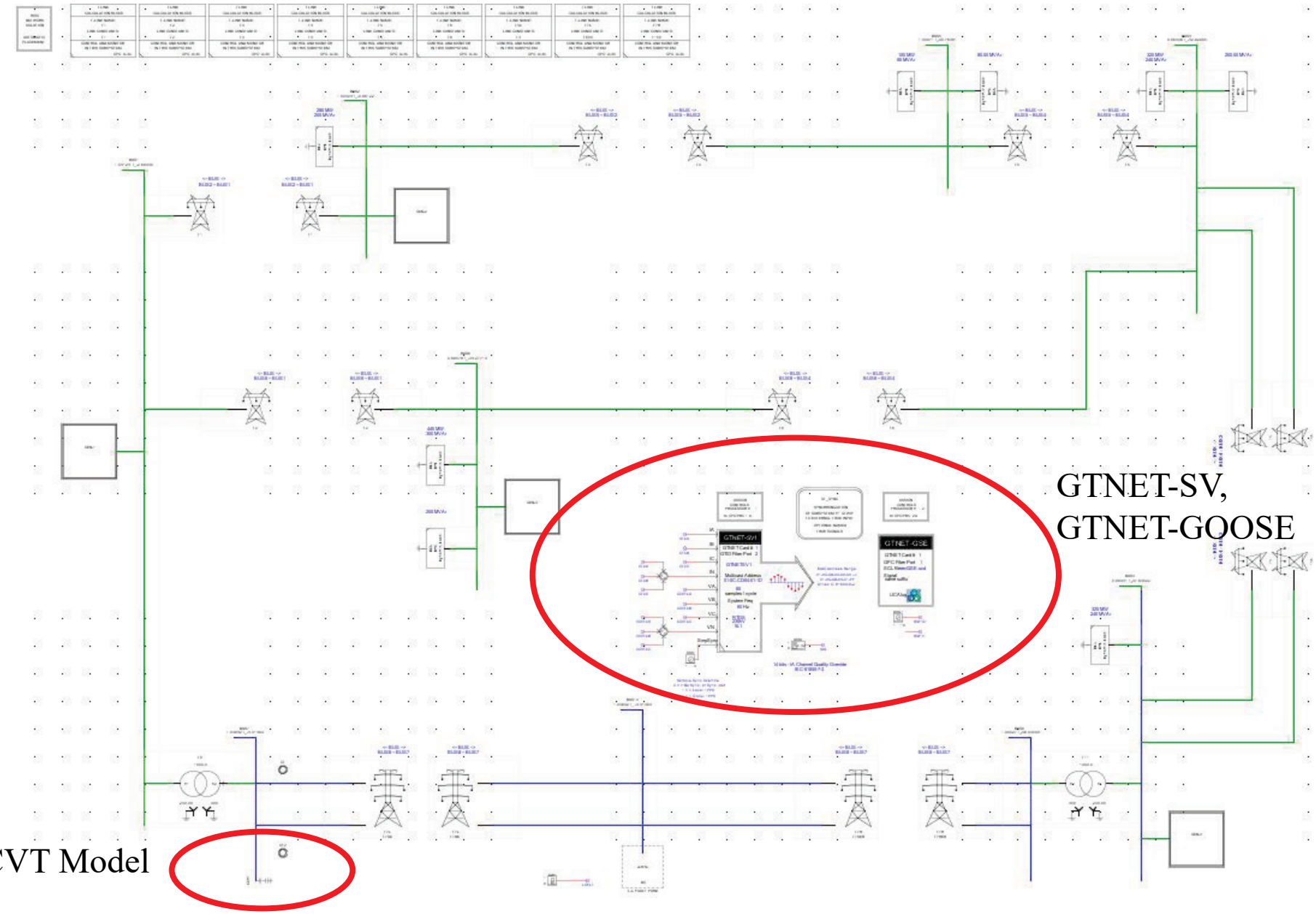


Test Platform: IEEE 12 Bus System[1]

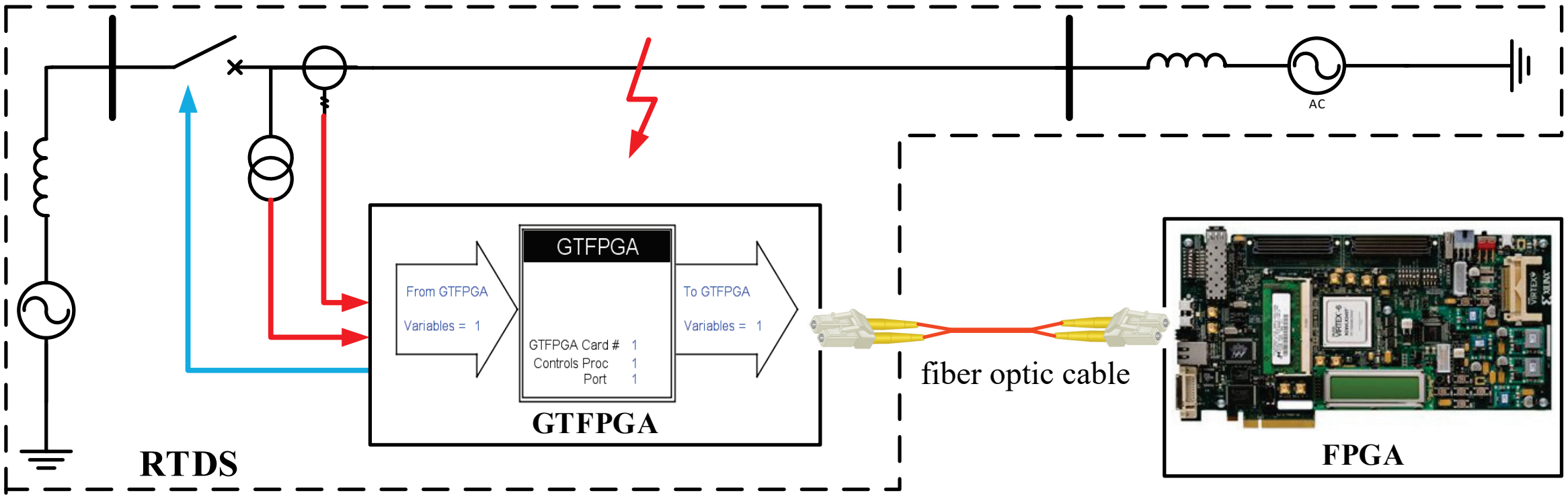


[1] S. Jiang, U. D. Annakkage and A. M. Gole, "A platform for validation of facts models," IEEE Transactions on Power Delivery, vol. 21, no. 1, pp. 484–491, 2006.

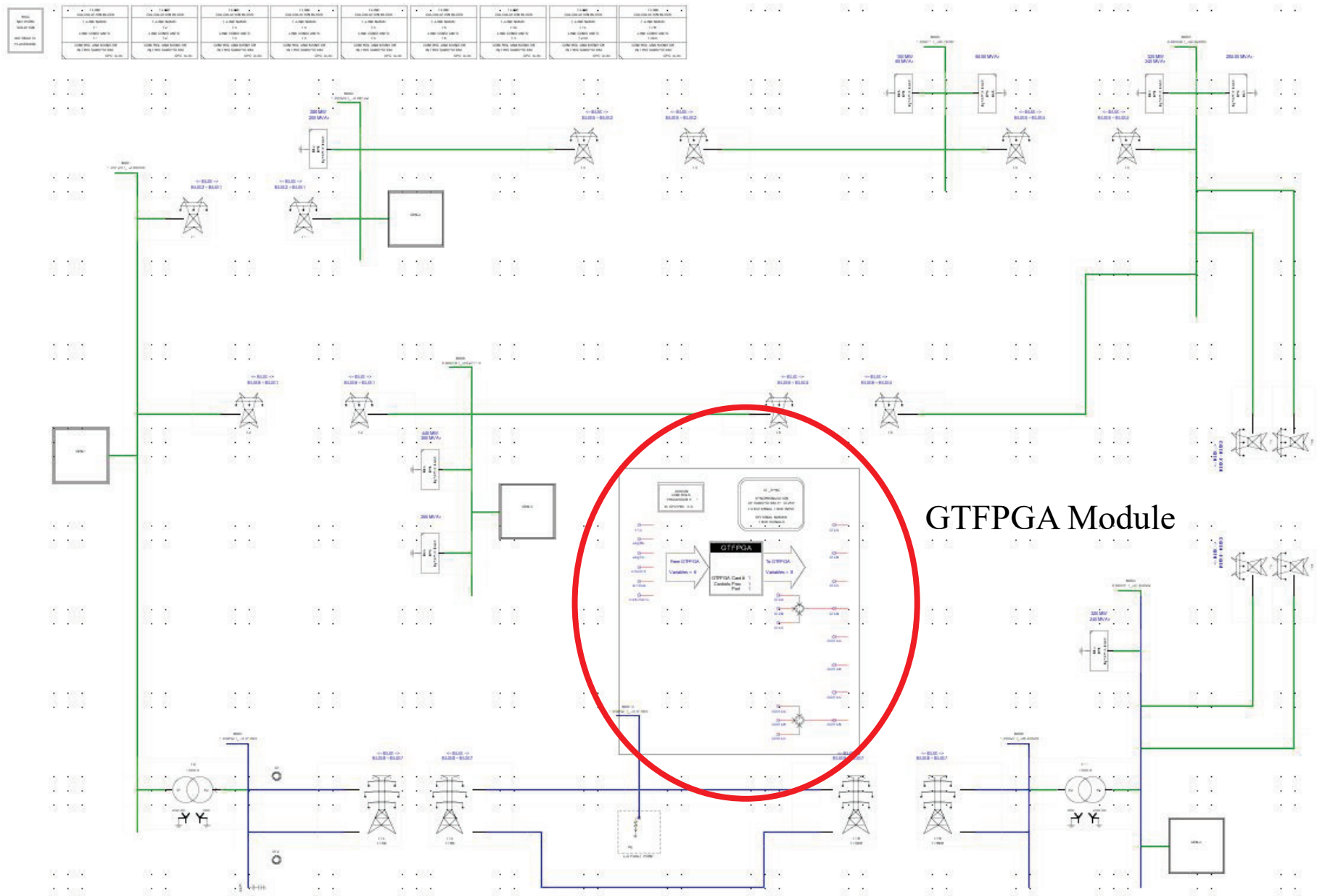
Test Platform: RTDS Model



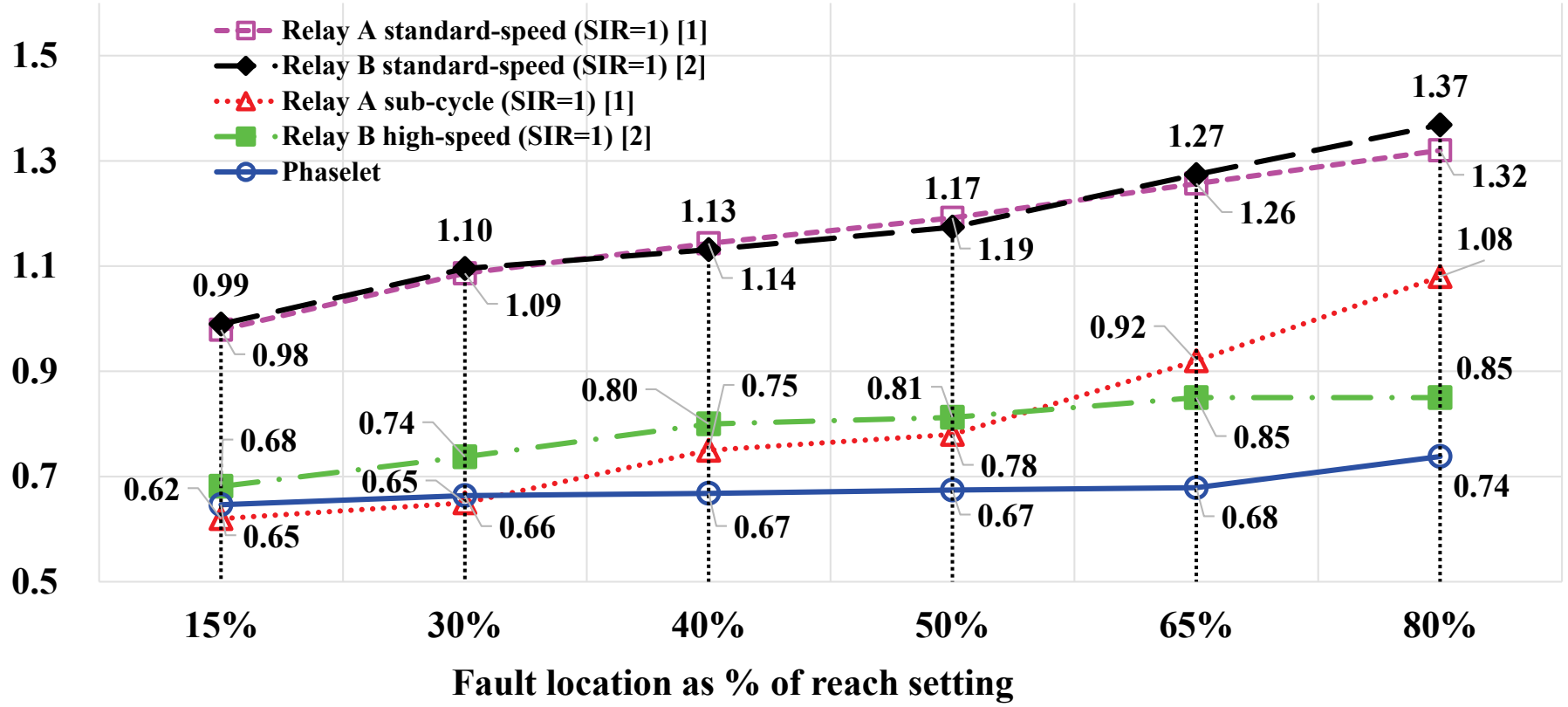
Test Platform: GTFPGA



Test Platform: GTFPGA

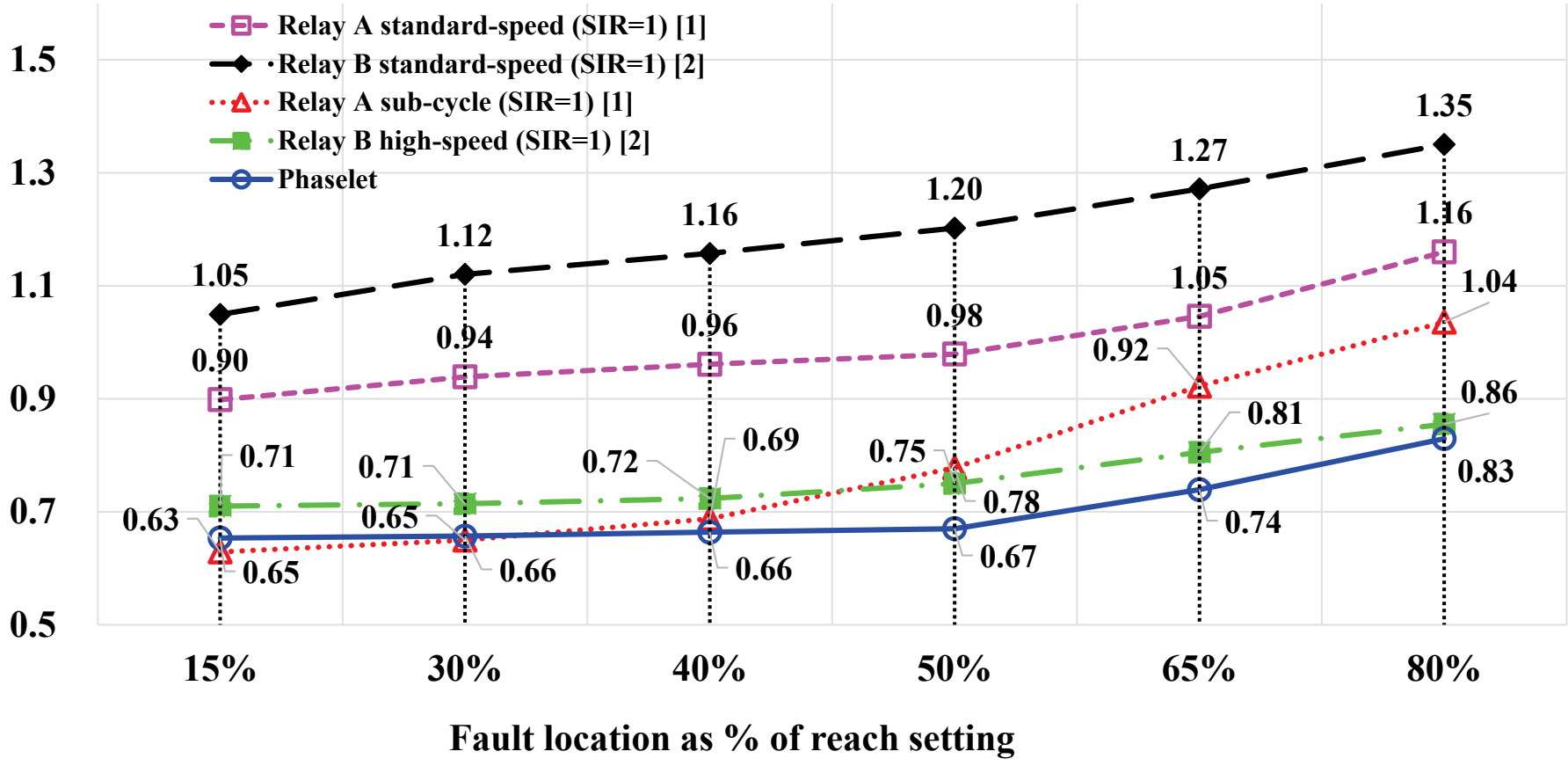


Results: Speed: L-G Faults



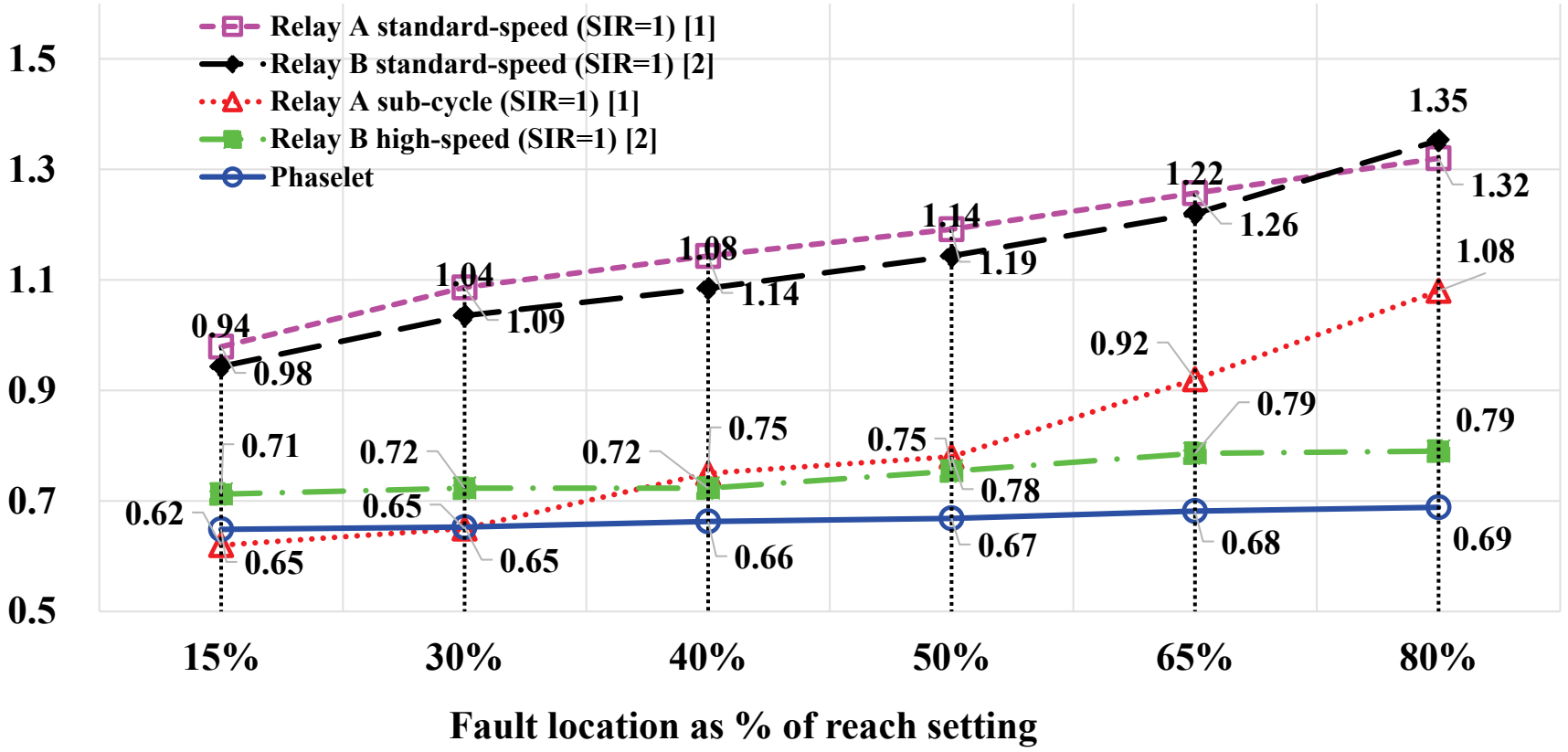
[1] GE Digital Energy, D90 plus line distance protection system instruction manual, 2013.
[2] Schweitzer Engineering Laboratories, SEL-421-4, -5 protection and automation system data sheet, May 2015.

Results: Speed: L-L Faults



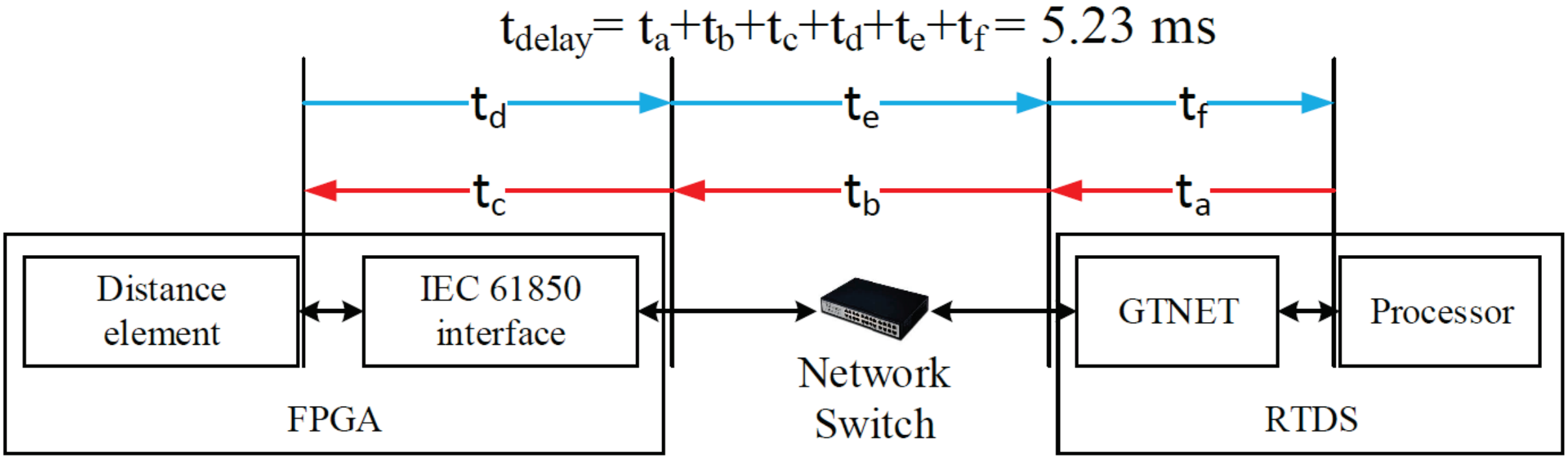
[1] GE Digital Energy, D90 plus line distance protection system instruction manual, 2013.
[2] Schweitzer Engineering Laboratories, SEL-421-4, -5 protection and automation system data sheet, May 2015.

Results: Speed: 3-phase Faults



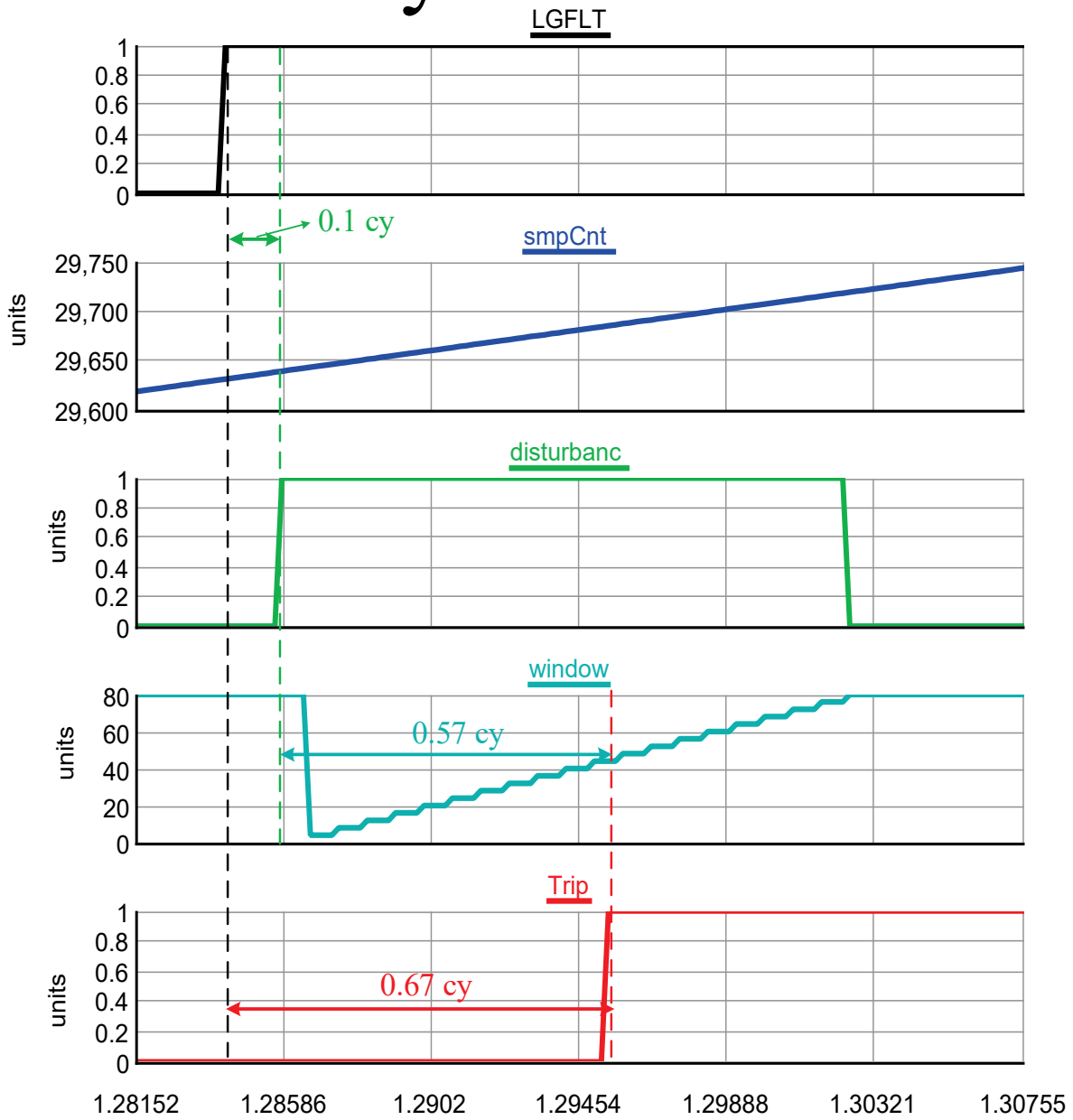
[1] GE Digital Energy, D90 plus line distance protection system instruction manual, 2013.
[2] Schweitzer Engineering Laboratories, SEL-421-4, -5 protection and automation system data sheet, May 2015.

Results: SV/GOOSE Latency



Results: GTFPGA Latency

- Consistent with that from IEC 61850
- The communication latency of GTFPGA is negligible. 400 ns?



Fault location: 50%
Inception angle: 30°

Results: Reliability

Incorrect Tripping Probability

# of lines	Single line			2 lines
Method	FCDFT	**Phaselet-no consideration of phase angle error**	**Phaselet**	Phaselet
Line-ground	0%	**8%**	**2%**	0%
Line-line	0%	**8%**	**1%**	0%
Three-phase	0%	**0%**	**0%**	0%

Summary

- **Phase angle error analysis** is proved to be equally important as the magnitude error. The proposed adaptive Mho characteristic can improve relay reliability.
- FPGA relay has the advantage of speed:
  - make secure trip decision in 0.6~0.8 cycles
  - processing time for each SV packet is 4.04 μs
- **IEC 61850** communication latency is ~5.23 *ms* (2-way). It matches the standard criteria (specified in IEC 61850-5, Type 1A, Class P2/3 messages, 3 ms for one way).
- GTFPGA latency is negligible when paired with external FPGA device.

Acknowledgement

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- Mr. Om Nayak, Nayak Corporation.
- Prof. Rama Gokaraju
- Financial support from RTDS Technologies Inc. & NSERC Engage

Thank you!

Q & A