RTDS-FPGA-based real-time simulation platform for modern power systems

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Outline

1-Introduction

2- FPGA-based simulation of power network

3- Simulation of Power Electronic Converters (PECs)

4- Simulation of Electrical Machines (EMs)

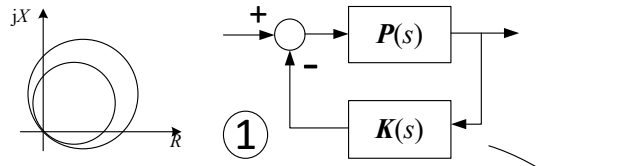
5- Parallel simulation between RTDS and FPGA

6- Real-time simulation platform

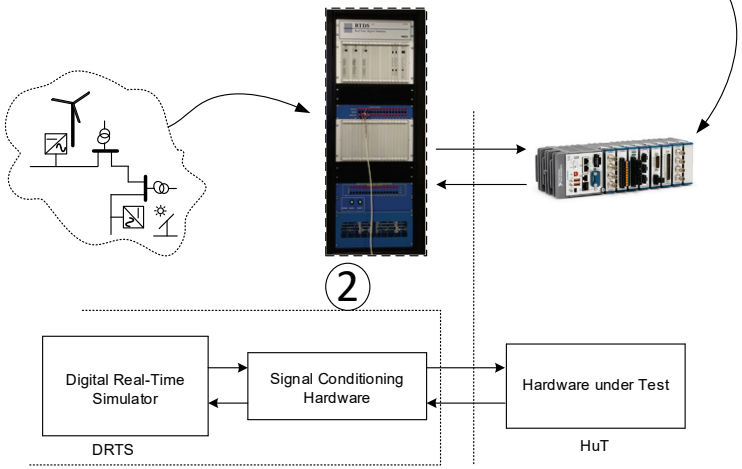
Introduction

Real-time simulation application
Hardware-In-the-Loop (HIL) test for power systems control/protection:

1- Algorithm Development



2- HIL test verification



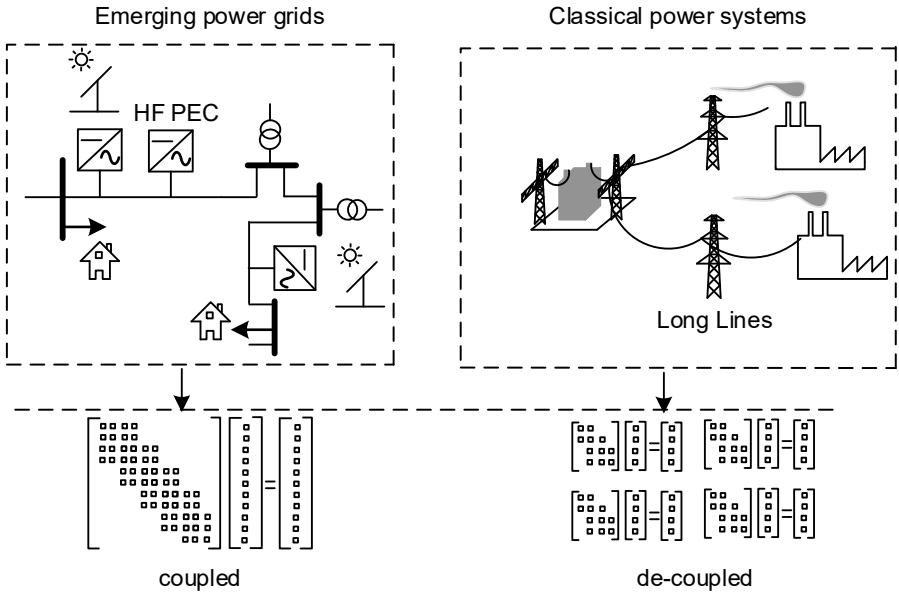
3- Field installation

Statement of the problem

HIL tests are necessary for modern power system, e.g., microgrids

Real-time simulation challenges:

1- Simulating a **large coupled network** using **small time-steps**



Structure of network equations for EMT simulation

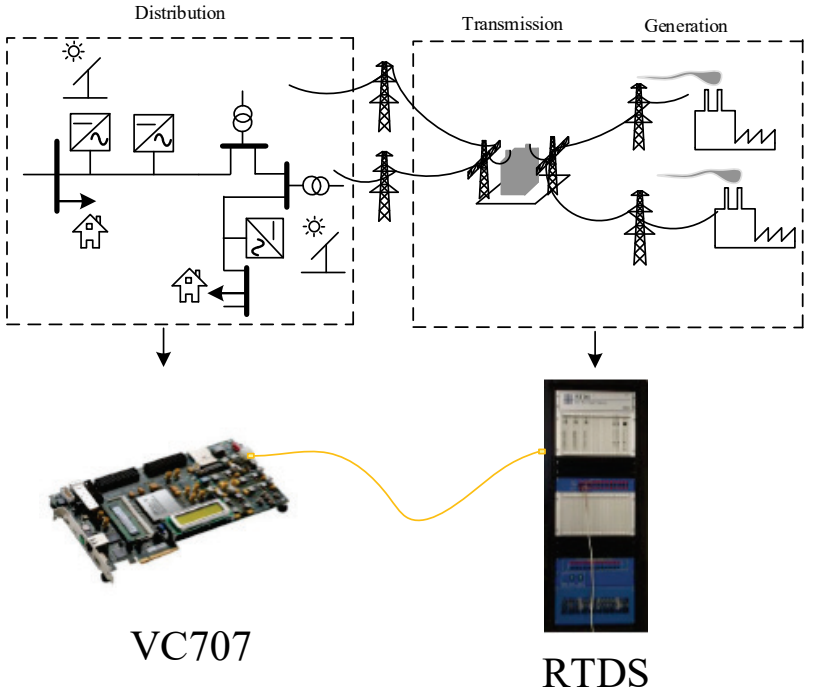
2- **Accurate representation** of component models especially **PECs**

3- **Floating-point** arithmetic is required

Objectives

- Real-time simulation of **large networks** using **small time-step (*μ*s-range)**
- Precise representation of **PEC**s
- Precise representation of **EM**s
- Using **Universal Line Model** for **parallel simulation**

parallel simulation for power system application



-**Fixed hardware** design

-Using standard **floating-point** arithmetic

2- FPGA-based simulation of power network

Conventional network formulation based on Modified Nodal Analysis (MNA) 4 tasks:

1- Independent source calculation

2- RLC history current calculation

3- Subsystem history calculation

$$\underbrace{\begin{bmatrix} G & A_g \\ B_g & 0 \end{bmatrix}}_{Y} \underbrace{\begin{bmatrix} v^{n+1} \\ i_{vs}^{n+1} \end{bmatrix}}_{x_{node}^{n+1}} = \underbrace{\begin{bmatrix} u_i^{n+1} \\ v_s^{n+1} \end{bmatrix}}_{u_{node}^{n+1}}$$

4- Solution of the equations $x_{node}^{n+1} = Y^{-1} u_{node}^{n+1}$

Structure of u_{node}^{n+1}

- **prevents Prallelism**

  The solution of the network (4) can not be started until first three (1,2,3) tasks are done.

- **prevents fixed hardware design**

  It depends on the network topology

Proposed FPGA-based formulation of network equations

RMNA formulation

$\mathbf{K_{SI}}$**:** node incidence matrix

$$\mathbf{b}_{node}^{n+1} = \begin{bmatrix} \mathbf{b}_s^{n+1} \\ \mathbf{i}_h^{n+1} \\ \mathbf{b}_{ss}^{n+1} \end{bmatrix} = \mathbf{K}_{SI}\mathbf{u}_{node}^{n+1}, \qquad \mathbf{x}_{node}^{n+1} = \mathbf{H}_{RMNA}\mathbf{b}_{node}^{n+1}, \qquad \mathbf{H}_{RMNA} = \mathbf{K}_{SI}\mathbf{Y}^{-1}.$$

Advantages of RMNA:

-enables **fixed hardware (**It does **not depend** on the **topology)**

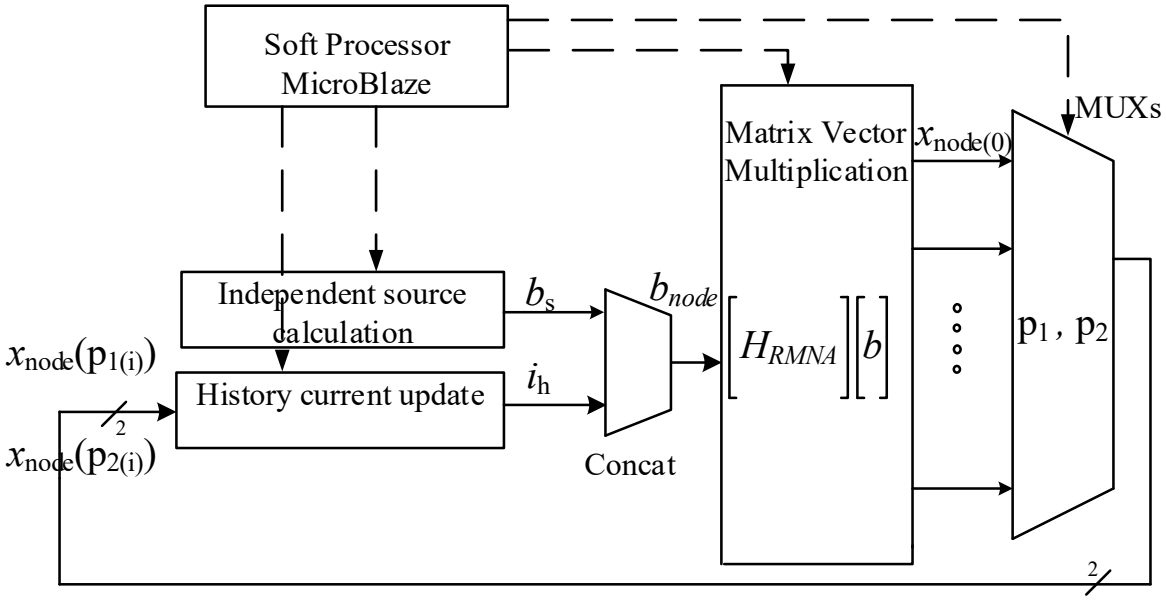
-Parallelism

-Appropriate scheduling of tasks based on**:**

-Input **data requirement** from previous time-step

-the **latency** of the their modules

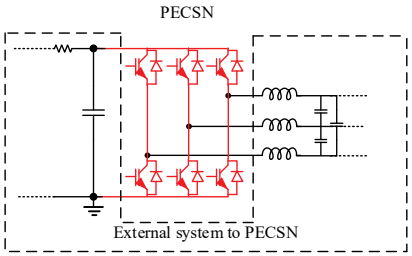
Proposed architecture based on RMNA



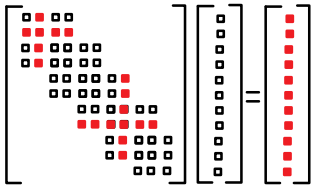
3- Proposed Partitioning method for PEC simulation

Challenge:

Using precise two-value resistor model



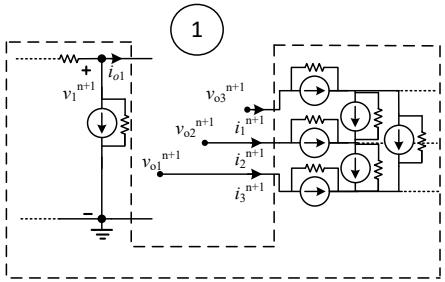
Structure of the discretized equations



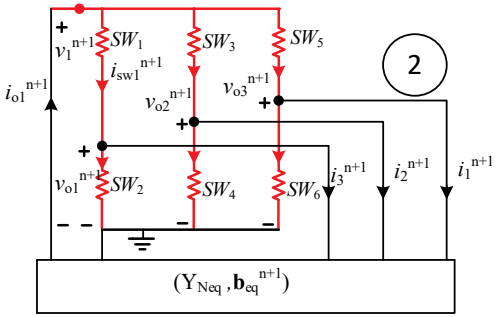
- Time-variant
- Fixed

Partitioning method:

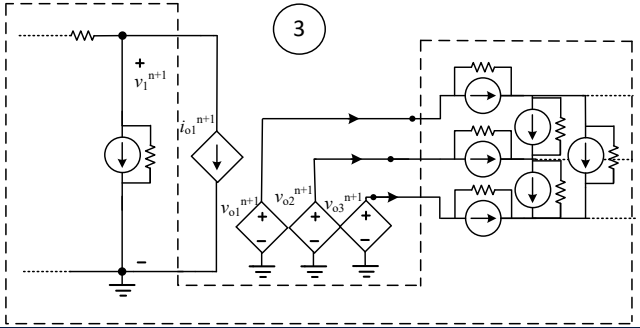
1- Finding the equivalent circuit



2- Solving the equations of each PECSN



3- Using terminal variables as sources in solution of network equations.



Implementation of proposed Partitioning method

step1

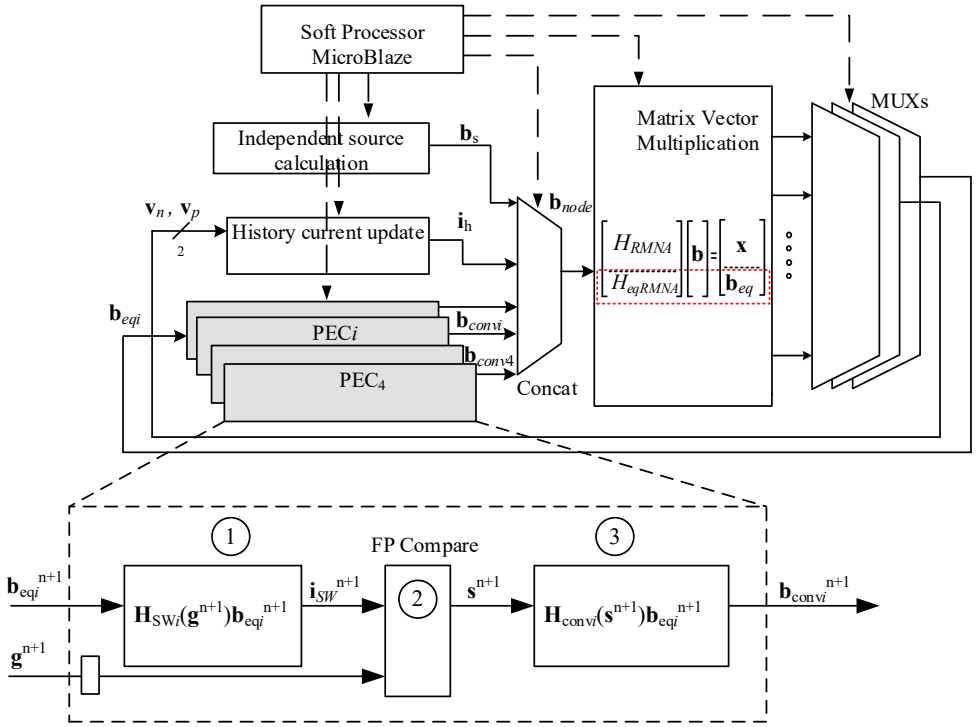
$$\begin{bmatrix} \mathbf{x}_{node}^{n} \\ \mathbf{b}_{eq1}^{n+1} \\ \vdots \\ \mathbf{b}_{eqm}^{n+1} \end{bmatrix} = \begin{bmatrix} \mathbf{H}_{RMNA} \\ \mathbf{H}_{eqRMNA1} \\ \vdots \\ \mathbf{H}_{eqRMNAm} \end{bmatrix} \mathbf{b}_{node}^{n}.$$

step2

-Needs a separate hardware, **PEC module**

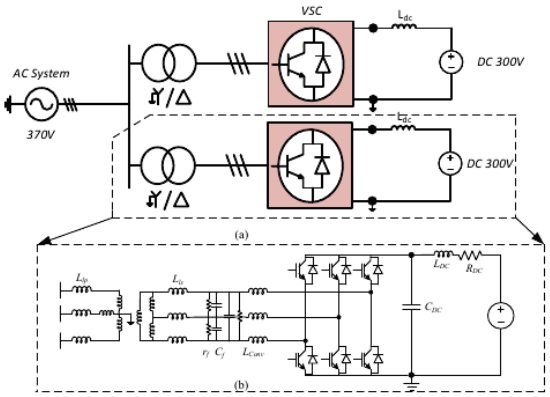
step3

Needs modifying the concat module

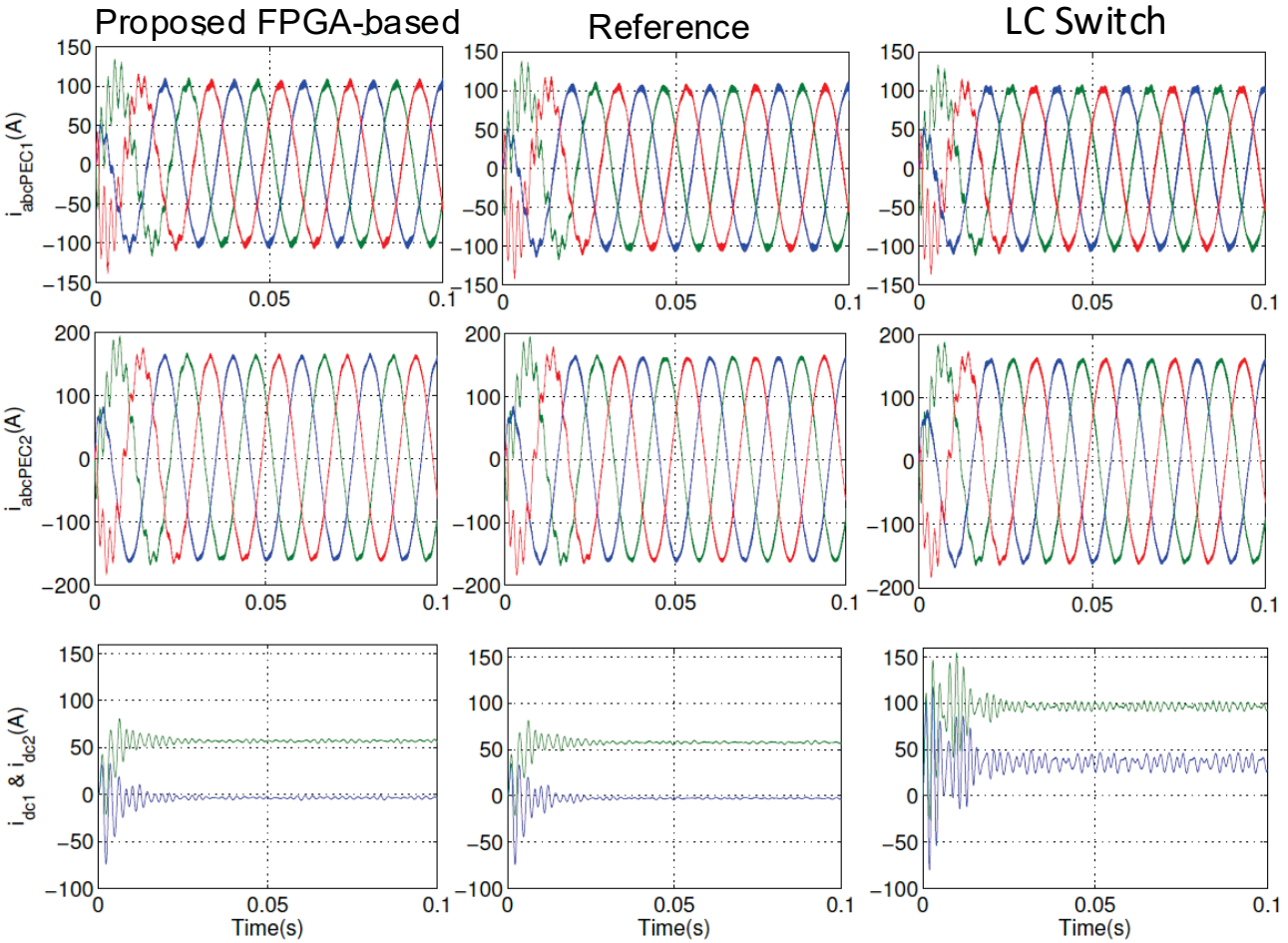


Verification of the proposed partitioning method

Scenario: Start-up

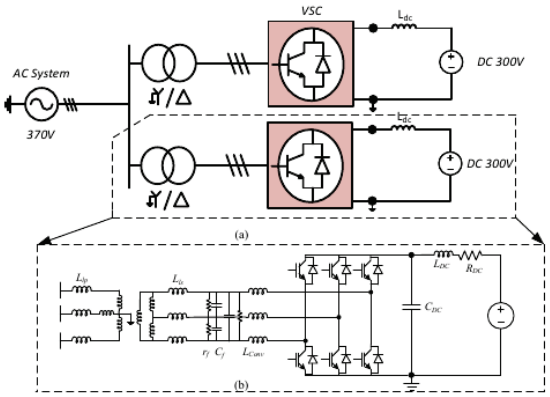


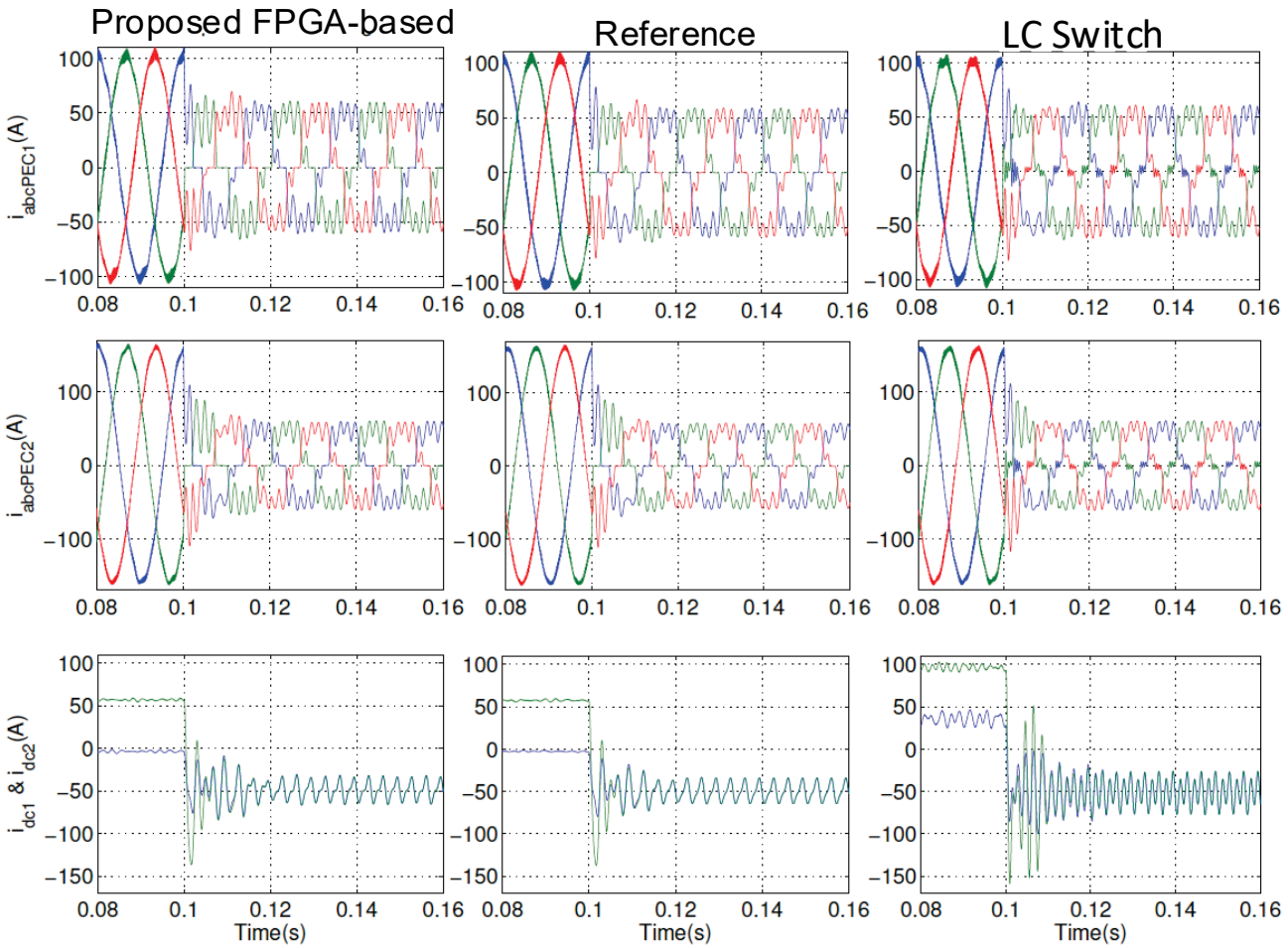
F_{sw}=5kHz
Δt=2μs



Verification of the proposed partitioning method

Scenario: Gate blocking @t=0.1s





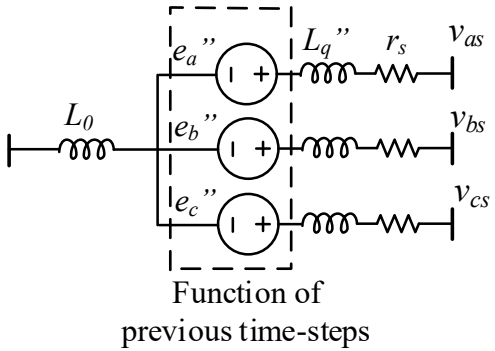
4- Proposed Electrical Machine (EM) model

Proposed Constant-Parameter-Voltage-Behind-Reactance (CPVBR) for EMs regardless of L_q"/L_d"

Implicit stiff LMS integration method

$$x^{n+1} + (a-2)x^n + (1-a)x^{n-1} = \Delta t\, a\, f(x^{n+1}, t^{n+1}), \quad 0 < a \leq 1,$$

CPVBR model **interface** for **IM, SM, PMSM**



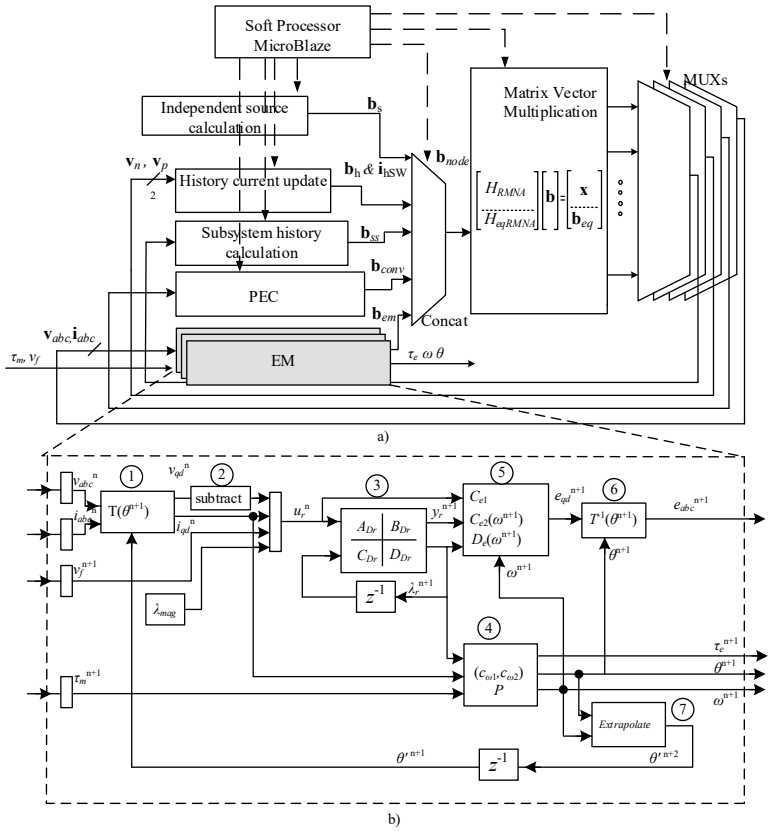
EM simulation task: calculation of voltage sources e_a", e_b" and e_c"

-In **parallel** with the rest of the tasks

Implementation of the proposed CPVBR EM model

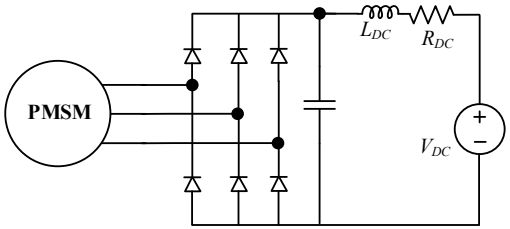
Features of the EM module:

- It has **fixed hardware** and can represent **SM**, **PMSM** and **IM** (up to 2 windings on each axis)
- Each EM module require **<2% of FPGA resources**
- It can simulate EMs **regardless of system configuration** and **EM dynamic saliency**
- It is in **parallel** with the rest of the modules

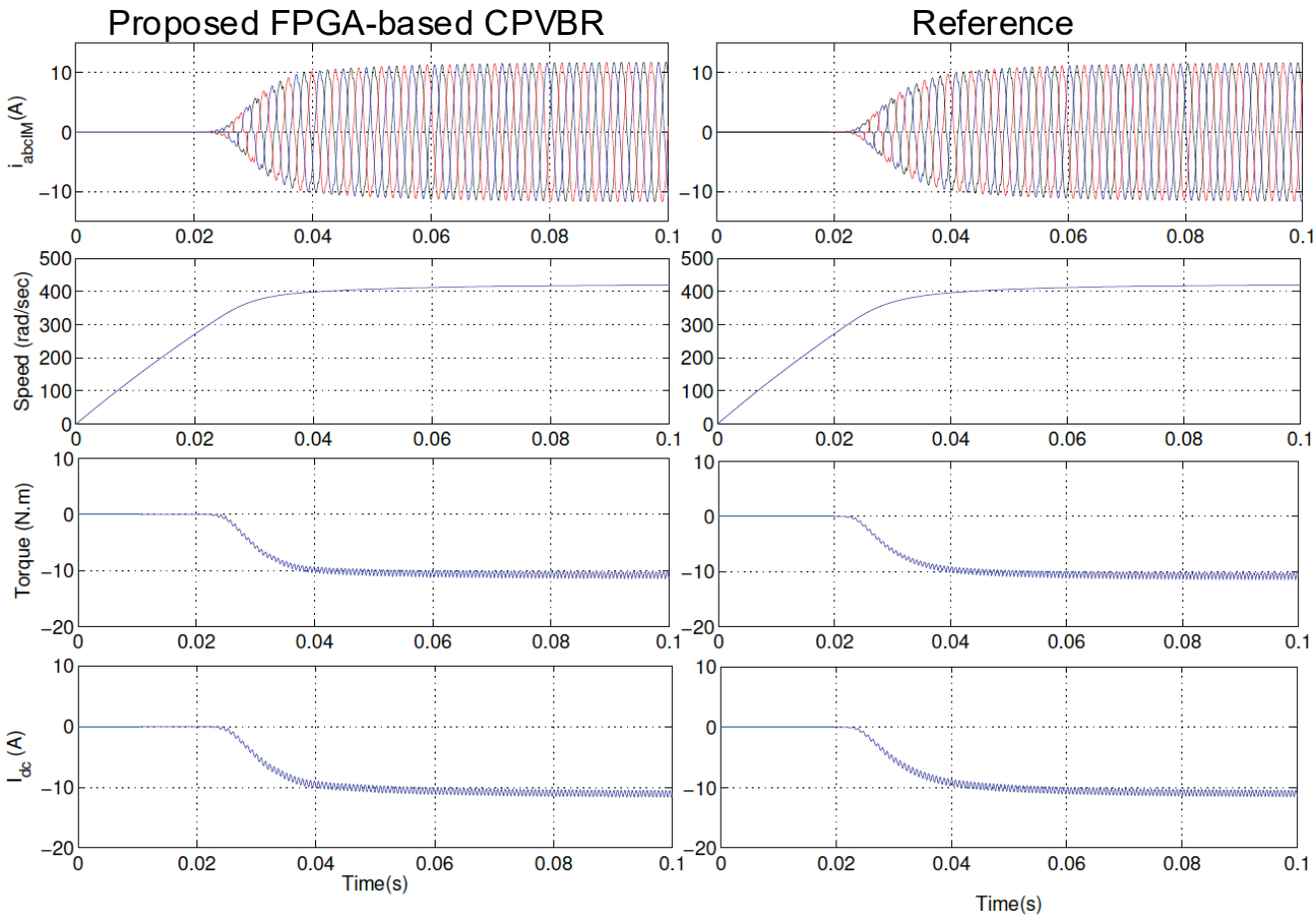


Verification of the proposed CPVBR model

PMSM diode bridge
Scenario: τ_m=-15N.m.

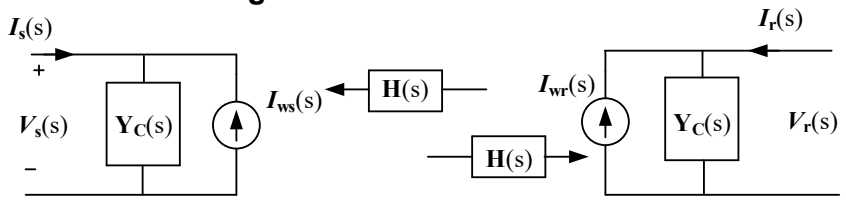


$$\frac{L_q''}{L_d''} = 1.5.$$

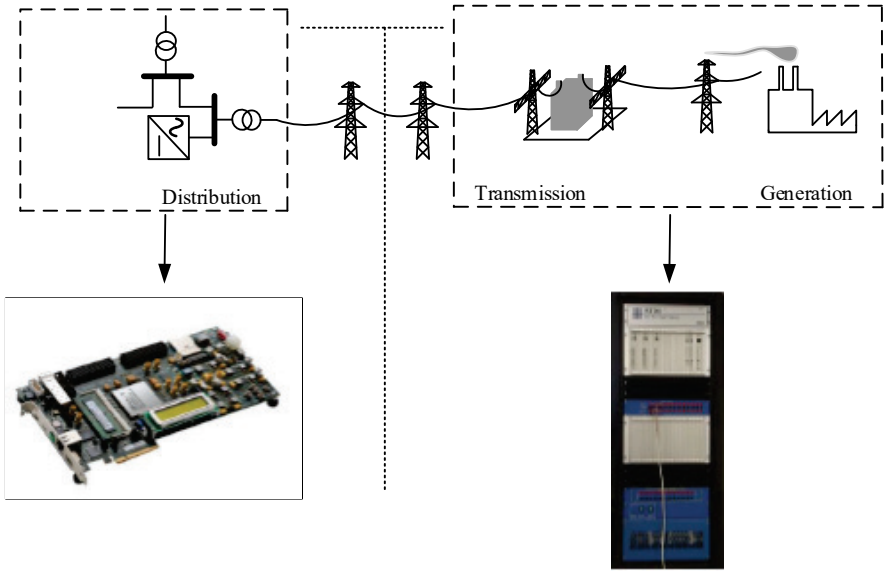


5-Transmission line model for parallel simulation

ULM traveling-wave transmission line model



Inter-Hardware-Universal-Line-Model
IHULM



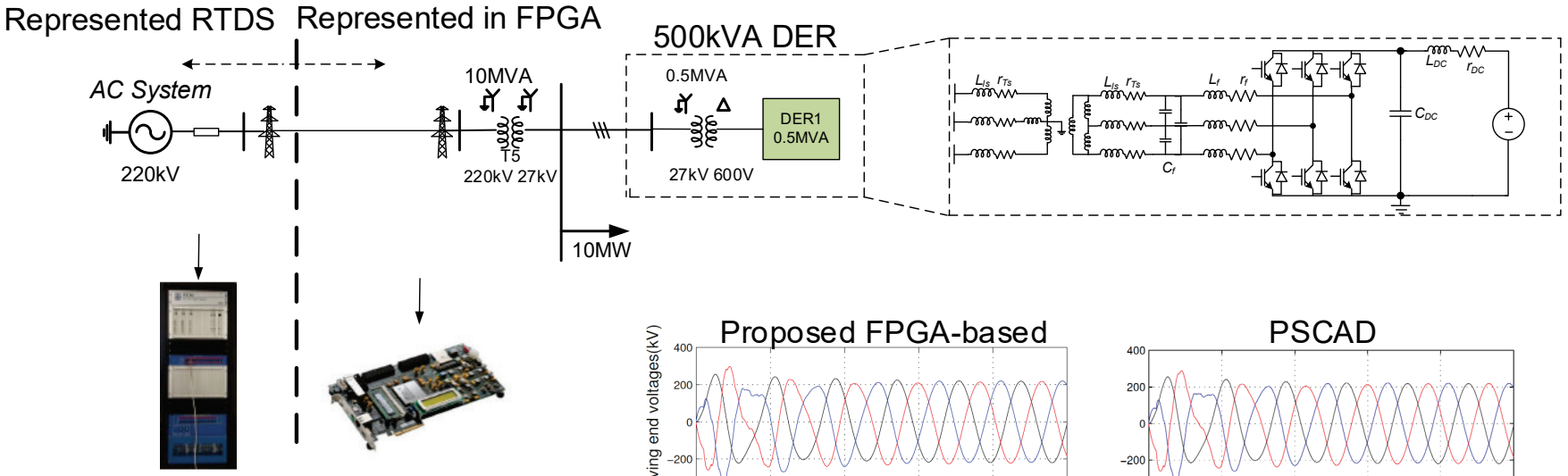
IHULM task:
To implement *H(s)* and $Y_C(s)$ *for* **both ends**

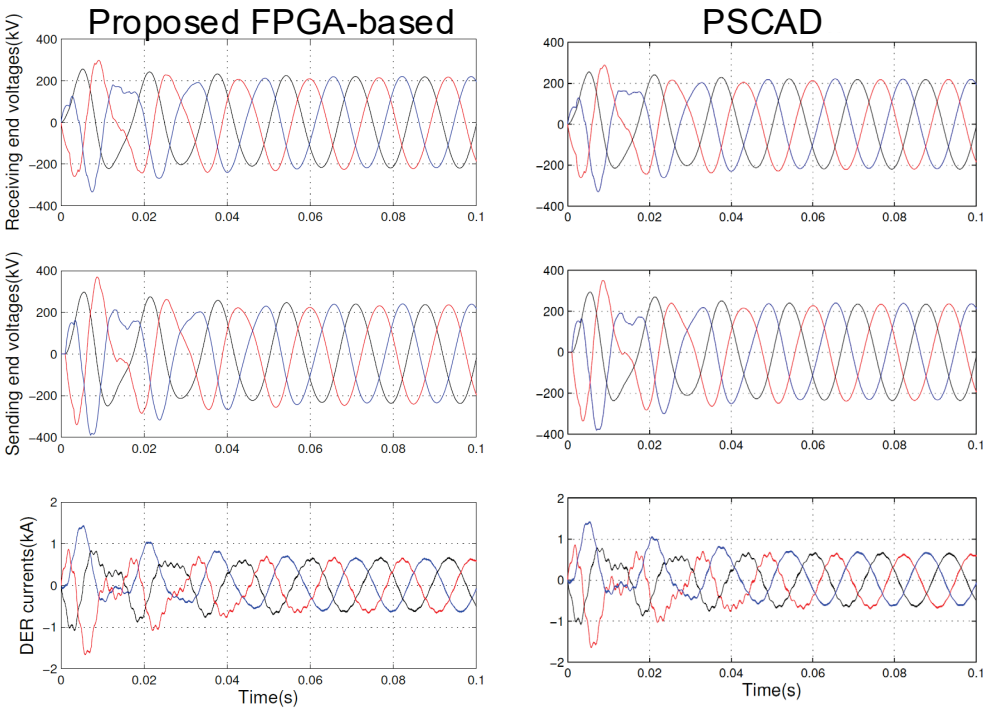
$$\boldsymbol{H}(s) \simeq \boldsymbol{H}_f(s) = \sum_{j=1}^{n_M}\left(\sum_{i=1}^{n_H} \frac{\boldsymbol{R}_{Hji}}{s - a_{Hji}} e^{-\tau_j s}\right),$$

$$\boldsymbol{Y}_c(s) \simeq \boldsymbol{Y}_f(s) = \boldsymbol{G}_0 + \sum_{i=1}^{n_Y} \frac{\boldsymbol{R}_{Yi}}{s - a_{Yi}},$$

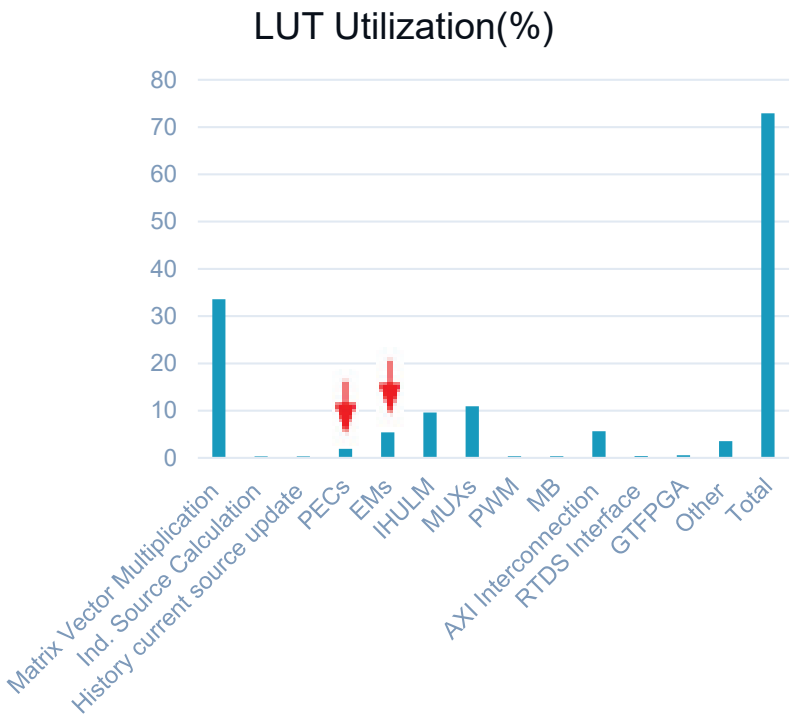
Verification of IHULM module

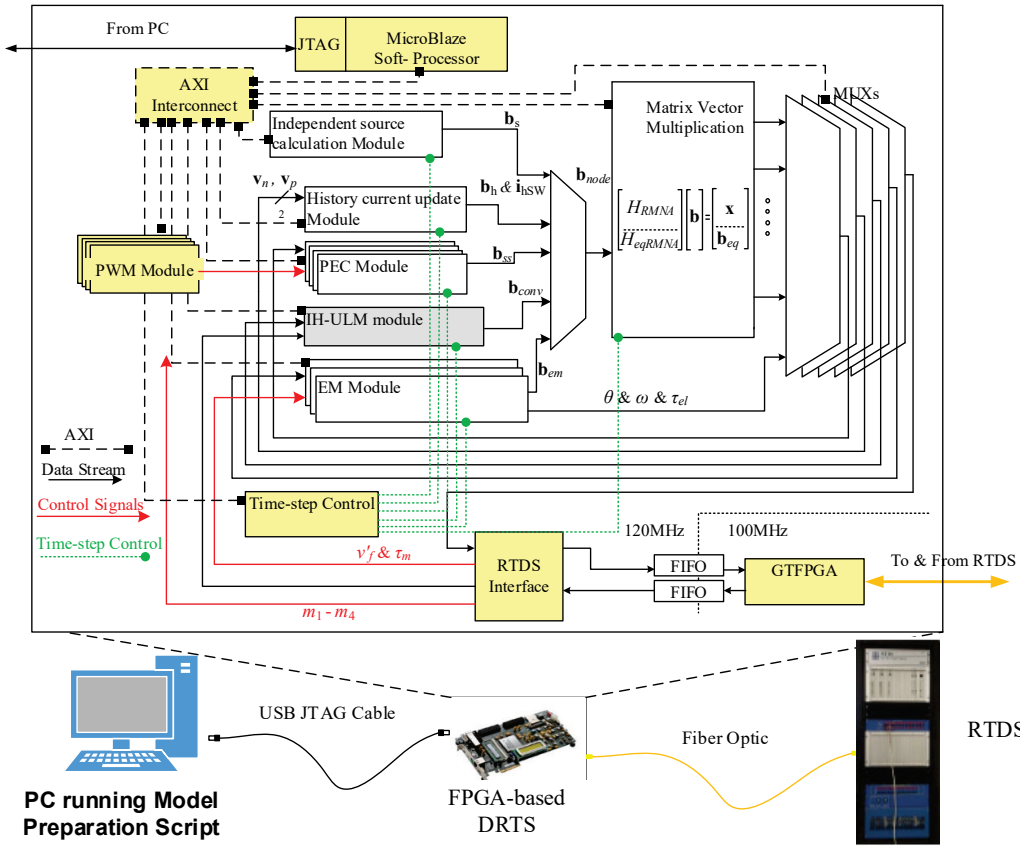
Parallel simulation case





6- FPGA-based real-time simulation hardware platform





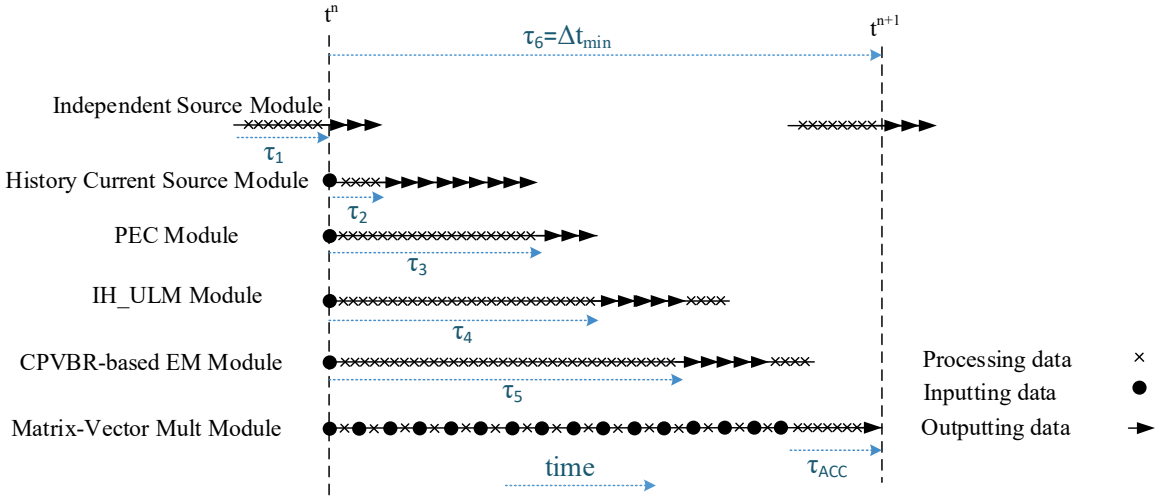
-160 nodes/outputs,

- 4 PECs,

- 3 EMs (IM, SM, or PMSM),

- 2.5417μs

Timing diagram of the platform



Stall-free pipeline condition

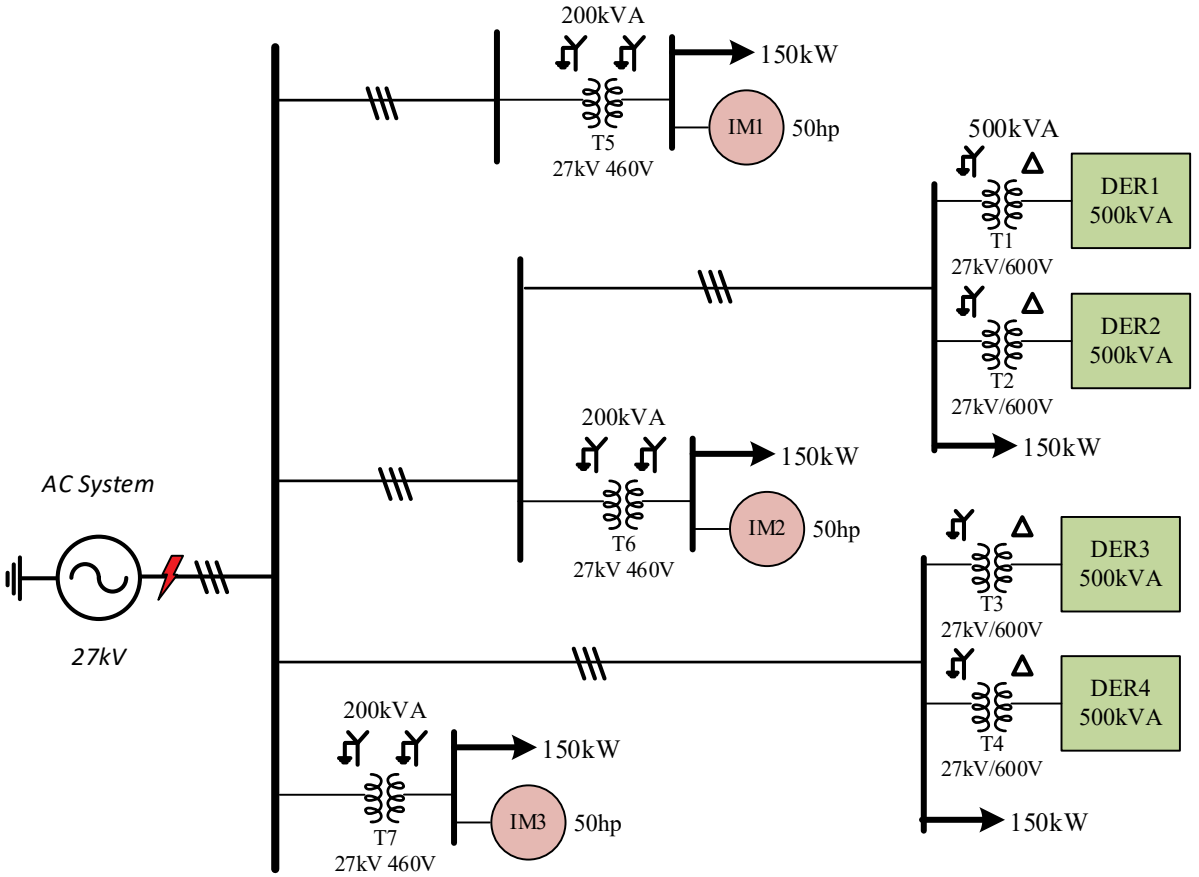
$$\tau_1 \leq \tau_6,$$
$$\tau_2 \leq 2l_1,$$
$$\tau_3 \leq 2(l_1 + l_2),$$
$$\tau_4 \leq 2(l_1 + l_2 + l_3),$$
$$\tau_5 \leq 2(l_1 + l_2 + l_3 + l_4),$$
$$l_1 + l_2 + l_3 + l_4 + l_5 = n_b,$$

Time-step = the latency of matrix-vector multiplication module
305 clock cycle @120MHz, **2.5417*μ*s**

Verification of the platform

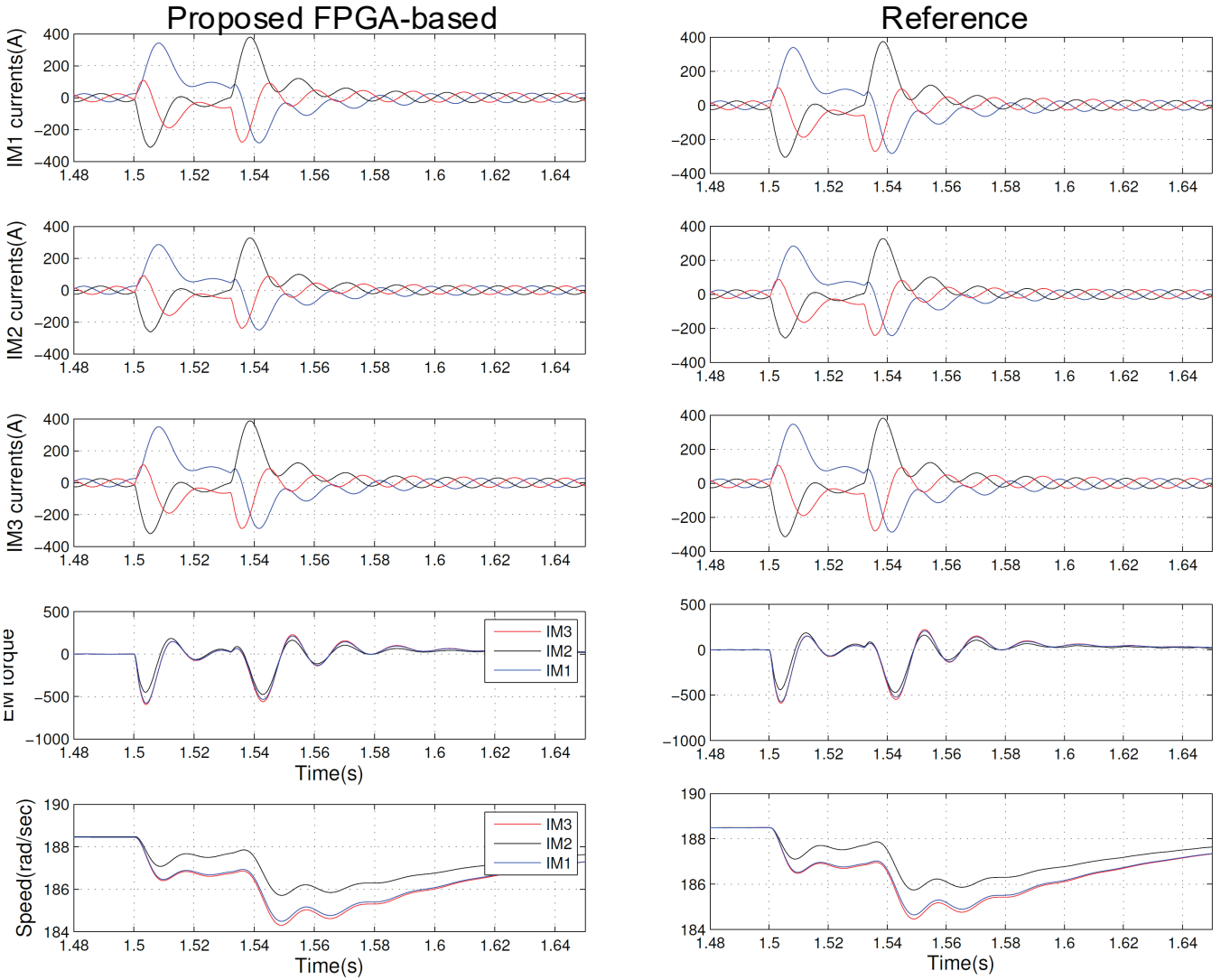
Case: Microgrid
Scenario:Three-phase temporary fault
Is applied @ t=1.5s and removed **@ t=1.532s**

Δt=2.6μs



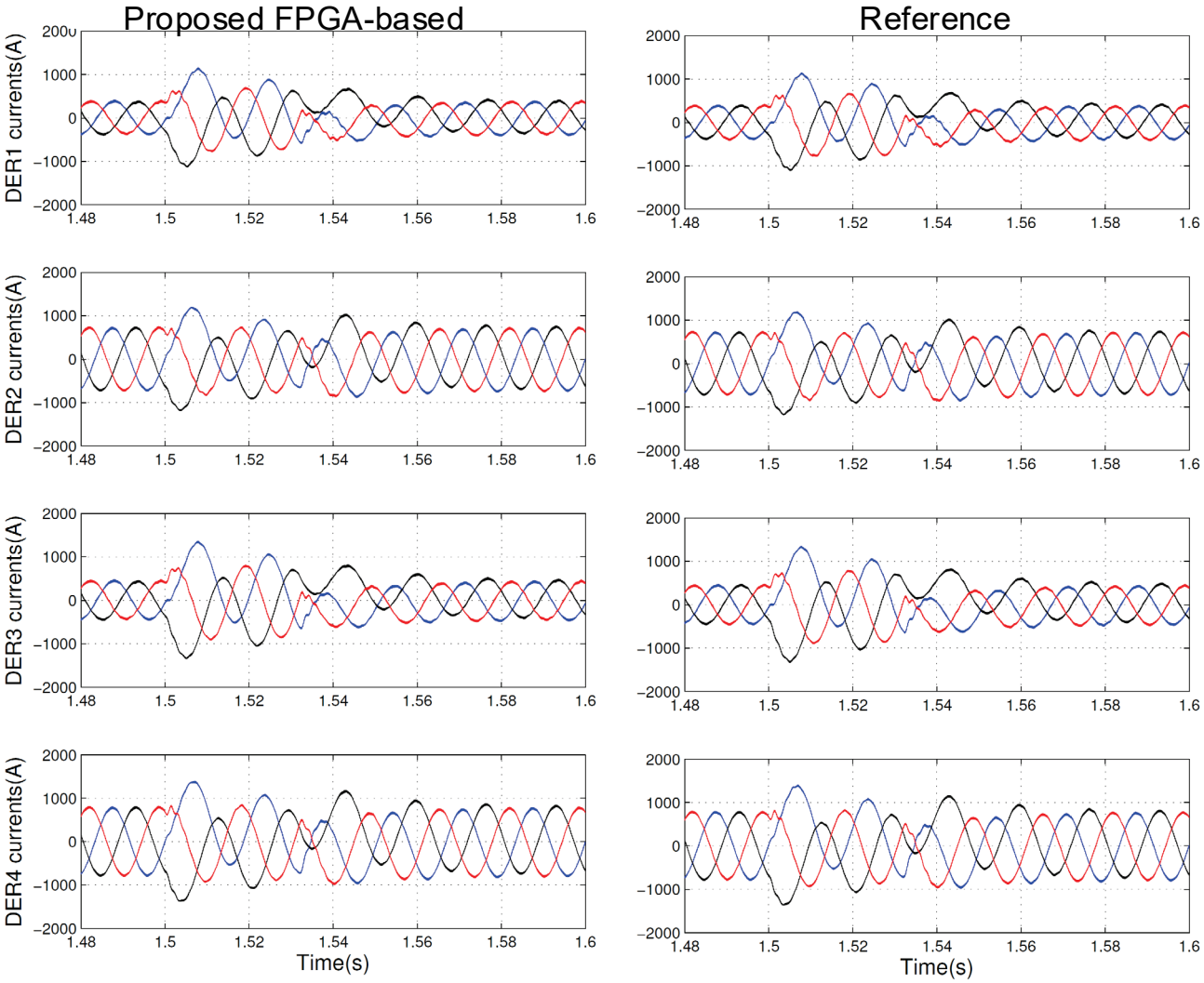
IM responses

Case: Microgrid



DER current responses

Case: Microgrid



Conclusions

-New FPGA-based **real-time simulator structure** and component **models, PEC, EM** and **IHULM** were **proposed**, **implemented** and their accuracy was **verified**

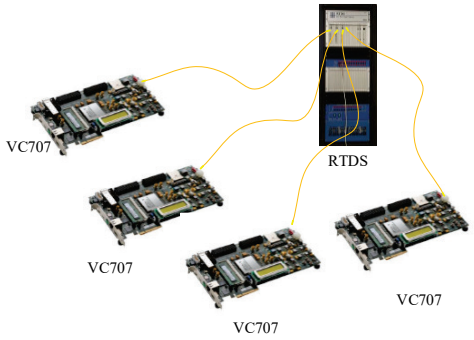
-The structure is **expandable** based on two approaches:

1- Larger chip for larger coupled grids

(FPGA chips with 2X resource → Matrix vector Mult. Module with a 2X performance)

~2X
Resource
→

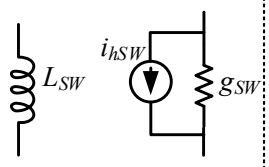
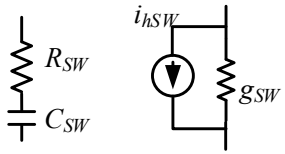
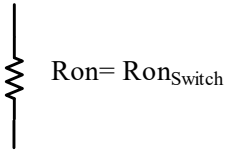
2- Modular expansion: (compatible with **power system** structure)



Thanks

4-Simulation of Power Electronic Converters (PECs)

Power switch models for EMT simulation

	Switch on	Switch off	Computation burden	Accuracy
ADC model (Common in Real-time)			Affordable (constant admittance matrix)	1- Artificial switching loss 2- Oscillation
Two-value resistor model (Common in offline)			High due to 1-variant admittance matrix 2-Iterative switch state determination	Precise

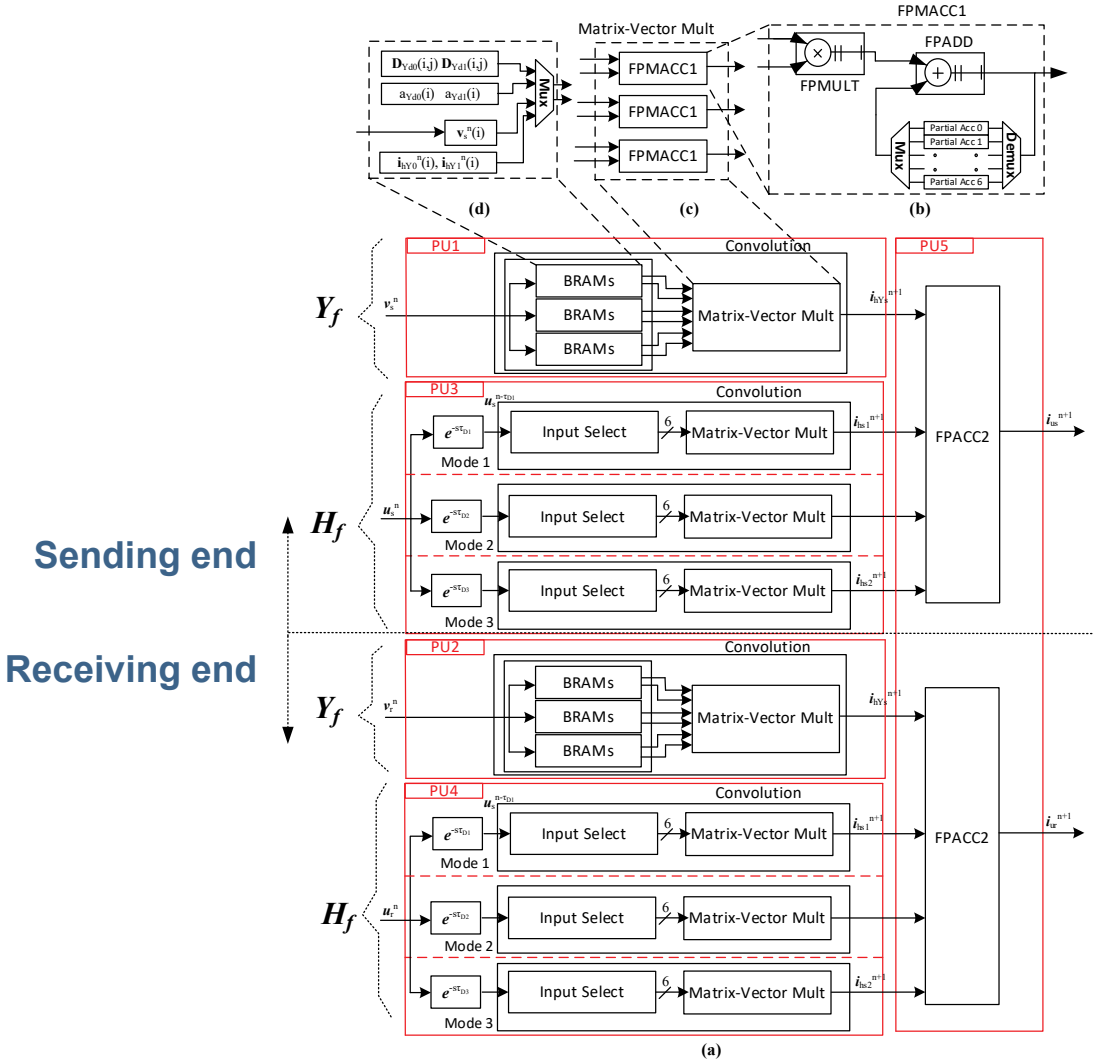
Our work uses this in real-time

Challenge:
Time-variant large set of equations

µs-range time-step and 100-200 nodes
requires O(n3) ~ 8TFLOPS computation burden for on-the-fly LU factorization

6-Transmission line model for parallel simulation

IHULM Module Design



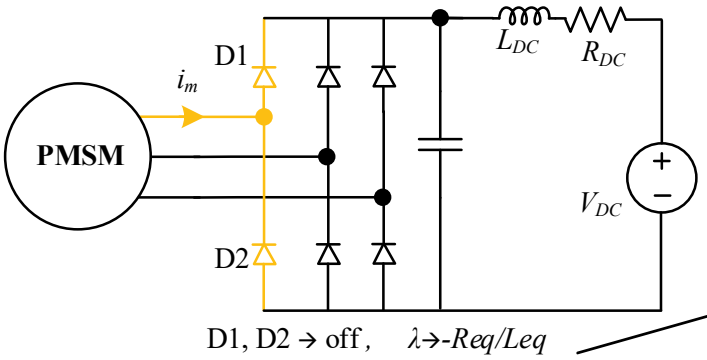
5-Simulation of Electrical Machines (EMs)

Objectives:
Design a fixed-hardware FPGA-based EM module for
- different types of EM
- regardless of system configuration;
- regardless of EM parameters;
- regardless of test scenarios.

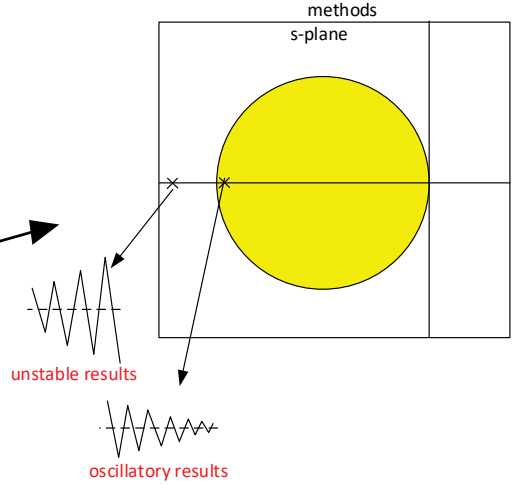
EM models for EMT analysis

Model	Rotor Frame	Stator Frame	Interface technique	Computational burden	Performance for stiff systems
QD	*dq0*	*dq0*	Current injection	reasonable	oscillatory, unstable
QD	*dq0*	*dq0*	Compensation	high (variable admittance)	accurate
PD	*abc*	*abc*	direct	high (variable inductance)	accurate
VBR	dq0	abc	direct	high (variable inductance)	accurate
CPVBR	dq0	abc	direct	reasonable	(?) depends on dynamic saliency Ld" = Lq" Ld" ≠ Lq"

Ex. of a numerically stiff system



Ex. of Region of A-stability for explicit methods



5-Simulation of Electrical Machines (EMs)

EM models for EMT analysis

Model	Rotor Frame	Stator Frame	Interface technique	Computational burden	Performance for stiff systems
QD	*dq0*	*dq0*	Current injection	reasonable	oscillation, instability
QD	*dq0*	*dq0*	Compensation	high (variable admittance)	accurate
PD	*abc*	*abc*	direct	high (variable inductance)	accurate
VBR	dq0	abc	direct	high (variable inductance)	accurate
CPVBR	dq0	abc	direct	Reasonable (Constant Parameter)	(?) depends on dynamic saliency Ld" = Lq" Ld" ≠ Lq"

Objective:

Devise an EM model

- **Compatible with PEC** simulation technique

and design a FPGA-based EM module

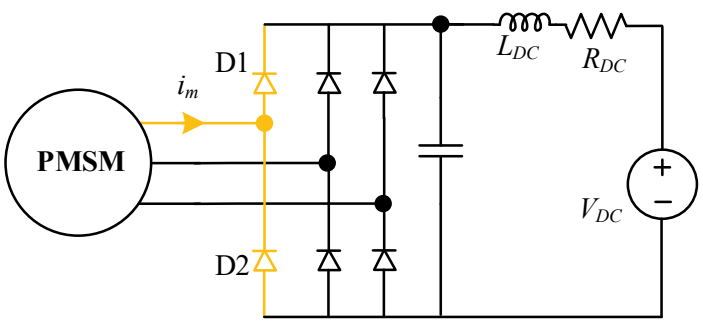
-with **fixed-hardware**

- for different types of EM

- regardless of system configuration

- regardless of EM parameters (dynamic saliency)

Ex. of a numerically stiff system



D1, D2 → off, $\lambda \rightarrow -Req/Leq$

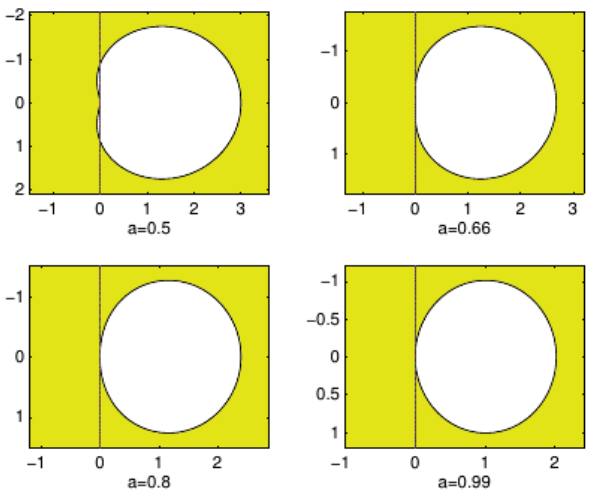
5-Simulation of Electrical Machines (EMs)

Proposed CPVBR for EMs with (L_d"≠L_q") :

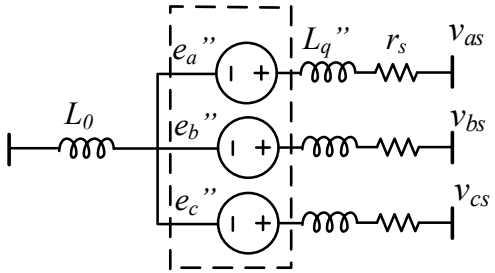
Implicit stiff LMS integration method

$$x^{n+1} + (a-2)x^n + (1-a)x^{n-1} = \Delta t\, a\, f(x^{n+1}, t^{n+1}), \quad 0 < a \leq 1,$$

Region of A-stability for the proposed method



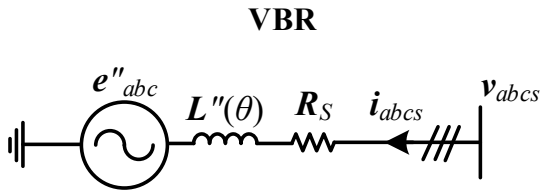
CPVBR model **interface** for **IM, SM, PMSM**

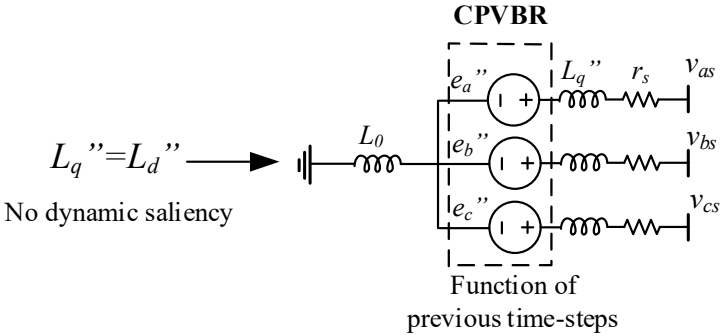


EM simulation task: calculation of voltage sources e_a", e_b" and e_c"

-In **parallel** with the rest of the tasks

CPVBR EM model





$$\mathbf{L}''(\theta) = \begin{bmatrix} L_s + \frac{L''_{mq}+L''_{md}}{3} & -\frac{L''_{mq}+L''_{md}}{3} & -\frac{L''_{mq}+L''_{md}}{3} \\ -\frac{L''_{mq}+L''_{md}}{3} & L_s + \frac{L''_{mq}+L''_{md}}{3} & -\frac{L''_{mq}+L''_{md}}{3} \\ -\frac{L''_{mq}+L''_{md}}{3} & -\frac{L''_{mq}+L''_{md}}{3} & L_s + \frac{L''_{mq}+L''_{md}}{3} \end{bmatrix}$$

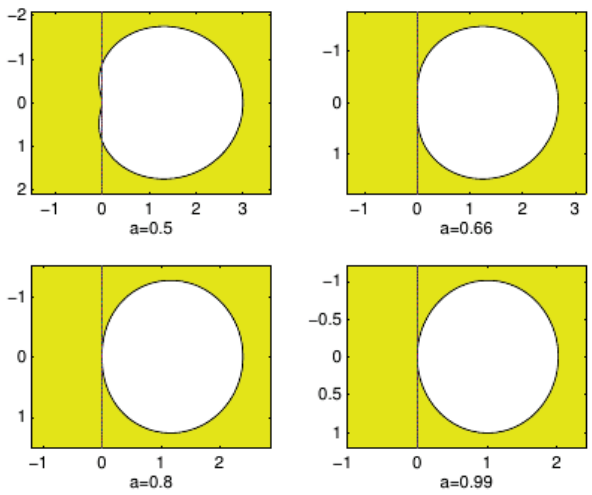
$$+\frac{L''_d - L''_q}{3} \begin{bmatrix} cos(2\theta) & cos(2\theta - \frac{2\pi}{3}) & cos(2\theta + \frac{2\pi}{3}) \\ cos(2\theta - \frac{2\pi}{3}) & cos(2\theta - \frac{4\pi}{3}) & cos(2\theta) \\ cos(2\theta - \frac{2\pi}{3}) & cos(2\theta) & cos(2\theta + \frac{4\pi}{3}) \end{bmatrix}.$$

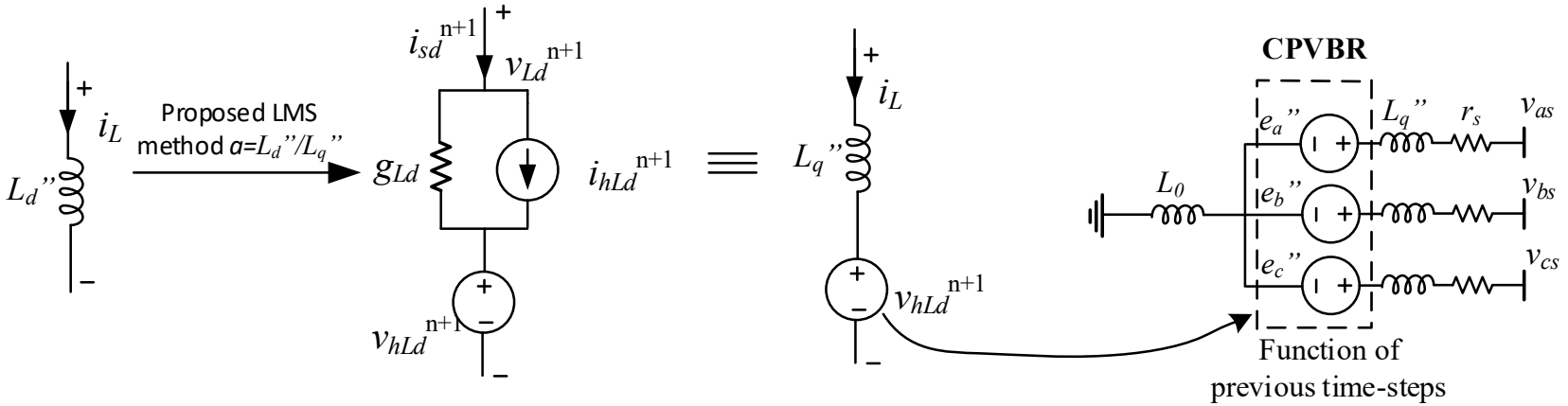
Proposed CPVBR for EMs with (L_d"≠ L_q") :

Implicit stiff LMS integration method

$$x^{n+1} + (a-2)x^n + (1-a)x^{n-1} = \Delta t\, a\, f(x^{n+1}, t^{n+1}), \quad 0 < a \le 1,$$

Region of A-stability for the proposed method

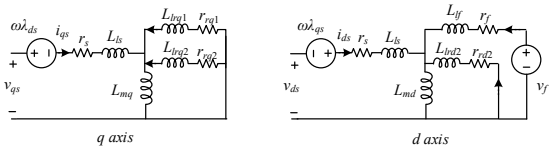




5-Simulation of Electrical Machines (EMs)

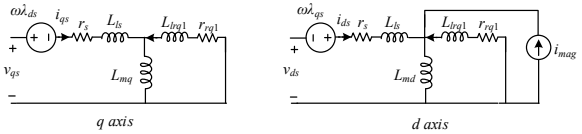
EM fixed-hardware module design approach

SM



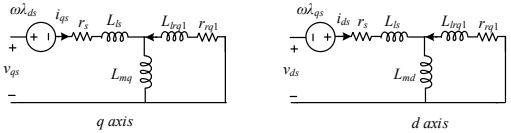
U

PMSM



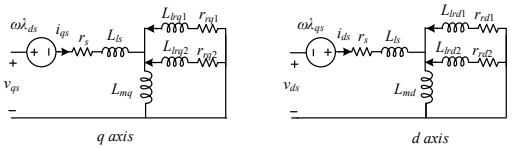
U

Single-cage IM

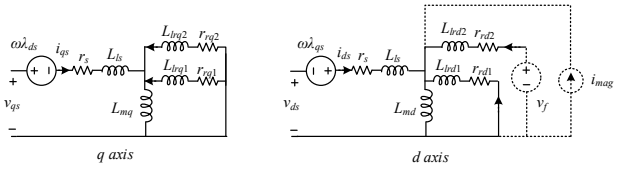


U

Double-cage IM

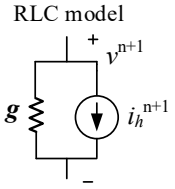


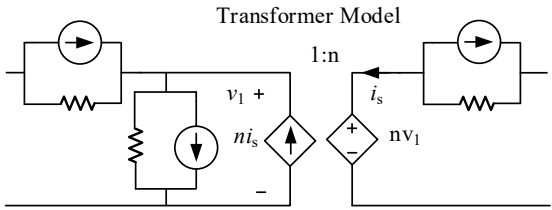
Generalized EM in this work

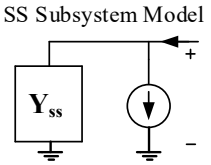


2- FPGA-based simulation of power network

- **Combined MNA and State-Space Formulation**
  - Independent sources
  - RLC Branches
  - Transformers
  - State-Space Subsystems







- **4 tasks (or 4 modules in FPGA design)**

  1- Independent source calculation

  2- RLC history current calculation

  3- Subsystem history calculation

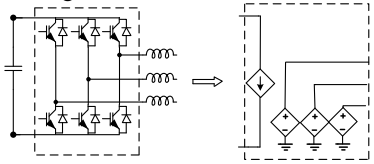
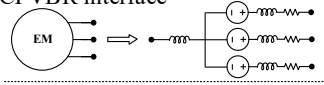
$$\underbrace{\begin{bmatrix} G & A_g \\ B_g & 0 \end{bmatrix}}_{Y} \underbrace{\begin{bmatrix} v^{n+1} \\ i_{vs}^{n+1} \end{bmatrix}}_{x_{node}^{n+1}} = \underbrace{\begin{bmatrix} u_i^{n+1} \\ v_s^{n+1} \end{bmatrix}}_{u_{node}^{n+1}}$$

  4- Solution of the equations $x_{node}^{n+1} = Y^{-1} u_{node}^{n+1}$

- **Limitations for FPGA-based implementation:**
  - **Anti-parallel pattern**
    The solution of the network (4) can not be started until first three (1,2,3) tasks are done.
  - **Prevents fixed hardware design**
    The structure of the nodal injection vector depends on the network topology

Model preparation script diagram

Order of Execution →

	Preparation of Intermediate Netlist	Calculation of RMNA matrix and Module parameters	Calculating system matrix
Independent source		Find: $(\Delta t, \mathbf{a_s}, \mathbf{s_{type}}, \boldsymbol{\varphi}^0, \mathbf{f_s})$	
History current source update		Find: $(\mathbf{c}_v, \mathbf{c}_h, \mathbf{i}_h^0)$	
IH-ULM		Find $(\boldsymbol{G_Y}, a_{Hdij}s, \boldsymbol{D}_{Hij}s, a_{Ydi}s, \boldsymbol{D}_{Ydj}s)$	
PEC	Replace each PECSN by its terminal voltage/current sources 	For each PEC find: $\mathbf{Y'}_{conv}(s)$	For i^{th} PEC find: Matrices $\mathbf{Y}_{eqi}$, $\mathbf{H}_{CONVi}(\mathbf{s})$, $\mathbf{H}_{SWi}(\mathbf{s})$ and $\mathbf{H}_{eqRMNAi}$
EM	Replace each EM by its CPVBR interface 	For each EM find: Matrices $\mathbf{C}_{e1}$, $\mathbf{C}_{e2}$, $\mathbf{D}_e$, $\mathbf{A}_{Dr}$, $\mathbf{B}_{Dr}$, $\mathbf{C}_{Dr}$, $\mathbf{D}_{Dr}$, and $c_{\omega 1}$, $c_{\omega 2}$.	
Matrix-Vector Multiplication		Constitute admittance matrix $\mathbf{Y}$ And obtain matrix $\mathbf{H}_{RMNA}$	Construct system matrix $\begin{bmatrix} \mathbf{H}_{RMNA} \\ \mathbf{H}_{eqRMNA1} \\ . \\ \mathbf{H}_{eqRMNA4} \end{bmatrix}$