(PHIL) Simulation based Testing

Solar PV Inverter Islanding and Medium Voltage DC Systems

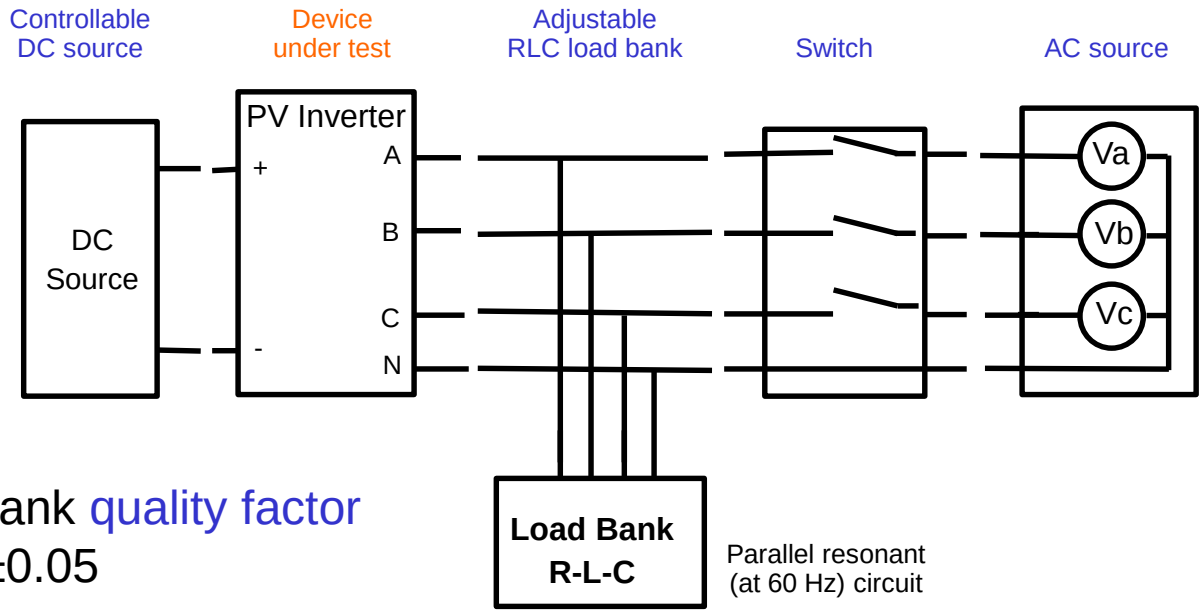
May 2015

Mischa Steurer, James Langston, John Hauer, Ferenc Bogdan, Michael Murry, Karl Schoder

Dionne Soto, Matthew Bosworth

RTDS Users' Group Meeting
San Francisco, CA

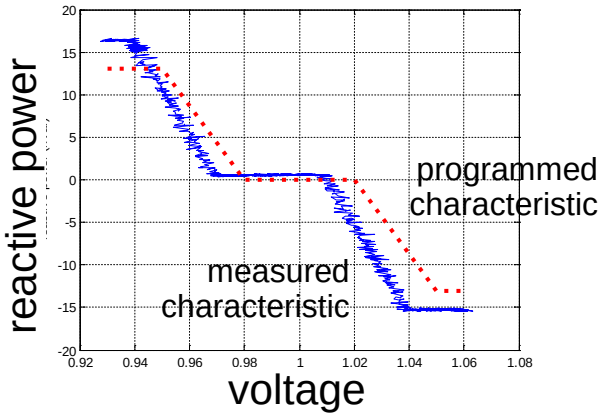
Unintentional Islanding Test (IEEE 1547.1)



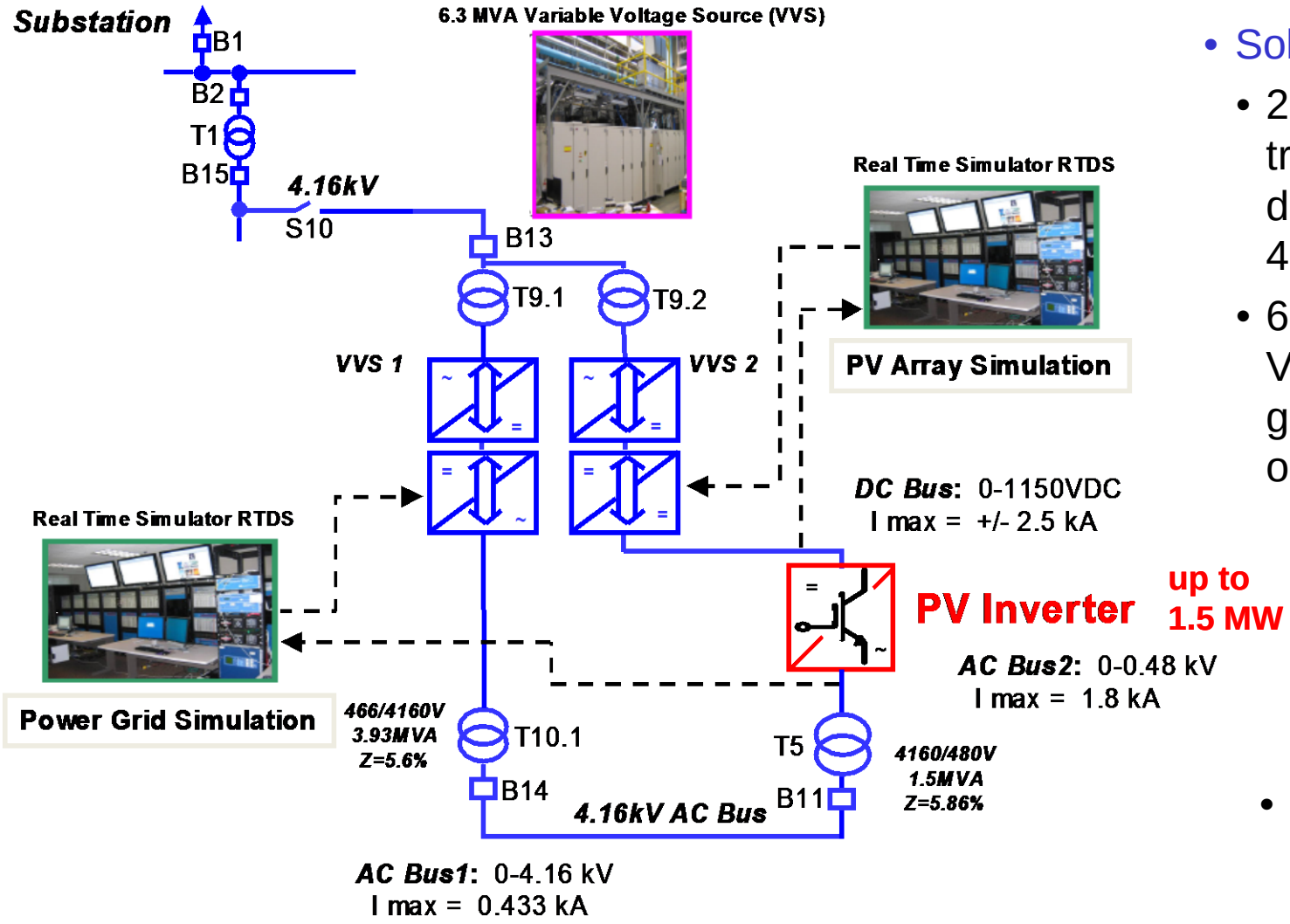
NREL
NATIONAL RENEWABLE ENERGY LABORATORY

Part of Hi-Pen PV Integration Project, Barry Mather

- Load bank quality factor $Q_f = 1 \pm 0.05$
- Residual current from grid: Inverter output matches load active power
- Inverter has 2 seconds to detect island (tries to destabilize system)
- Issues
  - Costs, inflexible, time (test setup reconfiguration)
  - What if advance control functions are active?
  - Can PHIL approach be used?



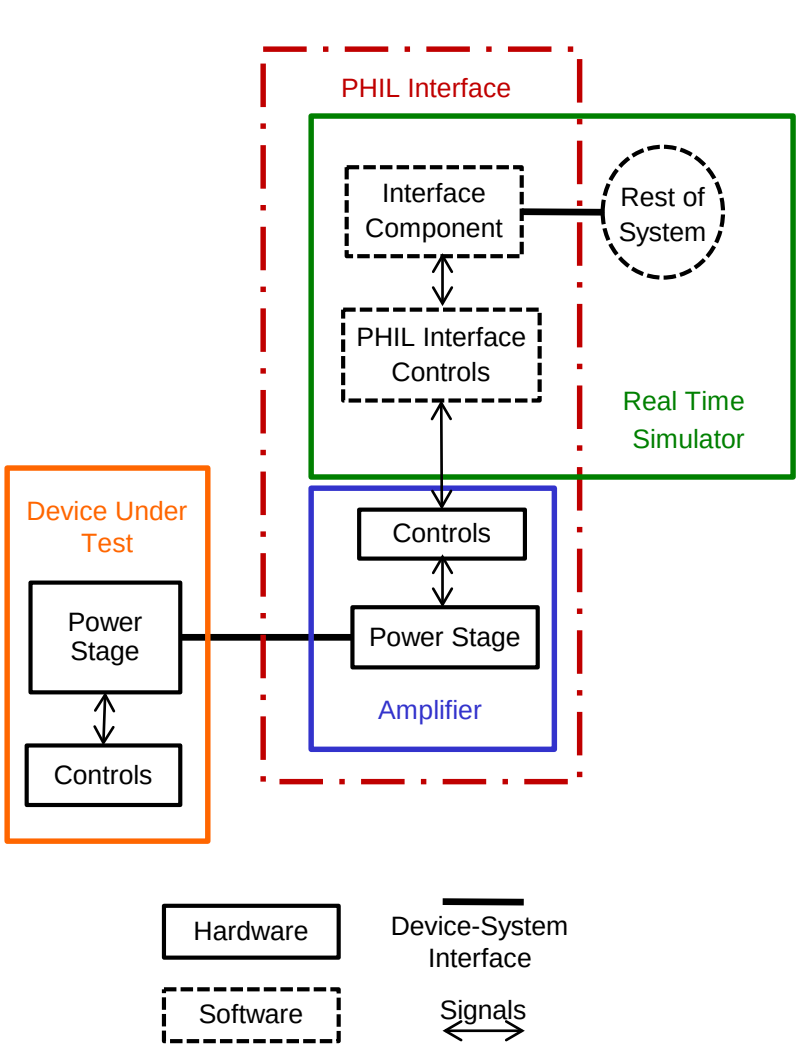
Test Setup and Facilities

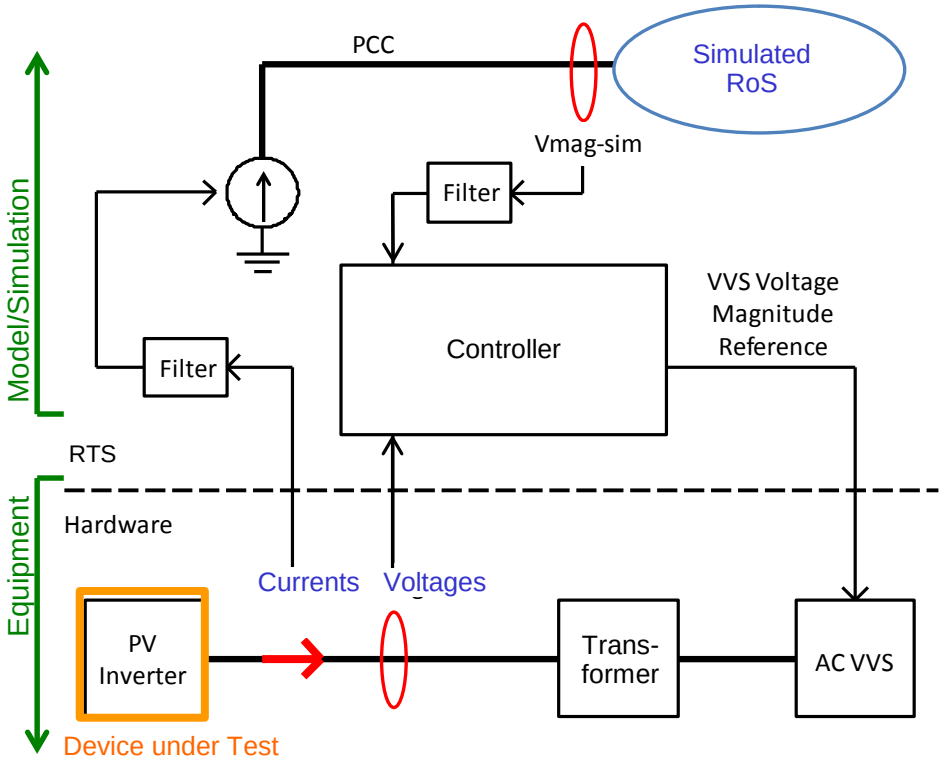


- Solar PV inverters
  - 20 kW, transformerless design, 480 V/277 V wye
  - 60 kW, 480 V/277 V wye with galvanic isolation on DC side
- Linear amplifier, limited to 350Vdc and 10 kW

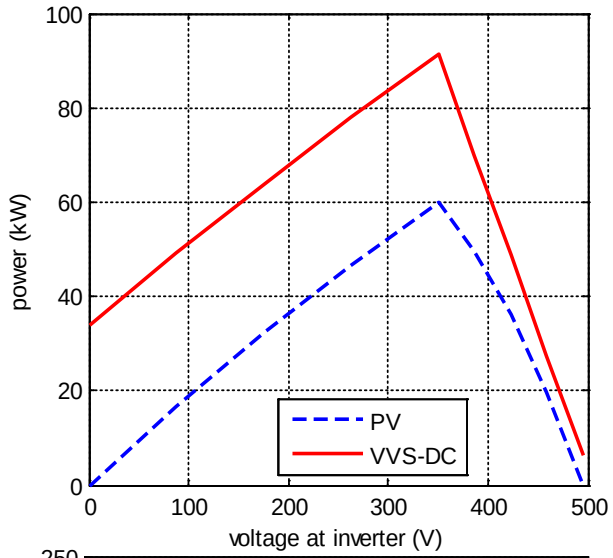
Power Hardware-in-the-Loop
Simulation Principle

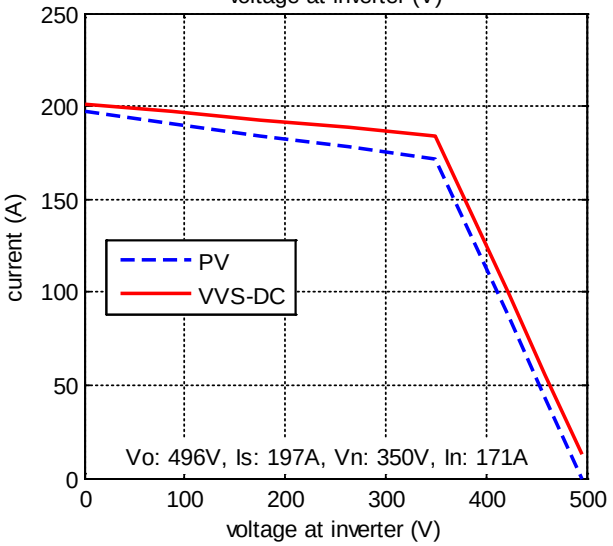
Coupling simulation and hardware





Emulating Solar PV Arrays

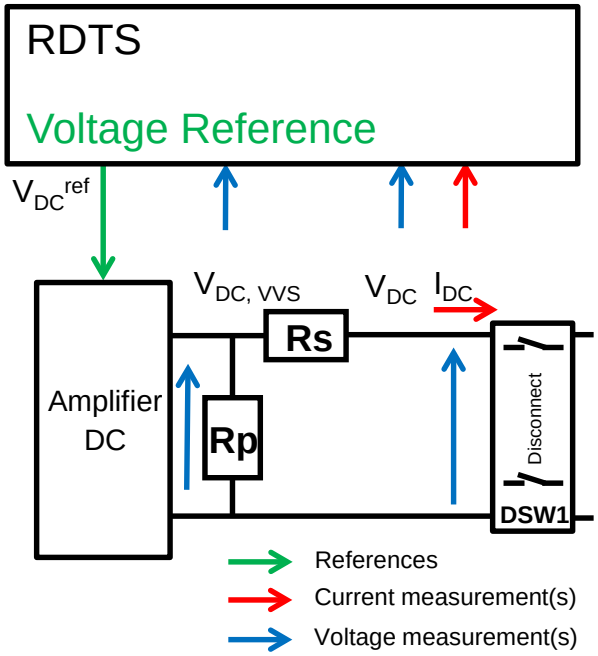




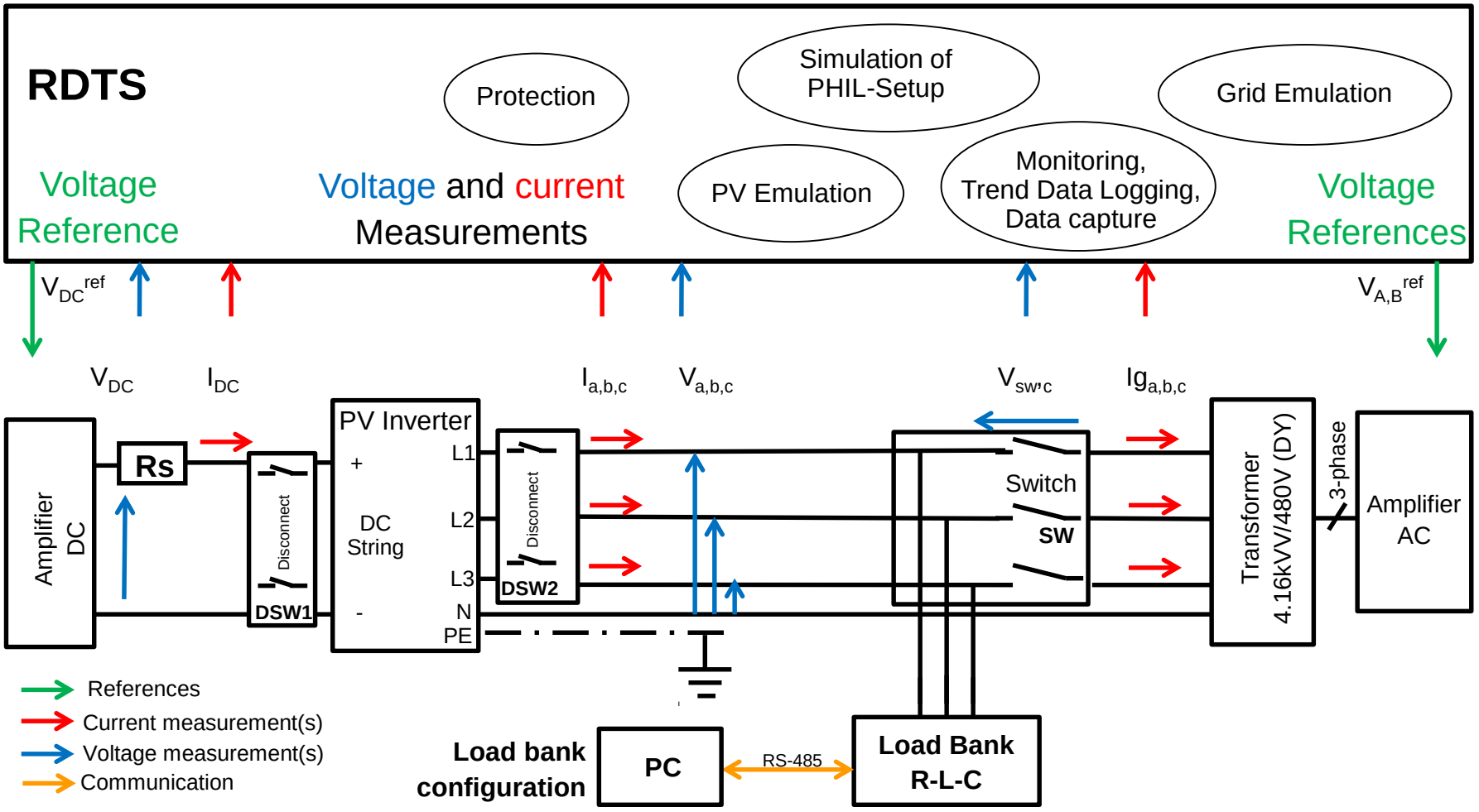
- PV array characteristic (blue)
- Amplifier control characteristic (red)

PHIL-interface on DC-side

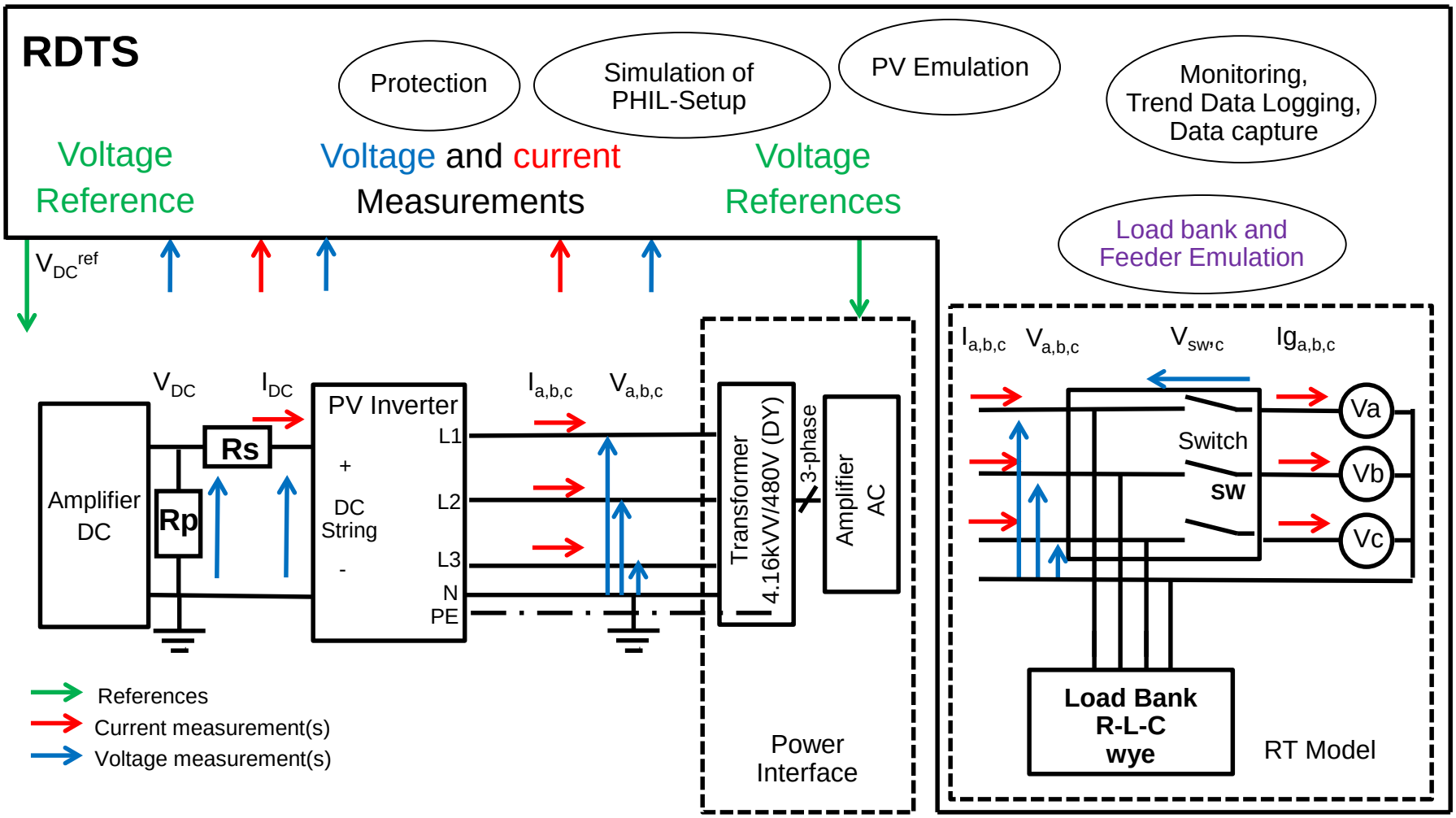
- Instantaneous voltage and current



Test Setup with Load Bank



Test Setup for PHIL

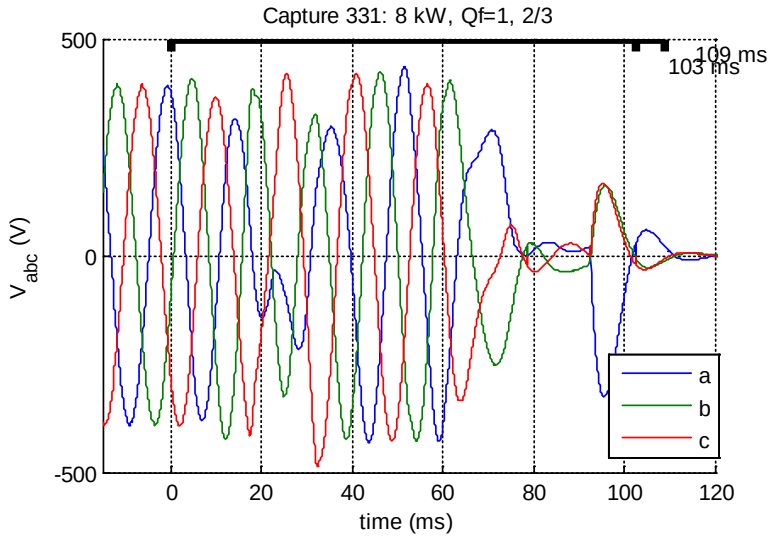


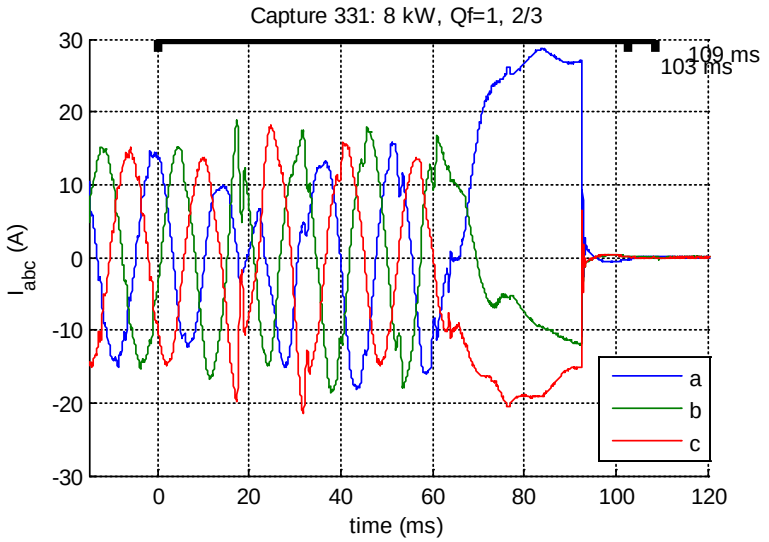
PHIL Interface Algorithms

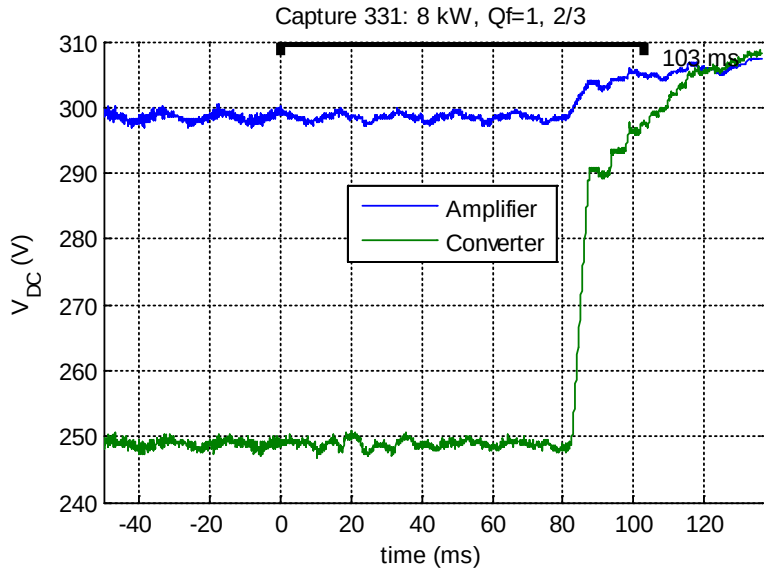
Several PHIL interface algorithms available and used:

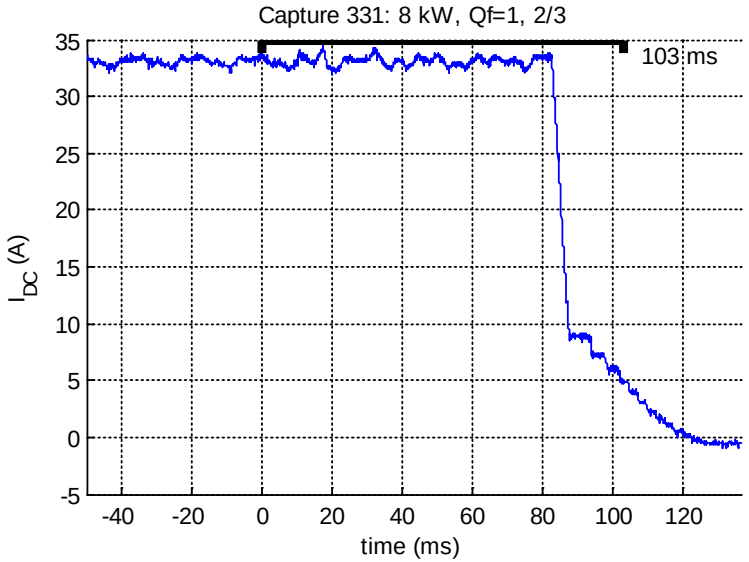
- Reference frame based approaches
  - Positive and negative sequence tracking
- Instantaneous Ideal Transformer Model (ITM)
  - Simple from an implementation standpoint
  - Region of stability smaller than compared to DIM
- Instantaneous Damping Impedance Method (DIM)
  - Current and voltage fed back into Rest-of-System model
- Challenges
  - Time delays
  - Stability and accuracy

Example Results: Using Load Bank (baseline)



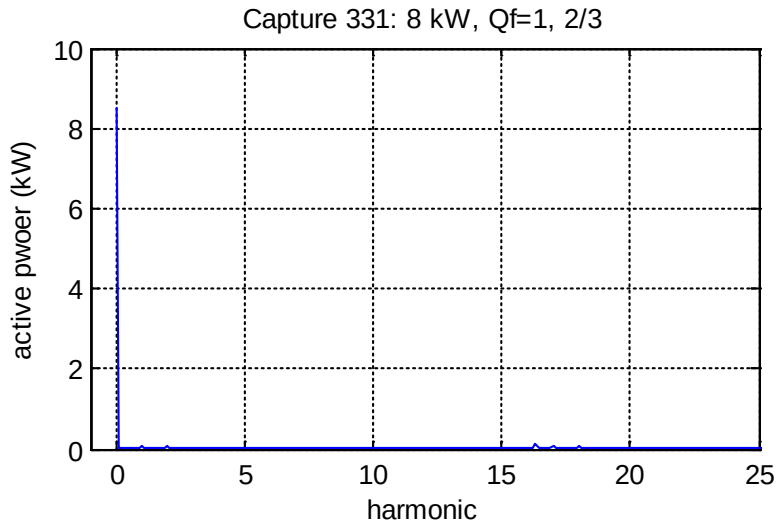


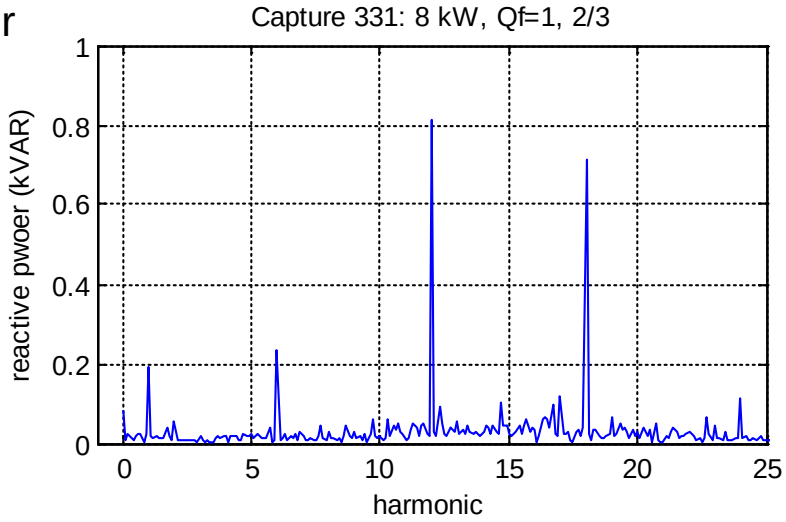




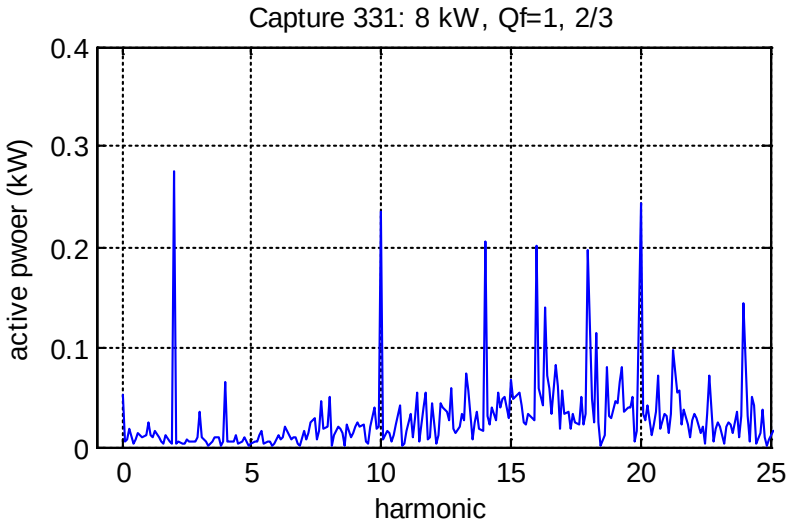
Example Results: Using Load Bank

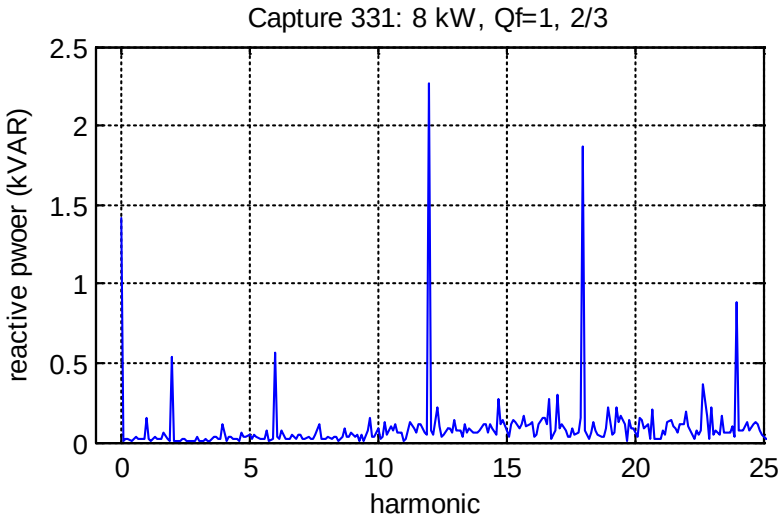
Inverter



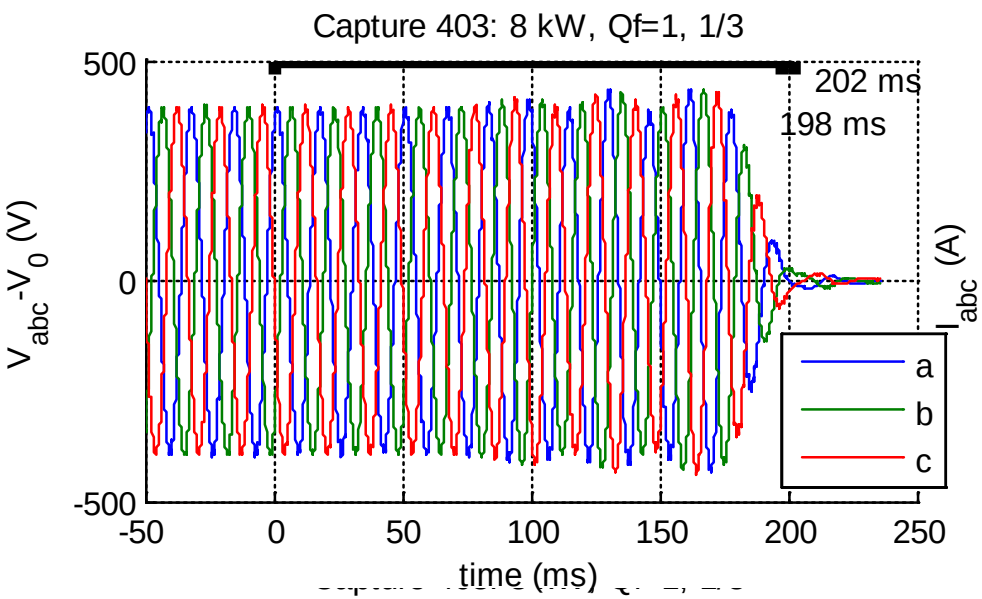


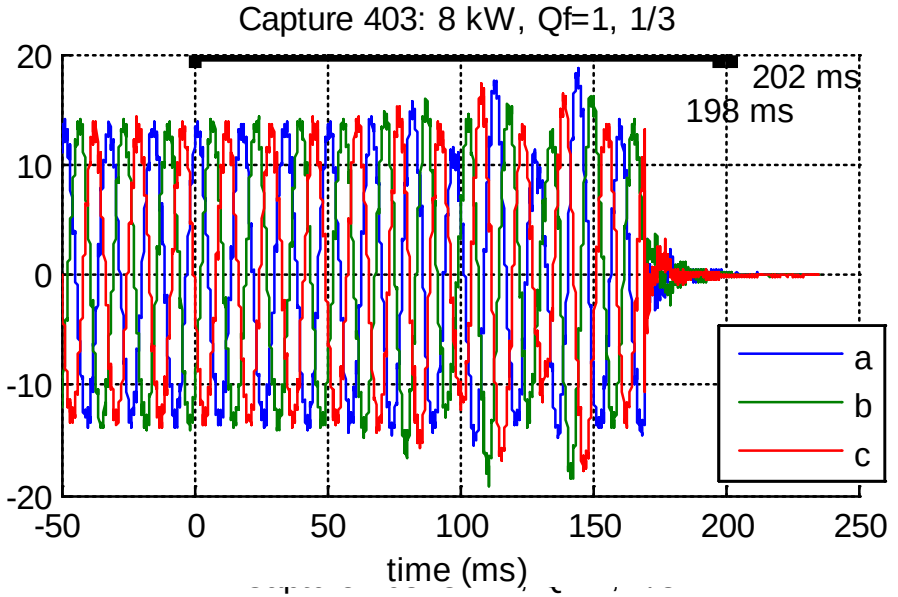
Grid

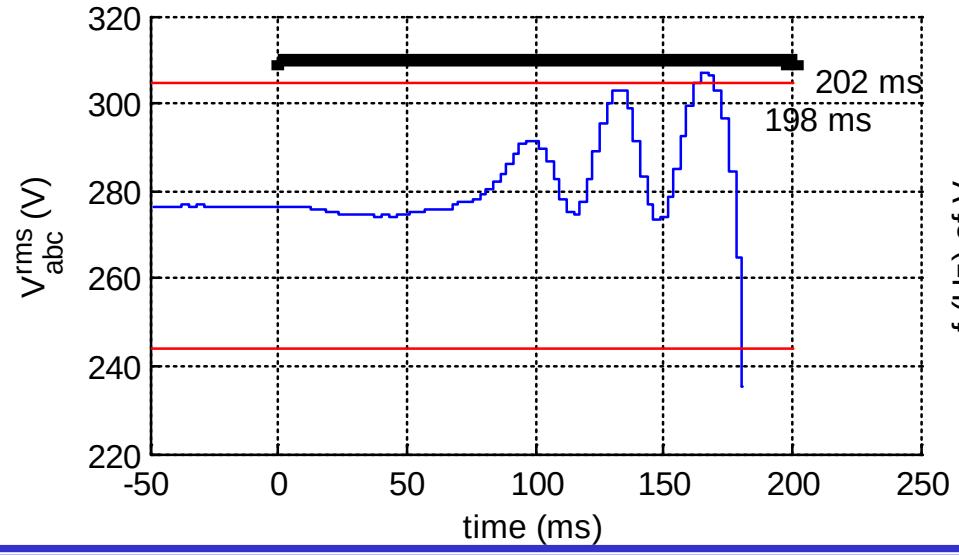


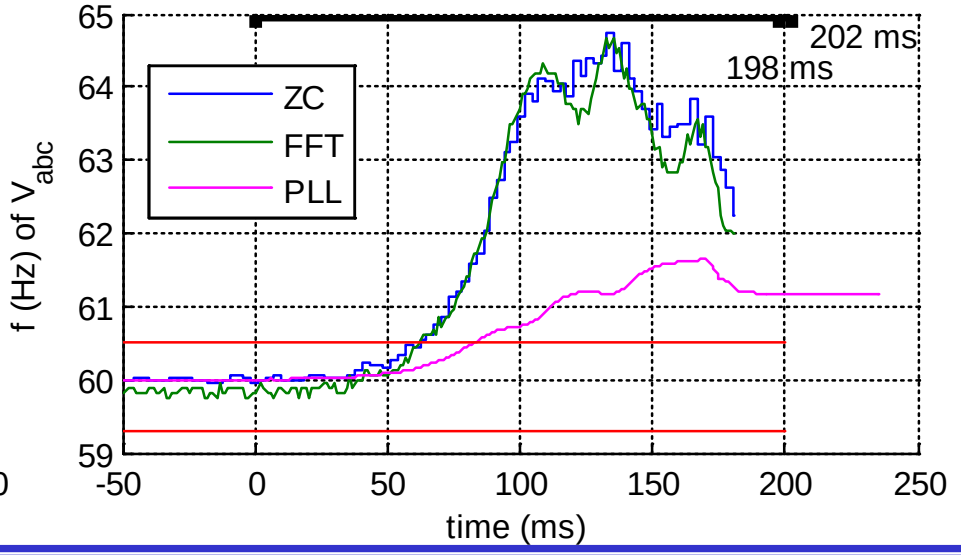


Example Results: RLC with DQ-PHIL

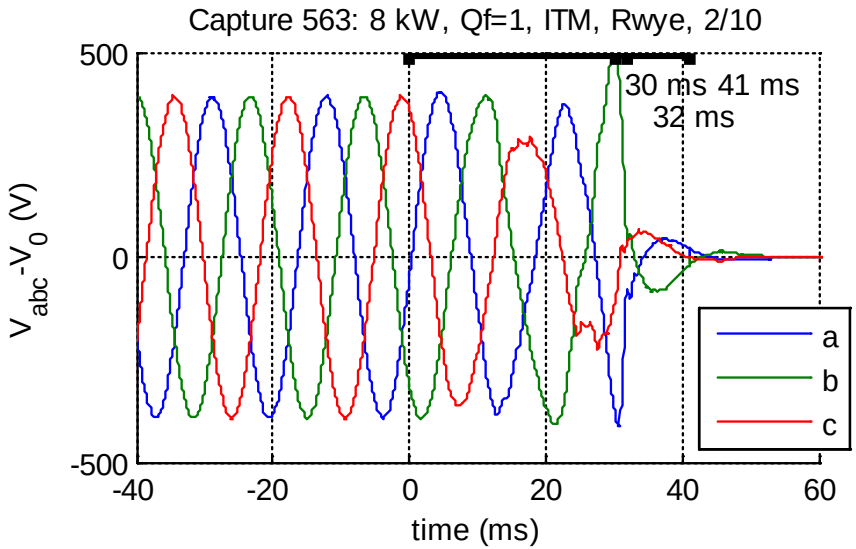


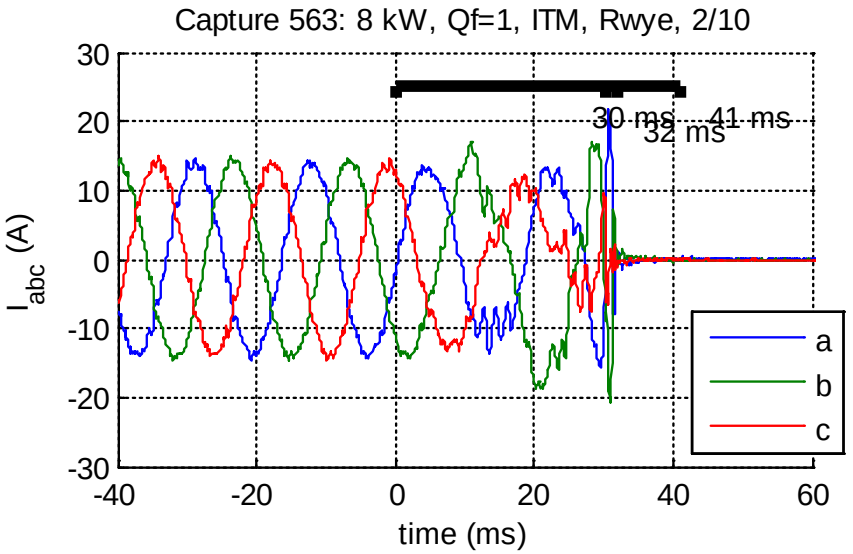


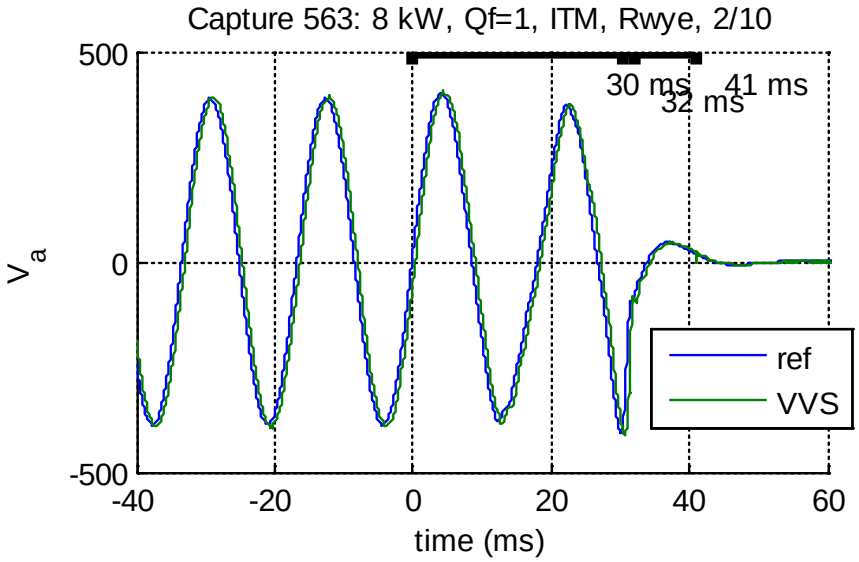


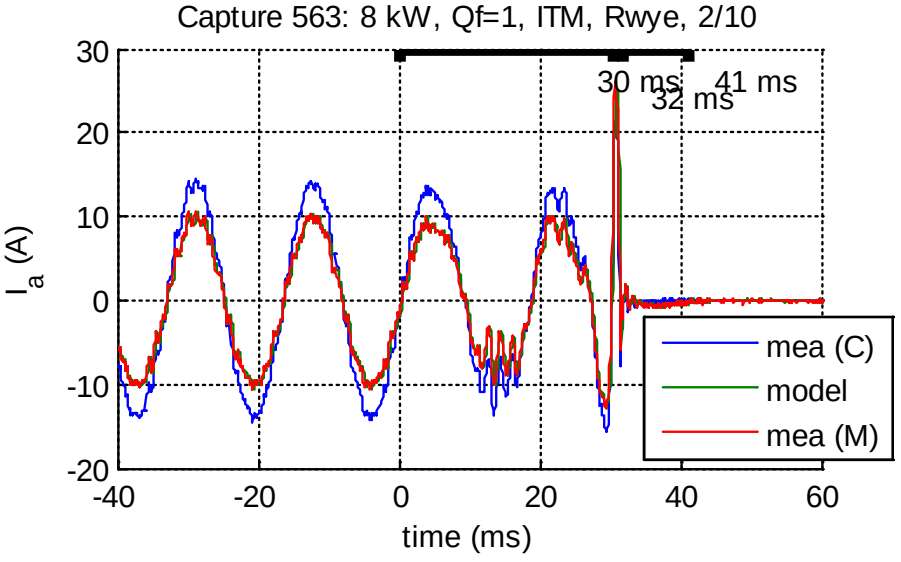


Example Results: RLC with ITM-PHIL





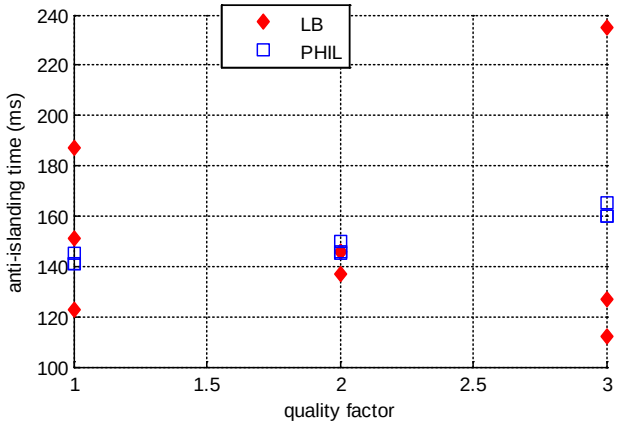




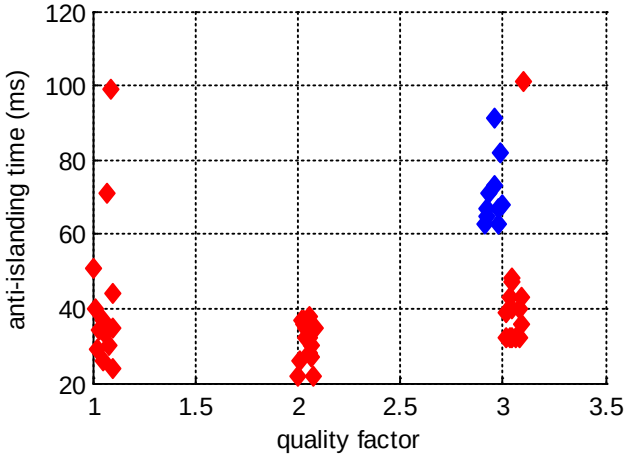
Timing for RLC Load Bank

3 kW

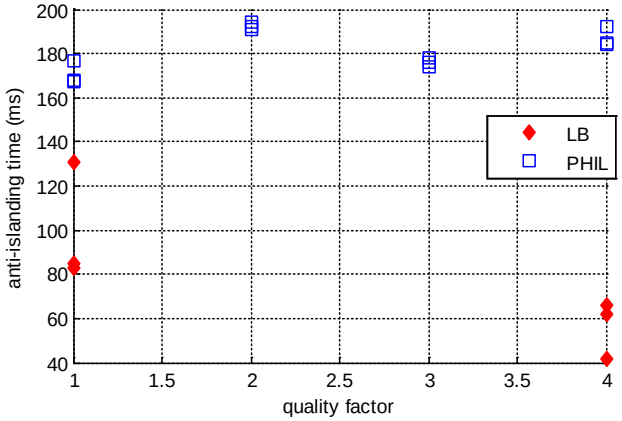
Load bank vs. DQ-PHIL

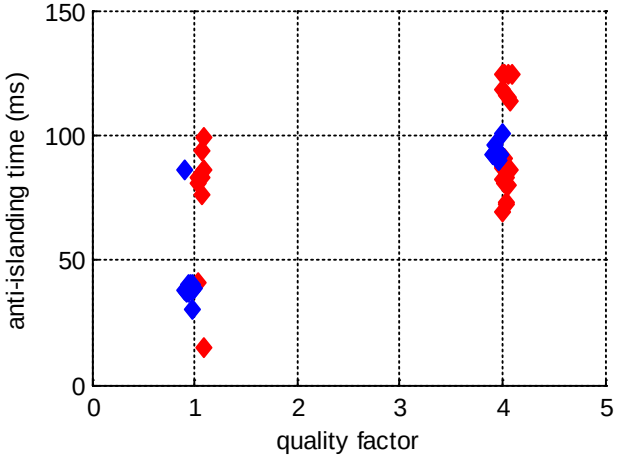


Load bank vs. ITM-PHIL



8 kW

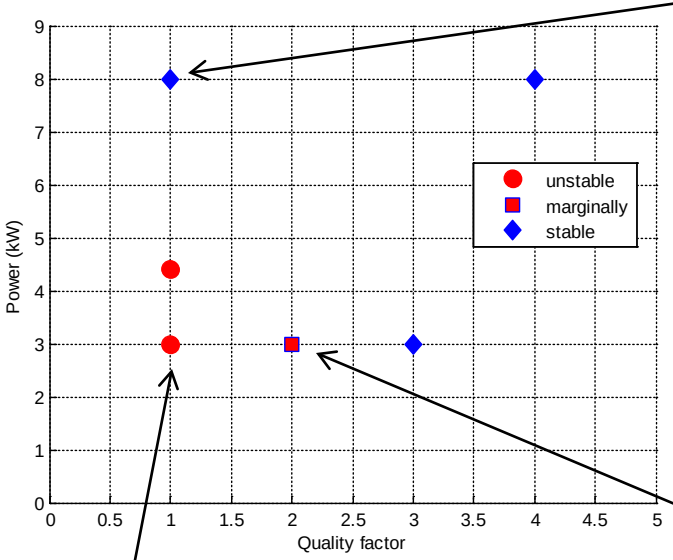


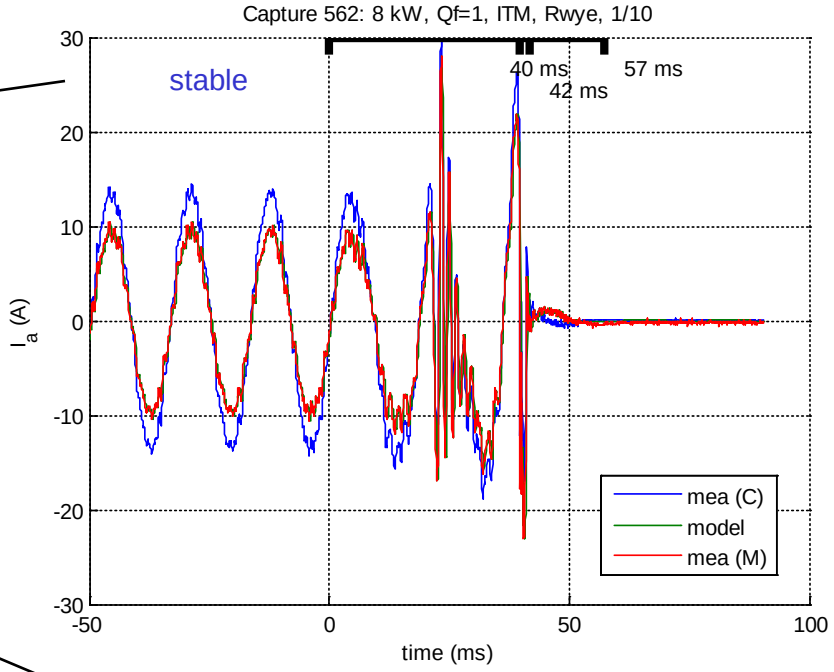


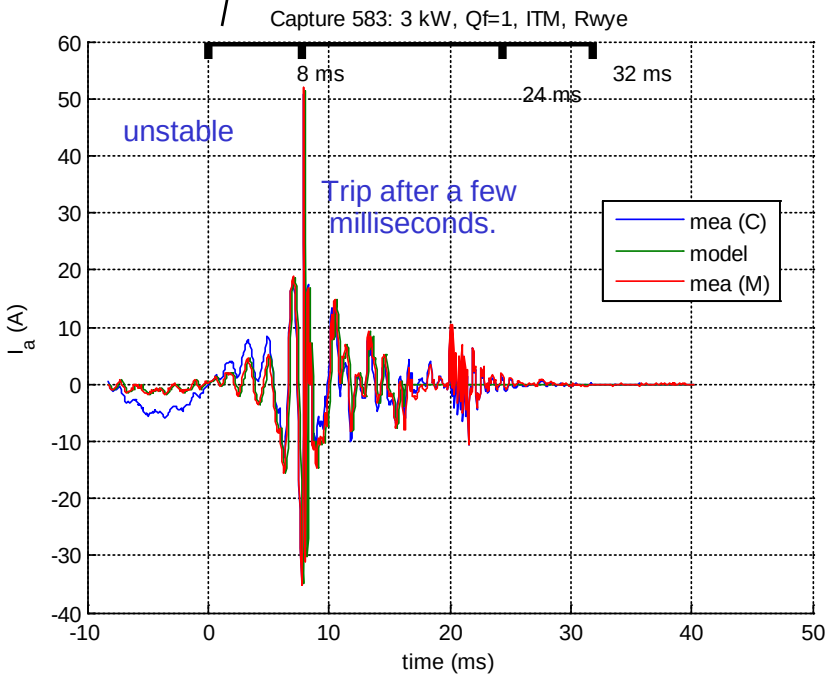
(Detection based on I_{DC})

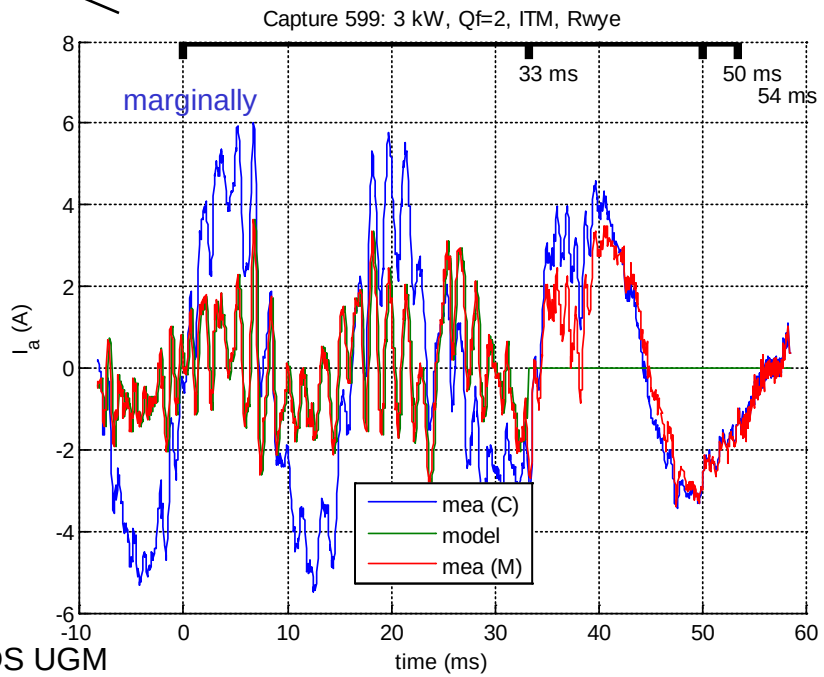
Objective: PHIL-result pattern similar to load bank derived results.

Example Traces: ITM-PHIL Stability

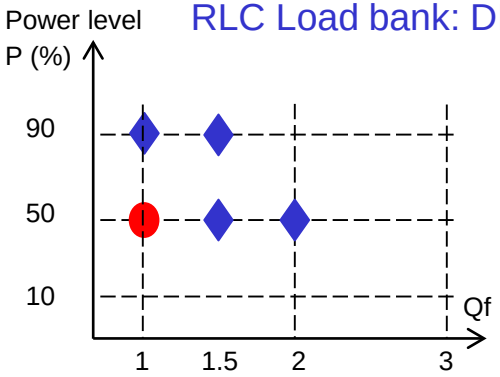


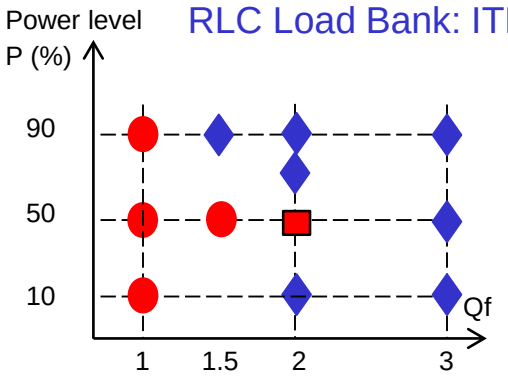


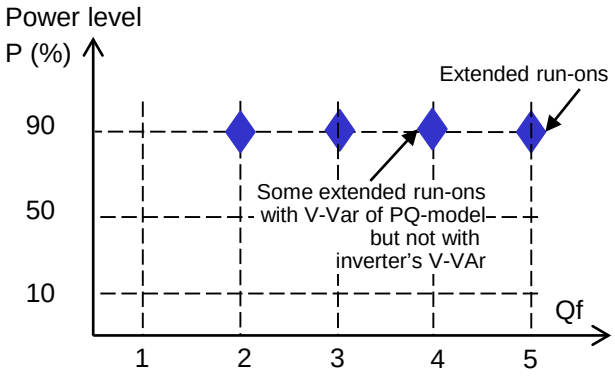


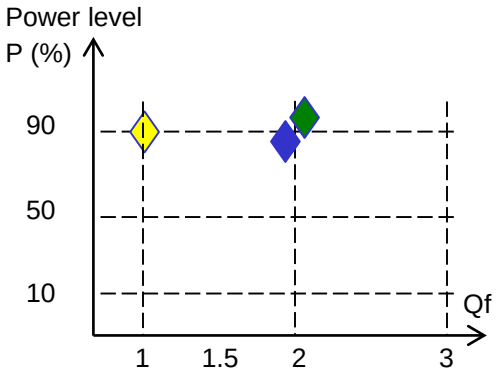


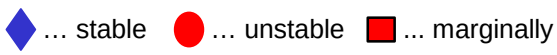
PHIL Experience and Summary

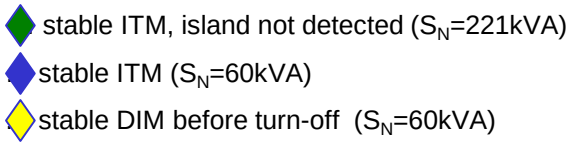












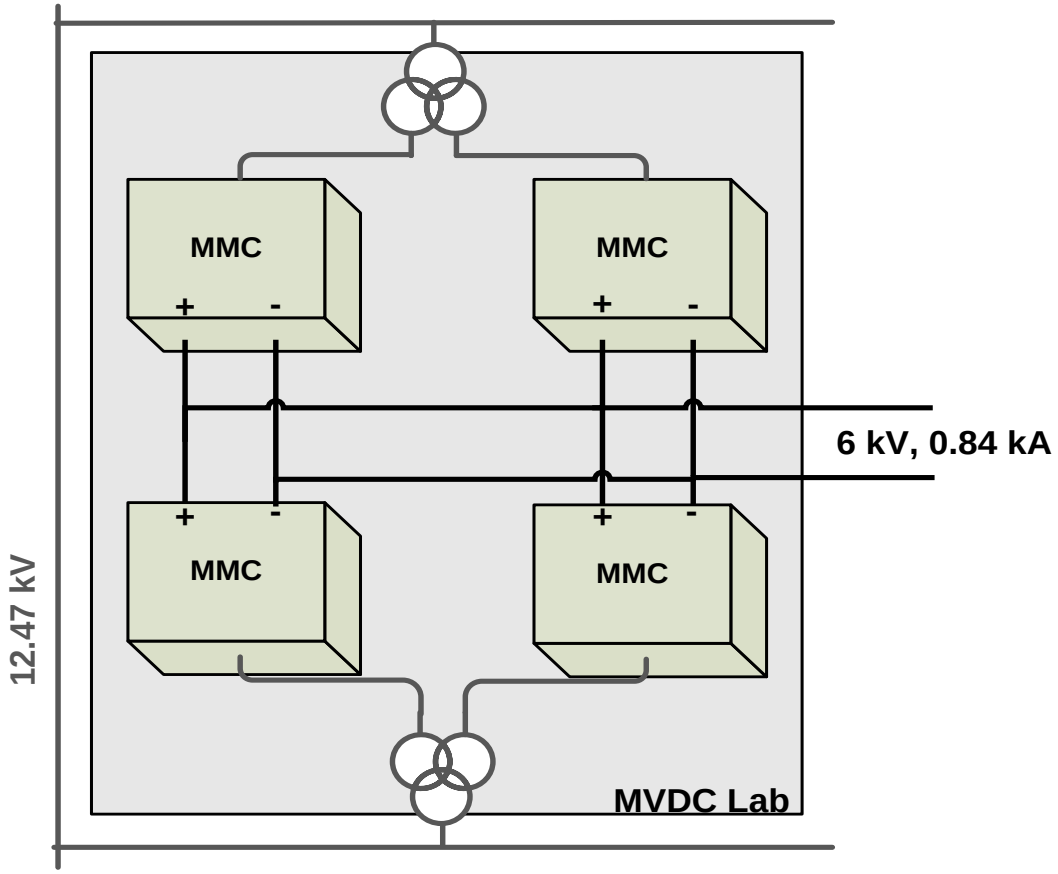
- Conditions beyond RLC load bank tested
- Flexibility of PHIL a clear benefit
- Inverters ability to detect islands when using PHIL maintained
- Need to get more robust at lower quality factors (stability an issue)
- Testing will become more challenging (in number/costs) with new advanced functions: PHIL may reduce costs

Medium Voltage DC Systems

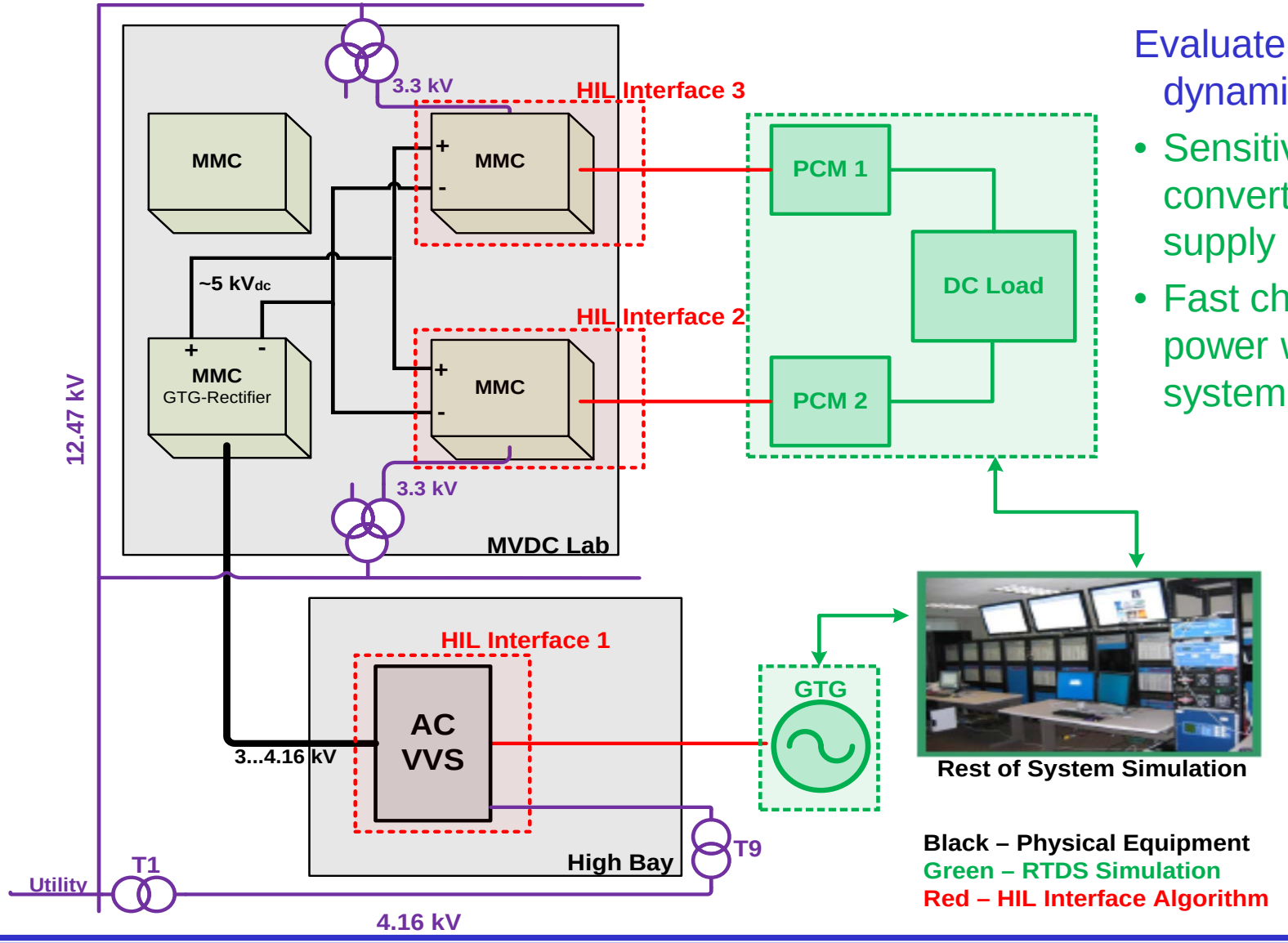
New test facility at CAPS.

- Four Modular Multi-level Converters
- Operating modes
  - individual (6 kV, 210 A)
  - series (24 kV)
  - parallel (840 A)
  - back-to-back
- Controllable from RTDS

- Application: DC microgrids



A Test Application Example



Evaluate interacting dynamic systems.

- Sensitivity of converters to AC supply deviations.
- Fast changes in power within DC system.

Black – Physical Equipment
Green – RTDS Simulation
Red – HIL Interface Algorithm

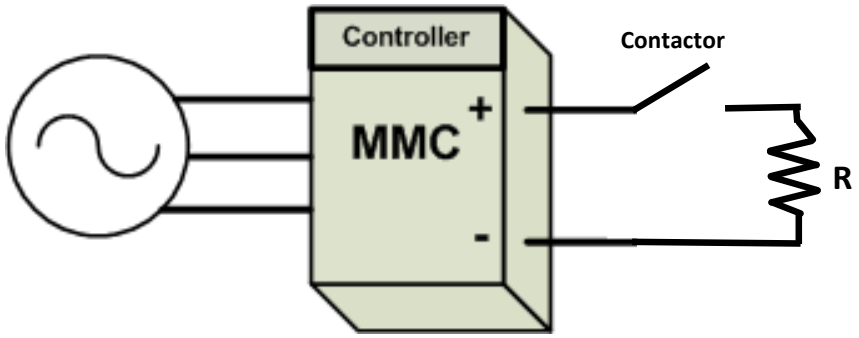
MVDC Fault Testing

Power electronics provide new means for fault handling:

- Controlled currents
- Interrupt in micro and milliseconds

Issues

- Fault behavior
- Coordination



Example test arrangement:
Closing a contactor into a Resistor

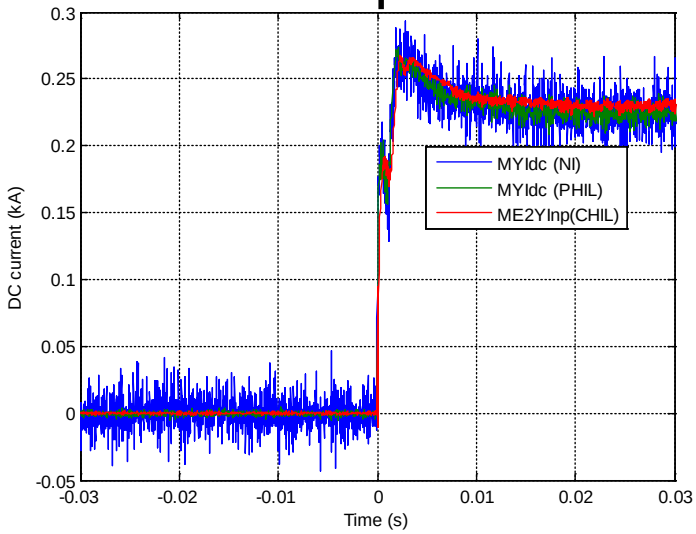
MVDC Fault Testing

Logic implemented in RTDS to drop the DC voltage **300ms** after closing the contactor.

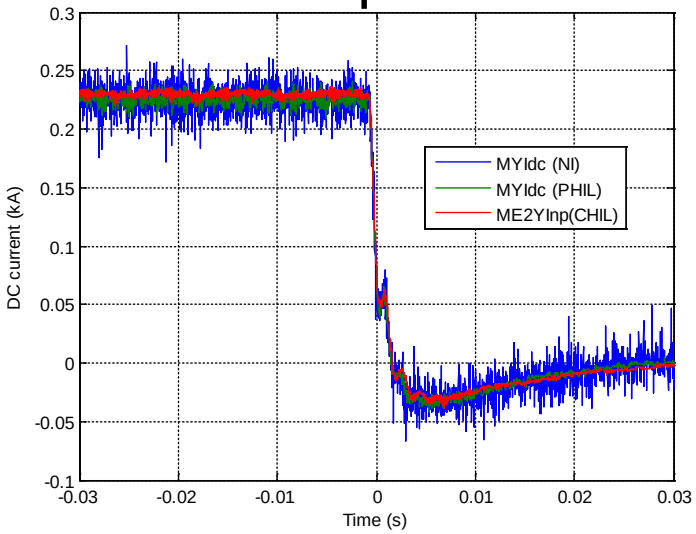
Fault applied

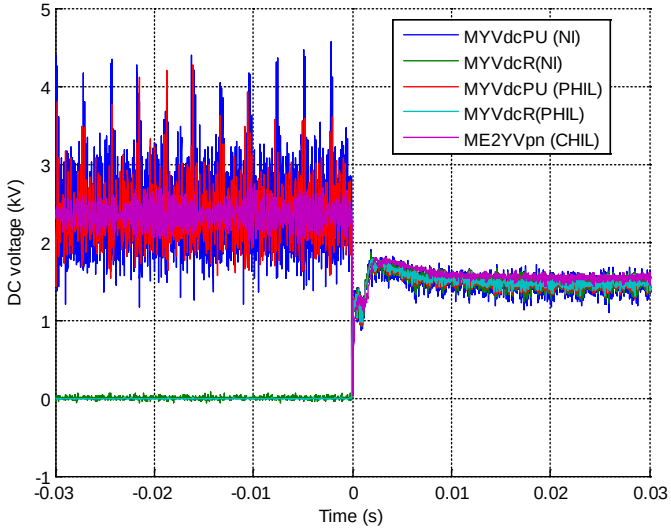
Fault cleared (controls turn-off)

time



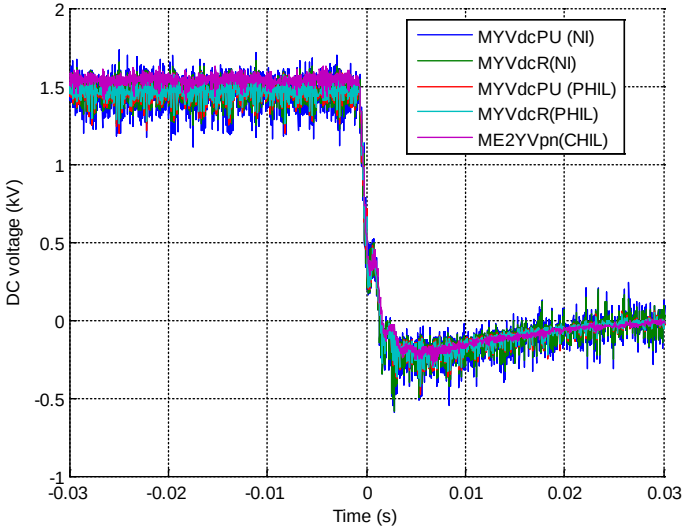
Controls respond to limit current.





DC output voltage set to 2.35 kV

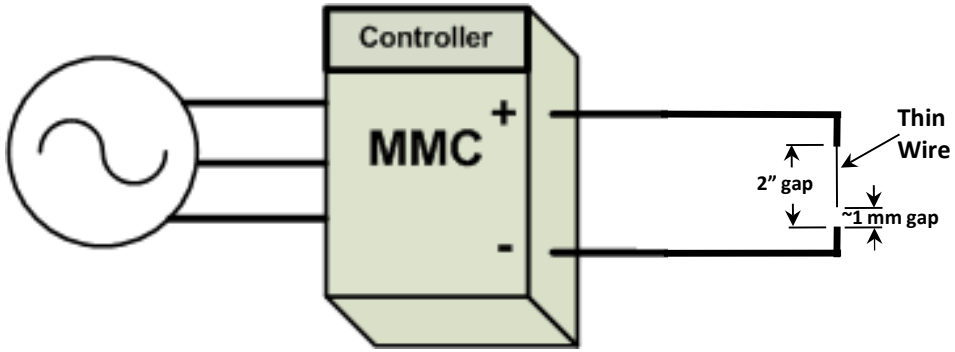
6.7 ohm resistor



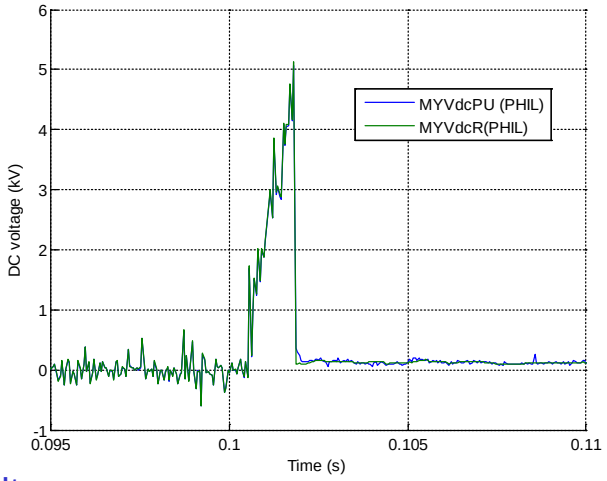
Arc Fault on DC Contacts with 2” Gap

Logic implemented in RTDS to step DC voltage from **0 to 5.5kV and back to 0V after 200ms.**

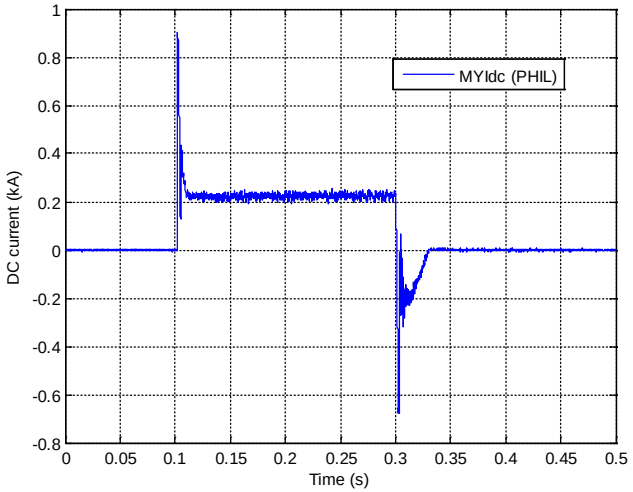
Arc fault setup with 2 inch gap between DC Rails and 1 mm gap between thin wire and negative DC Rail.



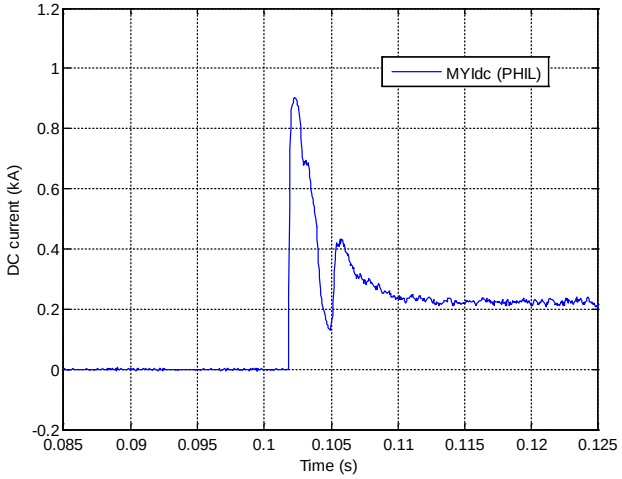
Voltage at beginning of fault condition.



Current during fault conditions.



Current at beginning of fault conditions.



Current at end of fault conditions.