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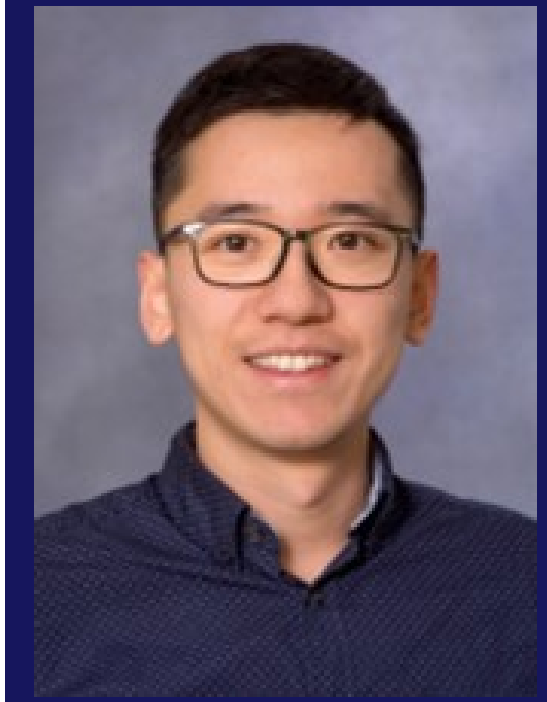
Session: 1A – Transmission Lines and Cables I

Work:



Development of Phase Domain Frequency-dependent Transmission Line Model on FPGA for Real-Time Digital Simulator

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Motivation and Objective

- Transmission Line Modelling
  - Frequency-dependent phase domain line model (FDPD)
- Processor-based FDPD Model
  - RTDS Technologies Inc. has developed a processor-based model with time-step size of 50us
- Small time-step FDPD Model
  - In HVDC-VSC simulation, the time-step is required to be relative small, for example about 3μs, to accurately simulate high frequency switching circuit.
  - FPGA has been widely used to design computationally intensive application

FPGA-based Real-time Model

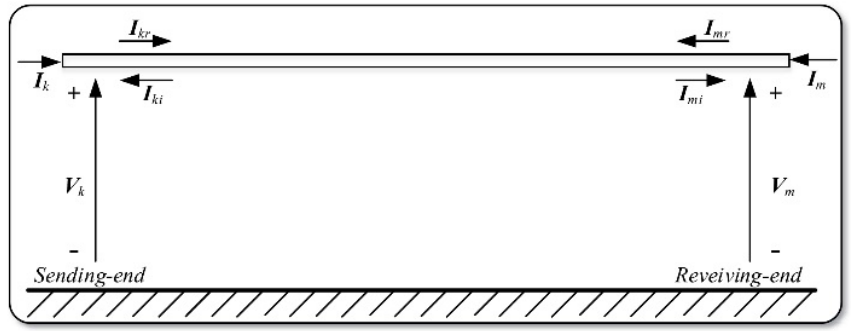
FDPD Transmission Line Model

The time domain solution

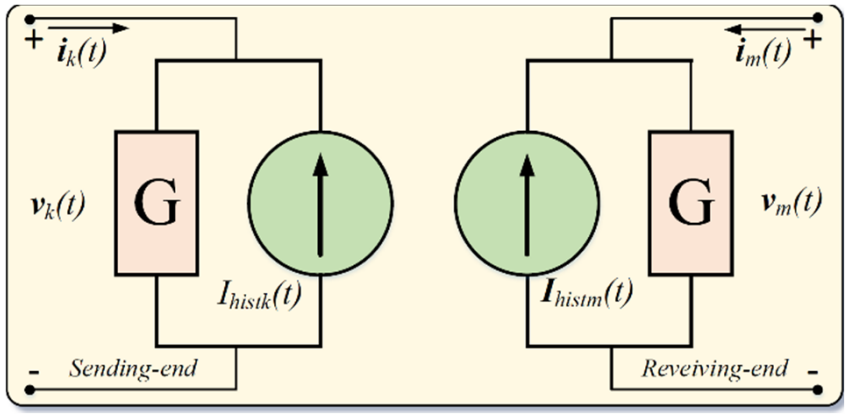
- $\boldsymbol{i}_k(t) = \boldsymbol{G} * v_k(t) - \boldsymbol{i}_{histk}(t),$ (1)
- $\boldsymbol{i}_m(t) = \boldsymbol{G} * v_m(t) - \boldsymbol{i}_{histm}(t).$ (2)

- $\boldsymbol{i}_{histk}(t) = \boldsymbol{Y_c} * v_k(t - \Delta t) - 2\boldsymbol{H} * \boldsymbol{i}_{mr}(t - \Delta t - \tau),$
- $\boldsymbol{i}_{histm}(t) = \boldsymbol{Y_c} * v_m(t - \Delta t) - 2\boldsymbol{H} * \boldsymbol{i}_{kr}(t - \Delta t - \tau).$

- $\boldsymbol{Y}_c * \boldsymbol{v}_k(t) = \boldsymbol{c}_{Yc}\boldsymbol{x}_{Yc}(t),$
- $\boldsymbol{H} * \boldsymbol{i}_{mr}(t - \tau) = \boldsymbol{c}_H\boldsymbol{x}_H(t) + \boldsymbol{G}_H\boldsymbol{i}_{mr}(t - \tau - \Delta t).$



An *n*-phase transmission line.



Norton equivalent circuit for time domain transmission line model.

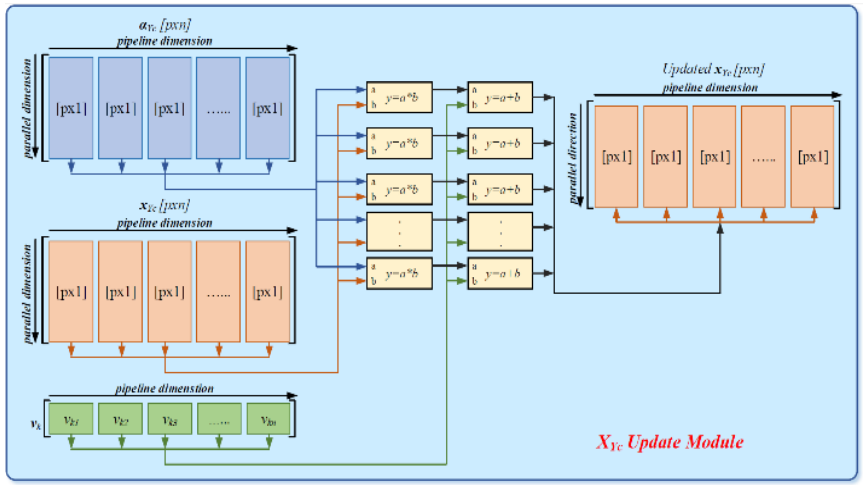
FPGA-based Real-time Model

❑ Hardware Design

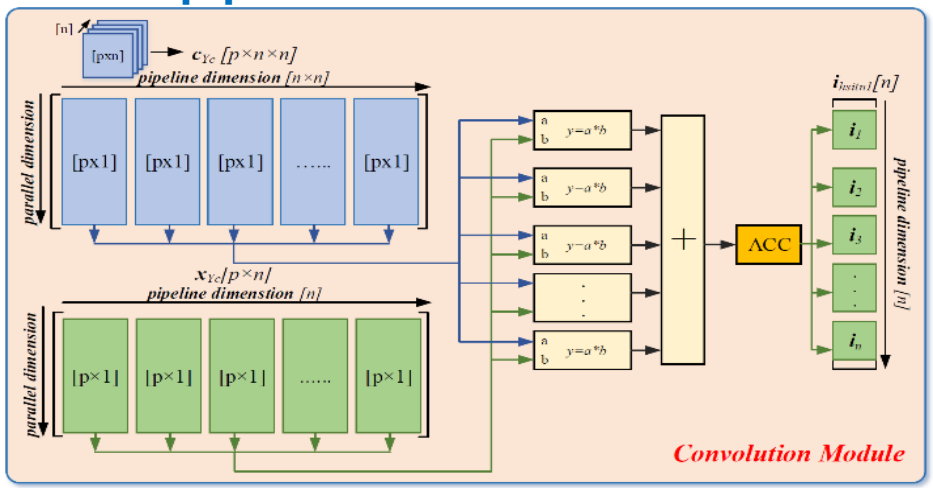
➢ Parallel Computations

- Sending-end and receiving-end calculations
- Two *update* modules are implemented to update $\boldsymbol{x}_{Yc}(t)$ and $\boldsymbol{x}_{H}(t)$
- Two *convolution* modules are implemented to calculation $\boldsymbol{Y}_c * \boldsymbol{v}_k(t)$ and $\boldsymbol{H} * \boldsymbol{i}_{mr}(t-\tau)$

➢ Within each module, all calculations are done in parallel and pipelined.



Paralleled scheme for $\boldsymbol{X}_{Yc}$ update module



Paralleled computation scheme in *Convolution* module

FPGA-based Real-time Model

- **Bergeron Interface Transmission Line**
  - To interface the FPGA-based FDPD line model to the rest of the small time-step network.
  - Has one small time-step travel time, so the FPGA can send the previous time-step injection currents to RTDS to achieved a smaller time-step (around **3.0µs**).
  - Can be removed to make a embedded model. This requires the FPGA to wait until receiving the terminal node voltage before calculation, which results in a larger time-step around **5.0µs**.

FPGA-based Real-time Model

- **Data Representation**
  - **The convolution in time domain equations require highly accurate computation**
    - **More floating-point system bits are desired**
    - **Double-precision computation is done in non real-time or large time-step real-time simulation.**
  - **Two data representations are used in the hardware design to compare the precision of the different floating-point system.**
    - **Single-precision design is implemented on Xilinx Virtex-7 FPGA VC707**
    - **Customized 48-bit precision design is implemented on UltraScale+ FPGA VCU118**

FPGA-based Real-time Model

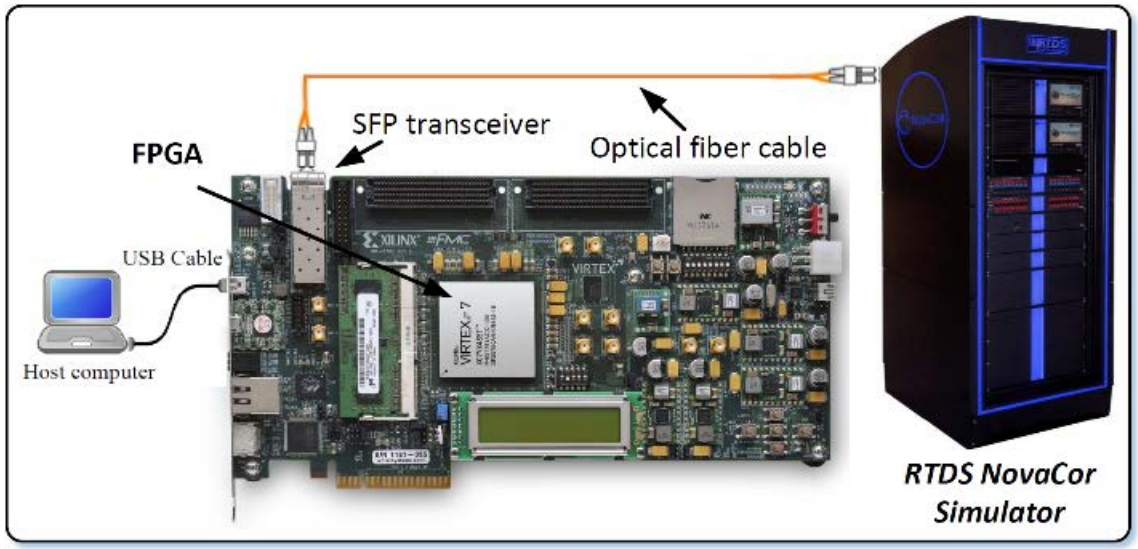
FPGA Hardware Setup with Real-time Simulator

- A optical fiber cable connected between real-time simulator and the FPGA is responsible for
  - At the case start-up, downloading the transmission line parameters to the FPGA.
  - During the simulation, exchanging the injection currents and sending the monitor signals to simulator.
- The FPGA runs at 100MHz clock

Hardware Utilization	12 Conductor Model
LUT	280958 (92.54%)
BRAM	773.5 (75.10%)
DSP48	2651 (94.68%)
FF	261639 (43.09%)
I/O	64 (9.29%)
BUFG	4 (12.5%)
GT	1 (2.86%)
Time-step	2.8µs

Hardware Utilization	12 Conductor Model
LUT	572113 (48.39%)
BRAM	1408 (65.18%)
DSP48	3220 (47.08%)
FF	454176 (19.21%)
I/O	12 (1.44%)
BUFG	39 (2.17%)
GT	1 (1.92%)
Time-step	3.27µs

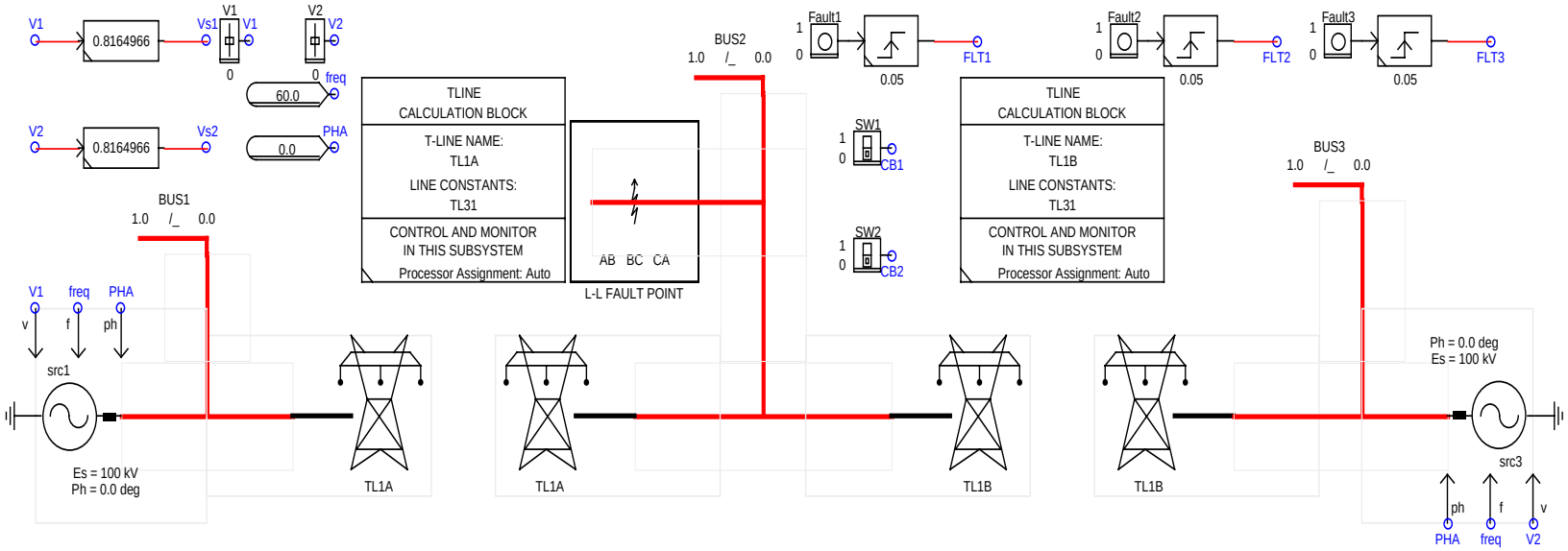
FPGA Hardware Resource Utilization On VC707 and VCU118



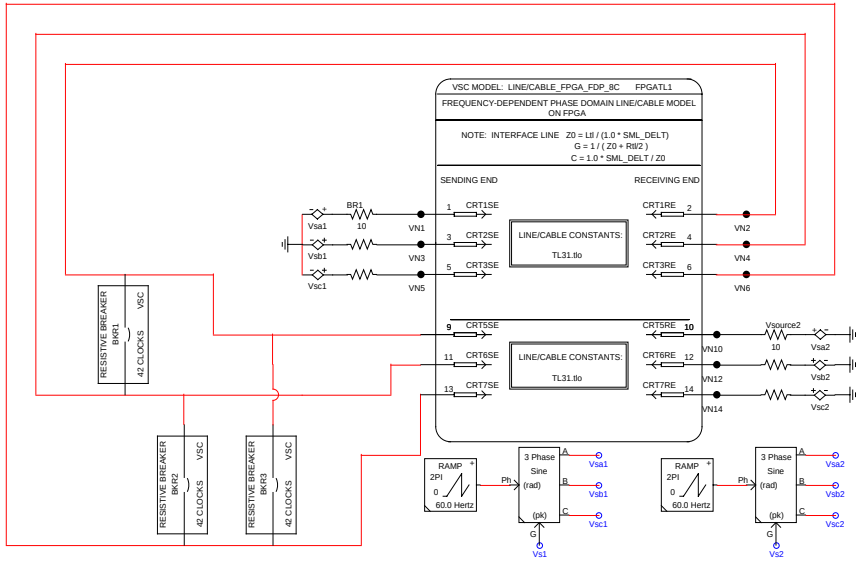
Case Study and Validation

❑ Case Study I

➢ A three-phase power system is simulated in both large time-step and small time-step



Single-line diagram in large time-step real-time simulation

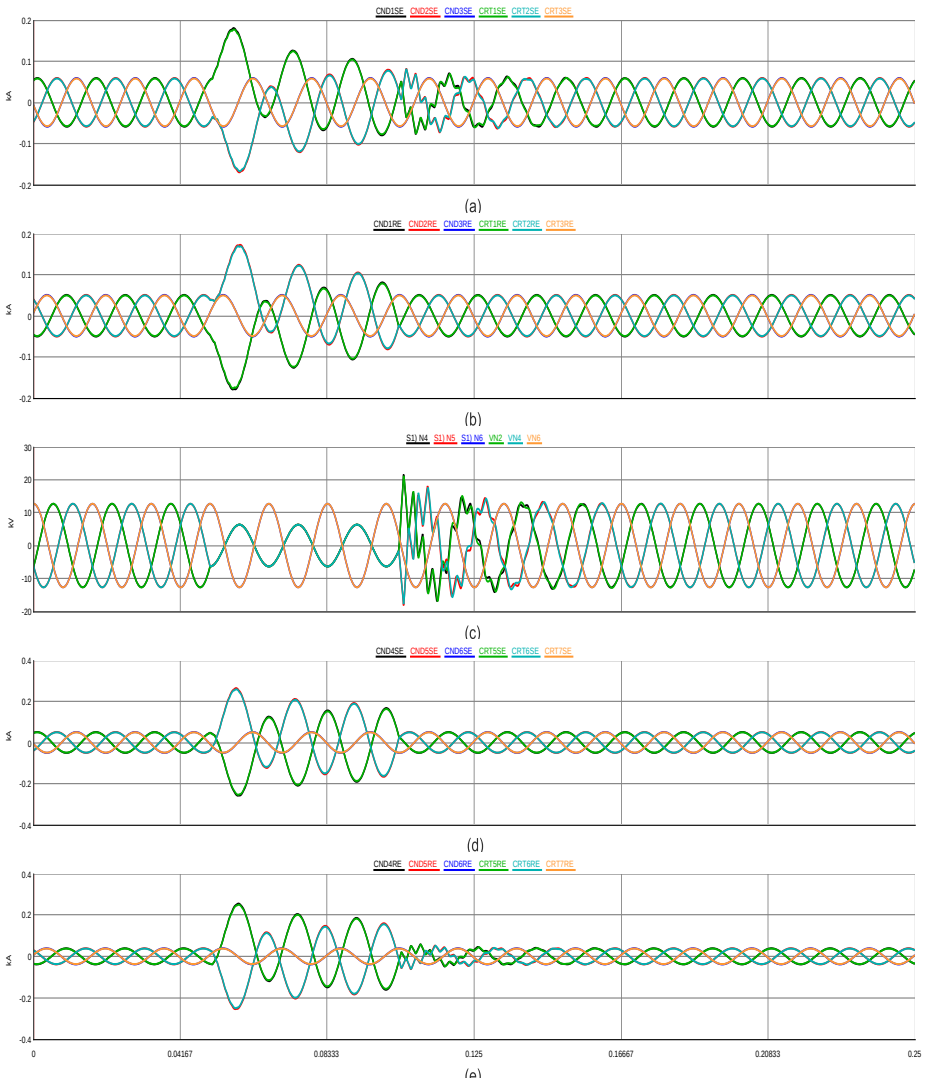


Small time-step real-time simulation

Case Study and Validation

❑ Case Study I

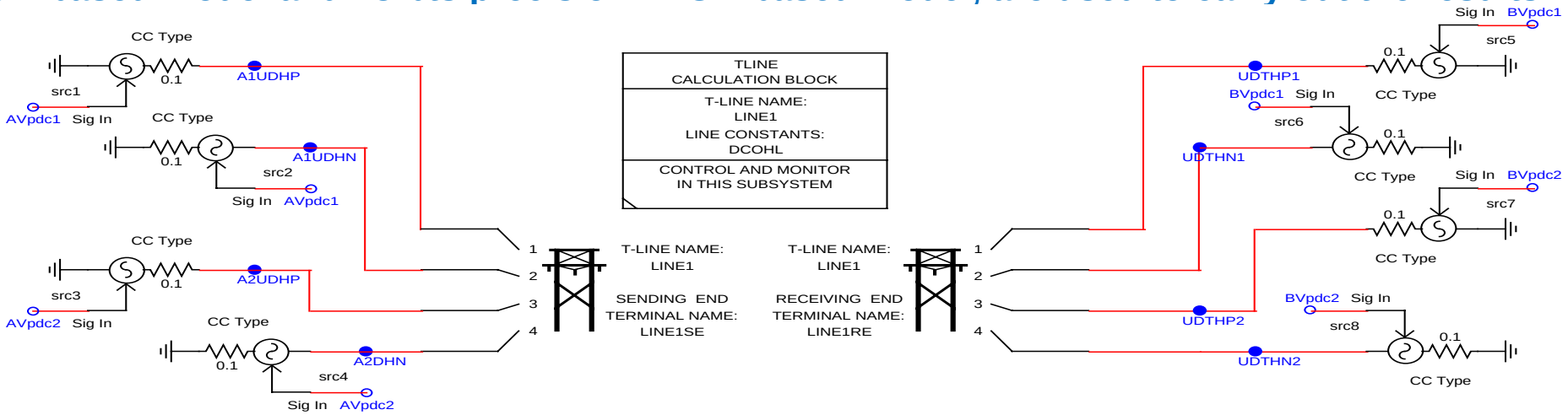
- ➢ A single phase-*a* fault is applied at the fault bus
- ➢ The three-phase voltages and current waveforms are plotted on top of each other to validate the FPGA-based model.



Case Study and Validation

Case Study II

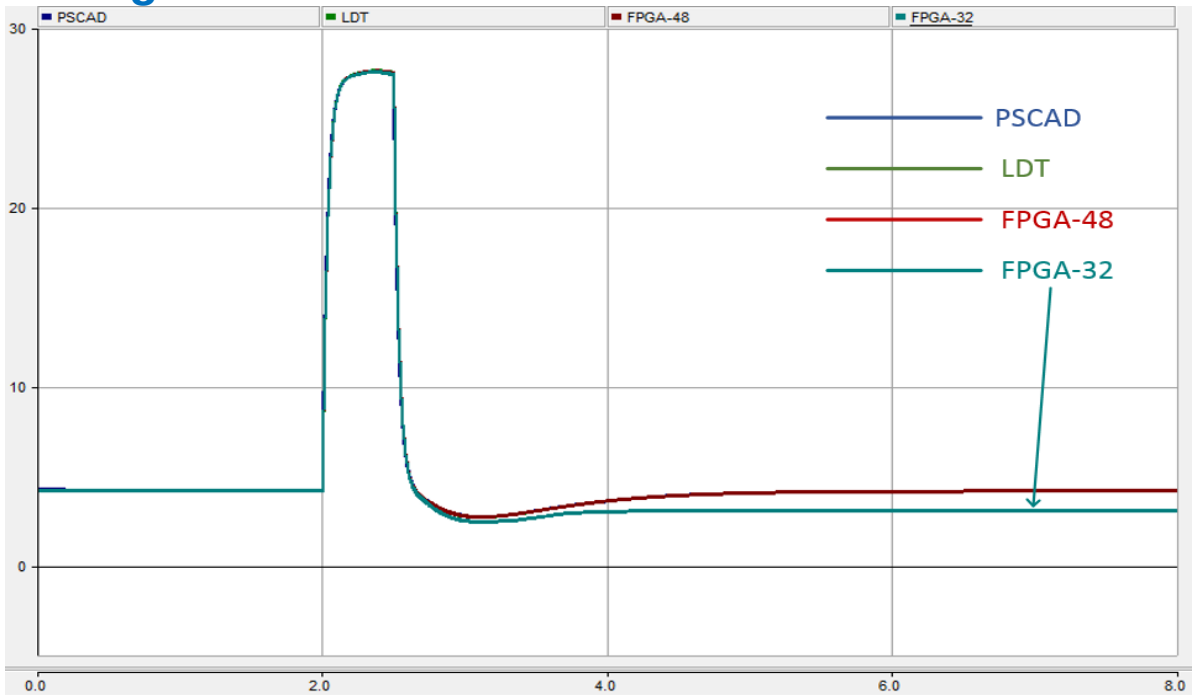
- This case study shows that the precision has a great impact on the model accuracy
- Simulation results are captured from both off-line software PSCAD and real-time simulator.
  - In the real-time simulator, different simulation model such as large time-step model, single-precision FPGA-based model and 48-bts precision FPGA-based model, are used to carry out the results.



Case Study and Validation

Case Study II

- This test is done by doing a sending-end voltage step-up and plotting the sending-end branch current waveforms together.



Case Study and Validation

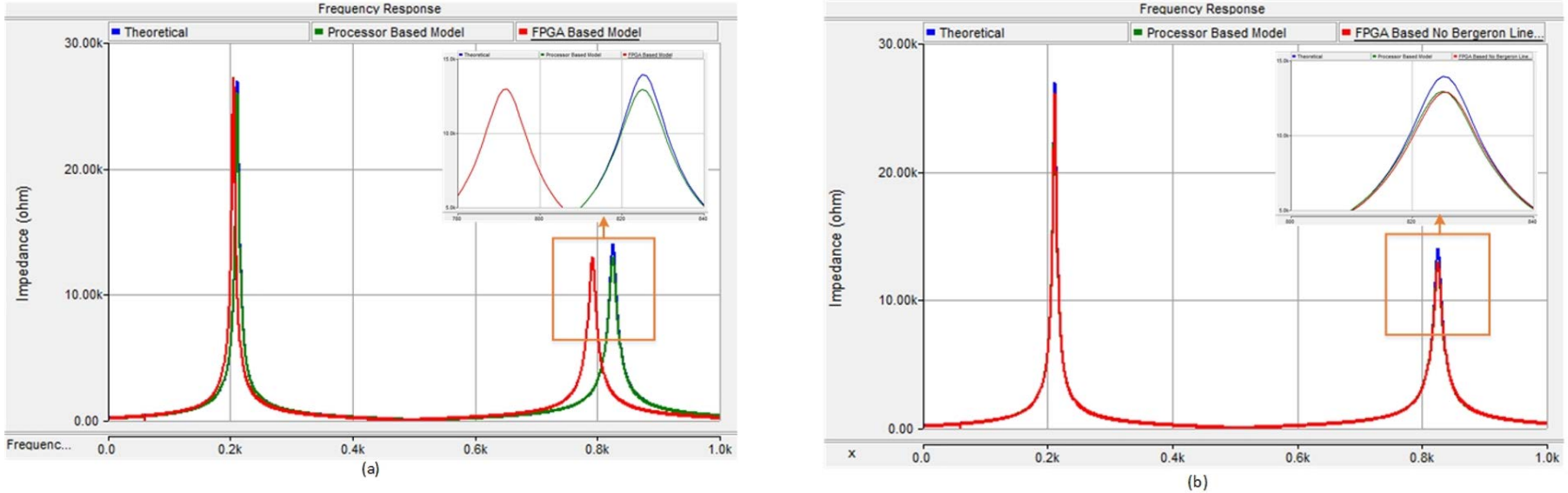
Case Study III

- Frequency response is an important concern to the power system industry due to the potential grid impact from a sudden loss of generations or loads during disturbance or restoration.
- It is necessary to investigate the frequency response of the proposed FPGA-based model, which is essentially a combination of FDPD line and interface Bergeron Line.
- Two methods are used to carry out the frequency response result in real-time simulator.
  - A frequency scan component to carry out the theoretical result in large time-step simulation.
  - A harmonic scan component to carry out the frequency response in large and small time-step simulation.

Case Study and Validation

Case Study III

- The results from 1Hz to 1000Hz of both methods are plotted
- The response of the FPGA-based embedded line model is also plotted



Frequency response results for processor-based model and (a) FPGA-based FDPD model with Bergeron interface; (b) FPGA-based FDPD model without Bergeron interface.

Conclusion

- Proposed an FPGA-based phase domain frequency-dependent transmission line model for real-time simulation.
  - Taking the natural advantage of FPGA to achieve a significantly smaller time step.
  - A customized 48-bits float point design is proposed to enhance he precision of the model.
  - Both time domain simulation and frequency scanning are used to validate the model.
  - A new option to eliminate the interface line was developed.

Questions

Thank you!

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