Webinar and Demo: The New Universal Converter Model — A Revolution in Real-Time Power Electronics Simulation

Wednesday, June 30, 2021

Questions and Answers

Please note the following errata from the webinar presentation:

- For validation of the UCM, a single-phase fault case was used (not a three-phase fault, as was erroneously mentioned in the presentation).
- For the STATCOM demo case, when Vac_ref = 1.0, the currents of the "Improved FP" with 5 µs has more non-characteristic harmonics. We are still investigating this difference.

Q1: Will the webinar recording and slides be made available?

Yes. The webinar recording and slides are available to all registrants. A link has been included with this document in the post-webinar email.

Q2: Will the demo cases be made available? How can they be accessed?

Yes. The demo cases are now available for users to access from the Downloads section of the RTDS Client Area. If you have trouble accessing the demo cases, please contact marketing@rtds.com.

The three demo cases in the folder (DAB, PMSM, and STATCOM) can all be run in RSCAD V5 (Version 5.014) with no revisions to the cases. ***However, in some situations, revisions must be made in order to run these cases in RSCAD FX (Version 1.0 or later). These changes are documented below.*** A subfolder has been included with the demo cases, which includes updated component definition files. The user can replace the existing definition files with these updates files as per the instructions below. If you have any trouble running the cases with the revisions, please contact support@rtds.com.

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1. For users running the STATCOM case in RSCAD FX:

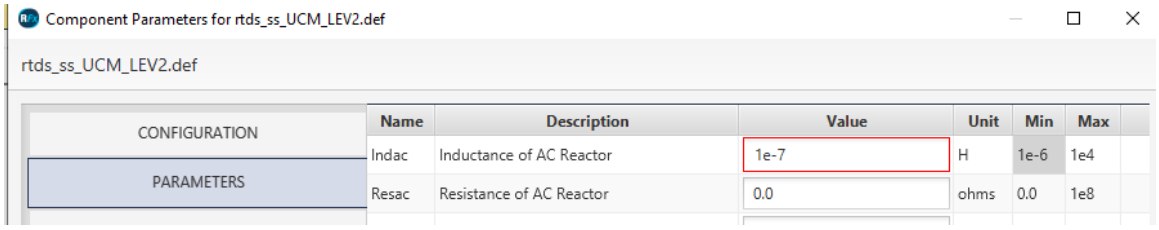
No changes are necessary if the switching frequency is less than 5.001 kHz. If the switching frequency is higher than 8.8 kHz, then the UCM_FP issues an error indicating that the switching frequency draft variable cannot be changed to 50 kHz (as shown in the demo). This error is being debugged and will be resolved in the next RSCAD FX version release.

If users want a switching frequency between 5.001 kHz and 8.8 kHz, they should remove the maximum limit of the **rtds_sharc_ctl_ARAMP** component by replacing the component definition file. Use the updated ARAMP definition file provided in the folder, and replace the existing definition file (location may vary depending on installation, but will likely be similar to the following):

C:\RSCAD_6\RSCAD FX 1.1\MLIB\COMPONENTS\CONTROLS\SIGNAL GENERATORS

2. For users running the DAB case in RSCAD FX:

No changes are necessary if no parameters are being changed. For the two level UCM converter, the inductance must be changed if other parameters are being changed. The value should be changed in the component as shown below.



To accommodate a new minimum of 1e-8, the component definition file for **rtds_ss_UCM_LEV2.def** must also be replaced with the new one in the folder. The location may vary but will be similar to:

C:\RSCAD_6\RSCAD FX 1.1\MLIB\COMPONENTS\Substep\POWER ELECTRONICS

3. For users running the PMSM case in RSCAD FX:

If running in FX 1.0, the PMSM “dL” should be changed to 10000 as shown below. This has been changed in FX 1.1.

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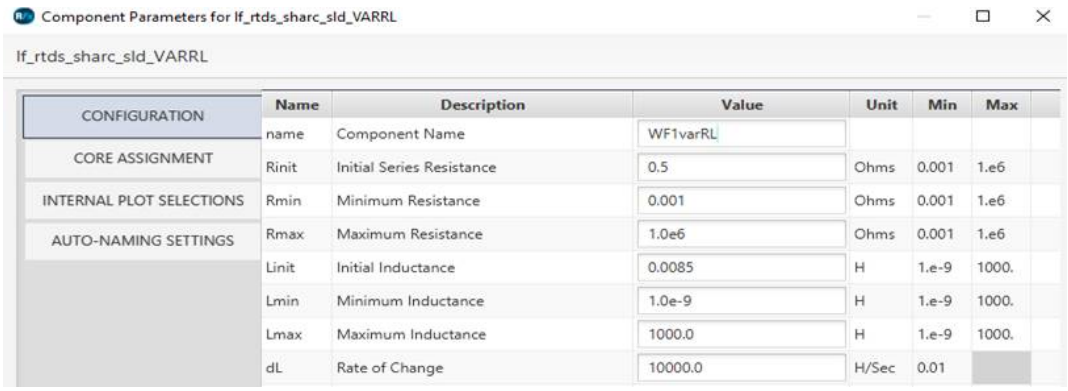

The **lf_rtds_sharc_sld_VARRL** component definition file must also be replaced with the new one in the folder. The location may vary but will be similar to:

C:\RSCAD_6\RSCAD FX 1.1\MLIB\COMPONENTS\POWER SYSTEM\PASSIVE

Q3: If I am understanding it correctly, the new UCM approach is the preferable method for nearly all application areas other than if you need to represent internal device failures within the converters themselves, is this correct? In other words, even for HIL testing of external firing controls, unless you want to include the impact of power electronic device failures, this type of converter model is preferable?

You are correct. The UCM (and, in particular, the Improved Firing input) is now generally preferred and recommended by RTDS Technologies for simulation and testing, due to the advantages presented in the webinar and demo cases.

For regular firing pulse input, we have validated our UCM models against our existing Substep resistive converter model and the performance is similar or better. We have not yet encountered a specific scenario where the UCM shouldn't be used.

Q4: Will it be possible to model MMCs with the UCM?

The UCM is currently not available for an MMC configuration and it will likely remain that way in the future. The UCM is more intended for drives, converter-interfaced generation and resources, modelling solid state and DC/DC transformers, etc. We don't currently see any motivation for modelling MMC valve models with UCM method, as our existing FPGA- and processor-based MMC models work well and are widely used in industry testing.

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Additionally, MMC valves do not need the added firing accuracy of the UCM as they are not typically switched at the high frequencies that motivated the UCM's development.

Q5: What about the amount of cores that has to be locked in Novacor chassis for a typical MMC device representation/execution (two to four hundred of submodules per arm) in the Substep environment? And under which situations is it more proper, in terms of hardware consumption, to represent the MMC valve model either by CPU cores or FPGA board?

Detailed information about modelling MMCs is out of the scope of this webinar as the UCM is currently not planned for MMC valve modelling. However: the MMC valve model you choose (FPGA-based vs. processor-based) is motivated by the level of detail that is required and the type of studies or testing you are doing. For systems of 200-400 submodules per arm, you would be choosing between the processor-based MMC5 model and the FPGA-based models (U5 and GM). MMC5 runs in the Substep on NovaCor without FPGA involvement, but it includes automatic balancing of SM capacitor voltages and requires only a modulation waveform. So, it cannot be used for firing pulse / submodule voltage level control testing. The FPGA-based hardware is therefore required if the user is doing low-level control studies.

It should also be noted that we have not changed our strategy on the use of FPGAs. When external controls at the firing pulses level are being tested, we use the FPGA to model MMC valves. That strategy is the same for the small timestep and Substep environments – the only difference is that Substep is easier to use and more accurate.

In terms of hardware allocation, if you are using the processor-based MMC5 model for example, a simple point-to-point case could theoretically be run on two cores (one core running the valve models, lines, sources, and other power system components, and one core mainly responsible for the controls). If you have allocation questions about a specific circuit, please send us an email at marketing@rtds.com.

Q6: Is the new GTDI V2 card a firmware update on the existing GTDI card, or a complete new hardware design?

What we presented in the webinar, the GTDI V2, is a complete new hardware design (with a new form factor - slightly smaller than the previous-generation GTDI card). However, we are also currently evaluating whether we can implement a new firmware version for the existing GTDI V1 card. This would allow users with the existing card to use the UCM's Improved Firing

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input with external controllers. We will keep users updated on this via our email subscription list and the RSCAD release notes.

Q7: In the Substep environment, 60 nodes are allowed. So, can I use multiple Substep subsystems if I want to model more than 60 nodes? (Also asked: Hay alguna forma de dividir un bloco de substep para evitar overruns / Is there a way to divide the Substep block to avoid overruns?)

Yes. You can connect multiple Substep boxes via a travelling wave interface to simulate a larger power electronic circuit. Note that each Substep subnetwork requires its own dedicated core. Also, the size of the Substep timestep must be the same for both subnetworks. For more information, check the Substep manual in RSCAD.

Q8: I assume that if you change from the UCM's firing pulse input to modulation wave input, each converter will require less processing power to solve on the simulator?

There is actually no real difference in computational burden. In the Substep environment, the UCM has the same computational load whether regular firing pulse, Improved Firing, or modulation input is used. In the Mainstep environment, each UCM placed in the case requires 10 Load Units, regardless of the input type used.

Another point of interest is that we have to model the converters in blocked and deblocked modes. In blocked mode, the computational burden is actually heavier – this is the computational bottleneck.

Q9: What's the limitation for switching frequency for DAB? Is 50 kHz possible with a low phase shift like 5 degrees? Just trying to understand the limitation here.

We tried to increase the switching frequency to 50 kHz based on our DAB demo case.
Here are the parameters we need to change:
1, the switching frequency of triangular waveform in "Firing Pulse Generator" to 50000 Hz.
2, the high-frequency transformer leakage to 0.086 pu;
3, the inductance of low-voltage side converter to 3e-8 H.
4, the MainStep size to 55us, the DAB simulation time step is 55/40=1.375us.

Here is the simulation results. We could control the output voltage to 1.4 Volts. The phase delay is 6.308 degree.

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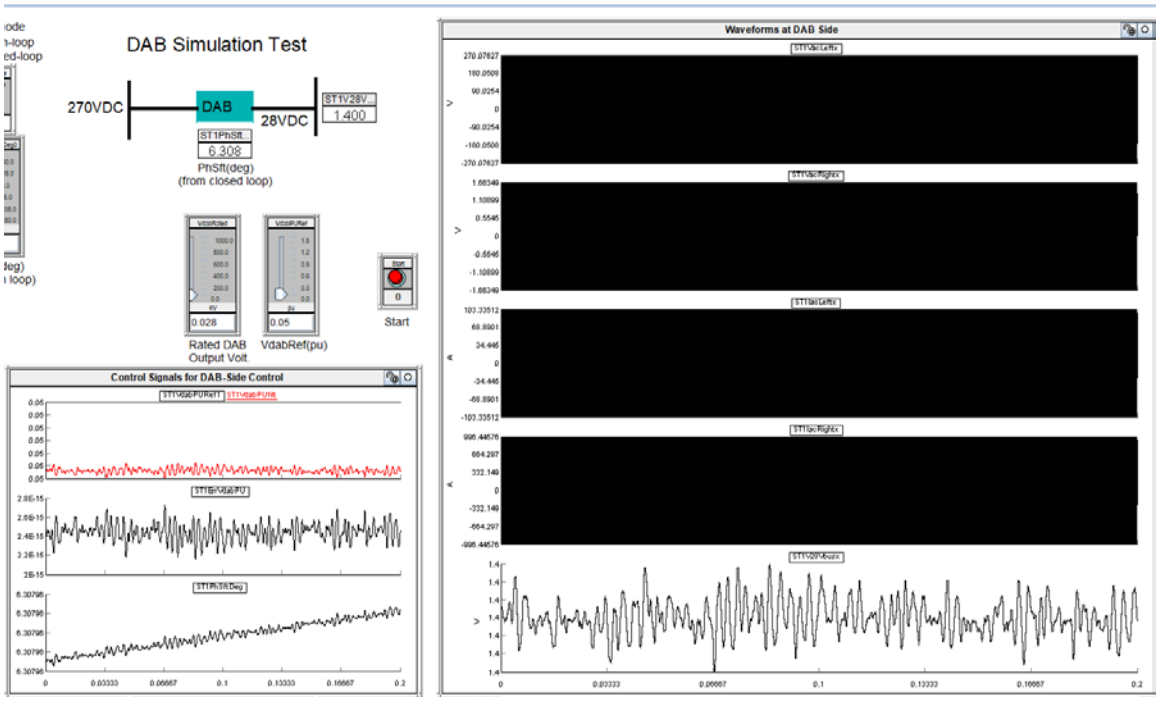
We are not clear the limits of the switching frequency. But the higher the switching frequency is, the larger the phase delay is needed in the simulation (larger than the theoretical value). This may be caused by the resolution of the firing pulse generator.



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