Enhanced Transformer Differential Protection – Design, Test and Field Experience

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Abstract:

Transformer differential protection normally use dual slope or multiple slope characteristics to provide stability during through fault and load conditions. It also uses harmonic blocking criteria to provide stability during various transformer inrush conditions. The advancement in the materials used in transformers can cause a reduction in harmonics during a transformer inrush which can lead to reduced 2nd harmonic settings down to 10% or lower in some applications. This paper discusses the impact of a reduced 2nd harmonic threshold on the differential protection and highlights the benefits of waveform recognition algorithms such as the gap detection and the CT saturation techniques to unblock the differential protection during internal faults in the presence of harmonics. It also highlights the benefits of an adaptive transient bias technique to provide high stability during through fault scenarios and includes results of extensive RTDS testing and some of field performance examples.

1. Introduction

Traditional protection schemes use dual slope or multiple slope characteristics to provide stability during CT saturation, together with second harmonic as a restraining or blocking quantity for inrush conditions. However, studies have shown that there is a limitation with the dual slope characteristic for stability, to avoid requiring excessive over-dimensioning of the CTs. The second harmonic blocking has also been shown to slow down the protection for internal faults if CT saturation occurs. This is because CT saturated waveforms can also contain a high second harmonic component. Early studies on magnetising inrush currents indicate that the second harmonic content might be 15% or more of the fundamental current [3]. Recent studies indicate that improvements in the transformer design and core steel can result in a low content of second harmonic (as low as 7%) [3].

This paper highlights a novel transient bias technique for high stability during through faults and a no gap and CT Saturation technique to unblock the differential protection during internal faults for faster clearance even in the presence of harmonics generated during CT saturation. A transient bias algorithm increases the operating threshold momentarily when there is a sudden increase in the bias current, thus enhancing stability during external faults. This approach will not affect the performance during internal faults, since the differential current will rise much faster than the bias currents.

2. Stability during external faults

To provide further stability for external faults, additional measures are considered on the calculation of the bias current: delayed bias, maximum bias and transient bias.

The delayed bias is calculated on a per phase basis and it is the maximum of the fundamental bias quantities calculated within the last cycle. The delayed bias provides added stability when an external fault is cleared and the fault currents drop off.

$$I_{bias\,A\_delayed} = \text{Maximum}\,[I_{bias,A(n)}, I_{bias,A\,(n-1)}, I_{bias,A\,(n-(k-1))}] \quad (1)$$

$$I_{bias\,B\_delayed} = \text{Maximum}\,[I_{bias,B(n)}, I_{bias,B\,(n-1)}, I_{bias,B\,(n-(k-1))}] \quad (2)$$

$$I_{bias\,C\_delayed} = \text{Maximum}\,[I_{bias,C(n)}, I_{bias,C\,(n-1)}, I_{bias,C\,(n-(k-1))}] \quad (3)$$

The maximum bias is the maximum of the delayed bias currents from all three phases. The maximum bias is used to prevent maloperation under external faults conditions, when spill current could flow into the CT of a healthy phase, if the CT is partially saturated.

$$I_{bias,max} = \text{Maximum}\,[I_{biasA\_delayed}, I_{bias,B\_delayed}, I_{bias,C\_delayed}] \quad (4)$$

The maximum bias is used to calculate the differential operating current Iop, using the following equations by considering the multiple slope characteristic shown in Tripping characteristic of differential protection.

Characteristic equation for range:

$$0 \le I_{bias,\max} \le \frac{I_{s1}}{K_1} \tag{5}$$

$$\mathrm{Iop} = \mathrm{I_{s1}} \tag{6}$$

Characteristic equation for range

$$\frac{I_{s1}}{K_1} \le I_{bias,\max} \le I_{s2} \tag{7}$$

$$Iop = K_1 \cdot I_{bias,\max} \tag{8}$$

Characteristic equation for range:

$$\mathrm{I_{bias}} \ge \mathrm{I_{s2}} \tag{9}$$

$$Iop = K_1 \cdot I_{s2} + K_2\left(I_{bias,\max} - I_{s2}\right) \tag{10}$$

K_1: characteristic slope in range (11)

K_2: characteristic slope in range (12)

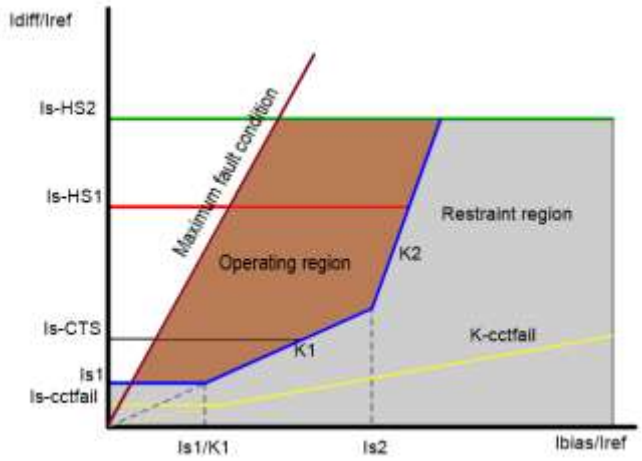

Figure 1 Tripping characteristic of differential protection

The transient bias is introduced when there is a sudden increase in the mean bias measurement or the activation of the external fault detector. The external fault detection technique considers the time to saturation. As soon as an external fault occurs, the bias current changes, but the differential current only increases after the time to saturation. The external fault detection algorithm is on a per phase basis. Once the transient bias is introduced, it decays exponentially and it resets to zero once the relay trips, or if the mean bias quantity is below the restrained element setting. A phase comparison algorithm is also used to disable the transient bias during some evolving fault conditions. The operating current threshold is calculated at the maximum bias current. The transient bias is calculated on a per phase basis and it is added to the operating current calculated at the maximum bias. Therefore, the following differential current thresholds are available:

Diff threshold phase A = Iop at (max bias + transient bias)_phase A (13)

Diff threshold phase B = Iop at (max bias + transient bias)_phase B (14)

Diff threshold phase C = Iop at (max bias + transient bias)_phase C (15)

The differential current is compared against the differential current threshold given above on a per phase basis. If the differential current is above the threshold, the biased differential element will trip as long as the second harmonic and fifth harmonic blocking elements are not asserted.

The transient bias technique considers a time decay constant, stability coefficients and the differential function settings to provide a dynamic bias characteristic.
Figure 2 shows the differential thresholds calculated by the relay on a per phase basis for a phase A-N external fault on the star side of a Ynd11 transformer. It can be observed that the transient bias has enhanced relay stability. For the relay to trip, the differential current should be above the operating current at max bias + transient bias.

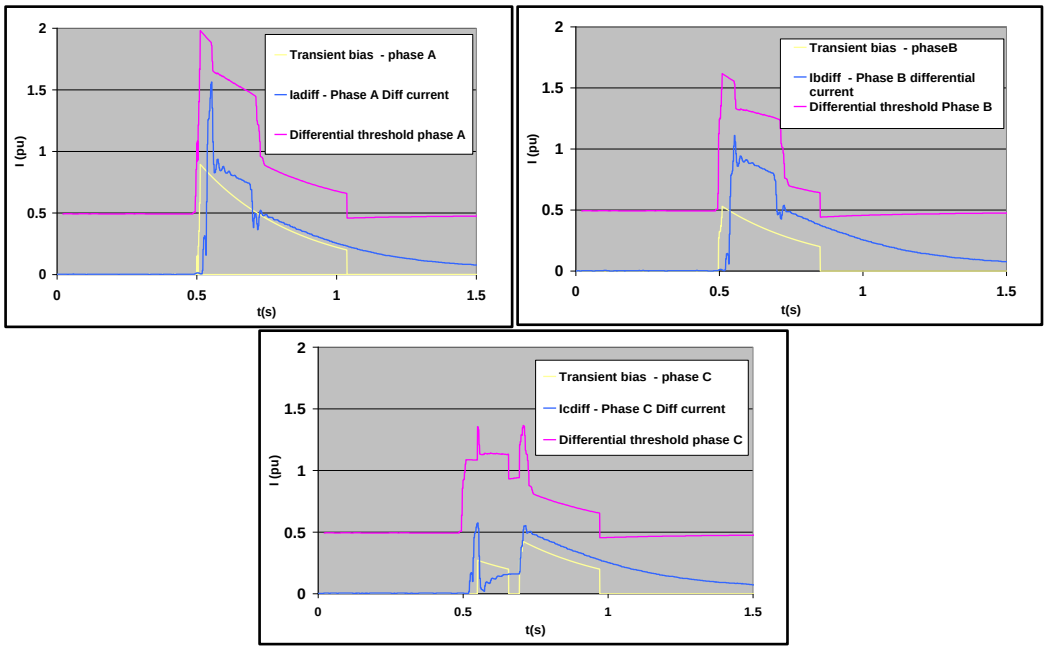

Figure 2 Transient bias – external fault

Differential characteristic with transient bias – external faultshows the nominal biased characteristic, the dynamic threshold and the differential current loci. The differential currents increment from A to B, meanwhile the differential current thresholds also increase from A' to B'. It can be observed that considering the nominal characteristic for phases A and B there could be a mal-operation because Iadiff and Ibdiff are above the nominal characteristic. Taking into account the transient bias quantities prevents an unwanted trip because Iadiff and Ibdiff are below the dynamic threshold. From B to C the differential currents are below the dynamic threshold from B' to C'.

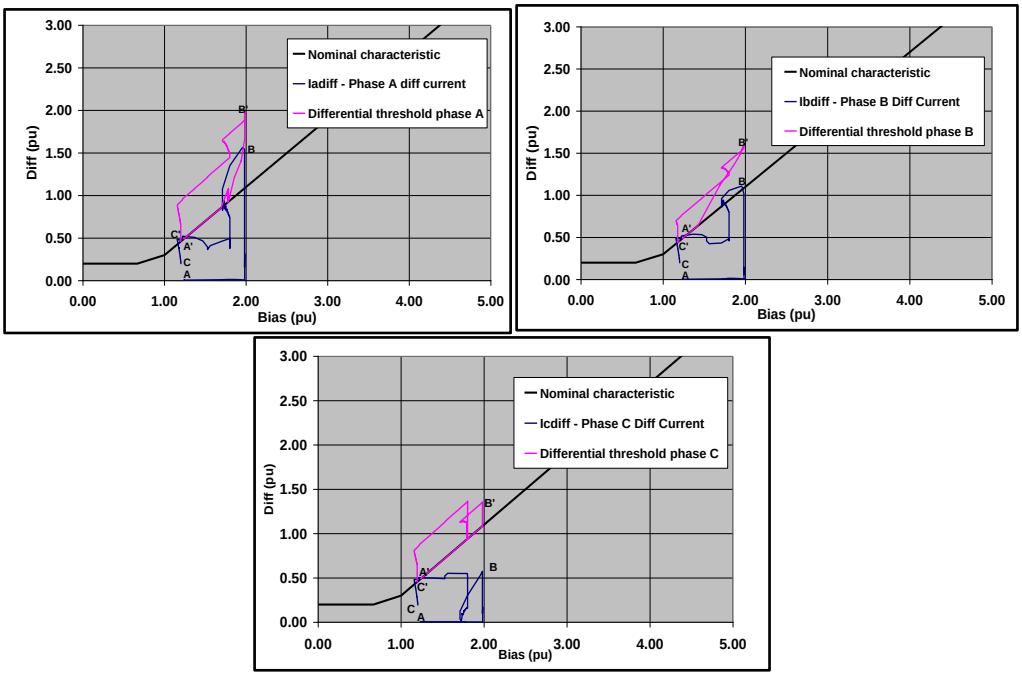

Figure 3 Differential characteristic with transient bias – external fault

The transient bias enhances the stability of the differential element during external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios. For single-end or double-end fed faults the differential current is dominant and the transient bias has no effect.

Figure 4 shows the differential thresholds calculated by the relay on a per phase basis for a BN internal fault on the delta side of a Ynd11 transformer. The transient bias does not prevent the operation of the differential element as the differential current is above the operating current at max bias + transient bias.

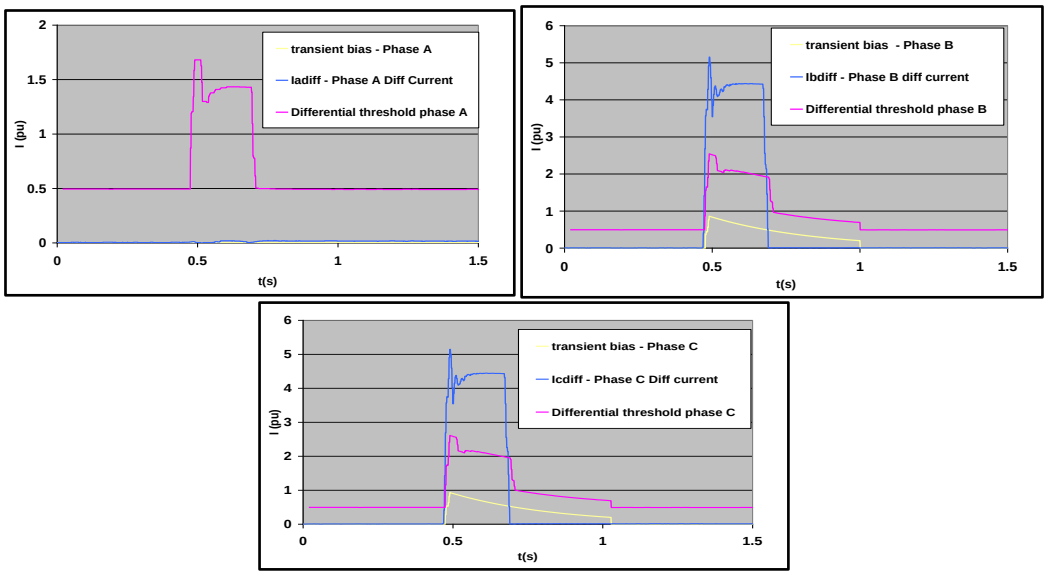

Figure 4 Transient bias – internal fault

Transient bias – differential characteristic – internal fault shows that the dynamic threshold coincides with the nominal characteristic because the transient bias for phase A is zero. For phases B and C the operating currents have been increased due to the transient bias, but since this is an internal fault the dynamic thresholds are well below the differential current loci.

No transient bias is produced under load switching conditions. Also, no transient bias is generated when the CT comes out of saturation.
It is setting less (no setting required) and automatically calculates the amount of transient bias to be added for higher security during through faults.

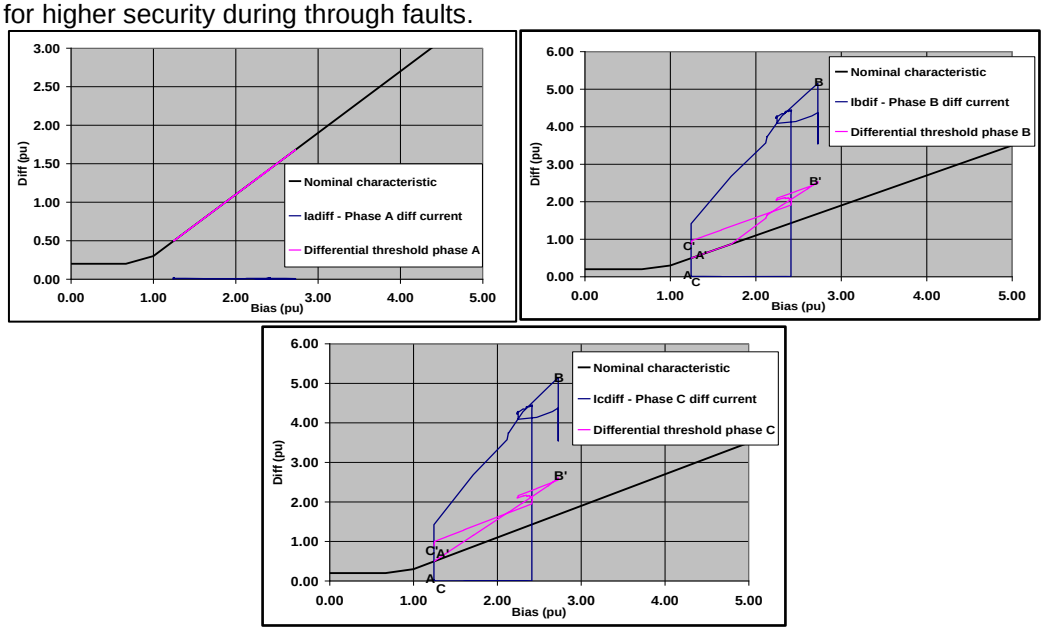

Figure 5 Transient bias – differential characteristic – internal fault

3. Field performance details with transient bias enabled and disabled

Figure 6 shows details for the differential protection of a 65.3 MVA, 132 kV/13.8 Kv transformer. Magnitude and vector compensation in the relay are calculated automatically based on the CT ratio, MVA rating, HV voltage and LV voltage. The full load current of the transformer on the HV and LV side is 285.62 A and 2732.03 A respectively.

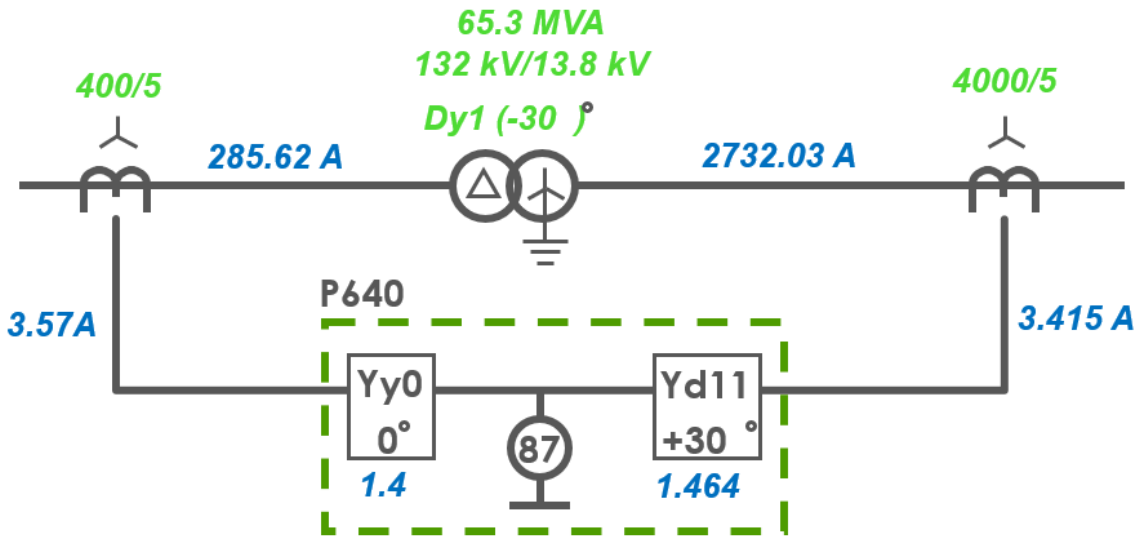

Figure 6 Differential protection using MiCOM P64x

Figure 7 shows the disturbance record for current captured during transformer loading by closing the LV breaker. The energisation of the transformer from the HV breaker was successful and as seen in the record, on closing of the LV breaker an increase in currents is observed on both the HV and LV side simultaneously. It also shows a large difference in the first and second peak of A phase current which could not be due to the primary load current. IN Hv in figure 7 is the calculated neutral current and the waveform shows a higher value of neutral current on HV side which is decaying over time which could be due to CT saturation. For ideal CTs, the calculated residual current based on IA-1, IB-1 and IC-1 (on Delta side of transformer) should be zero.

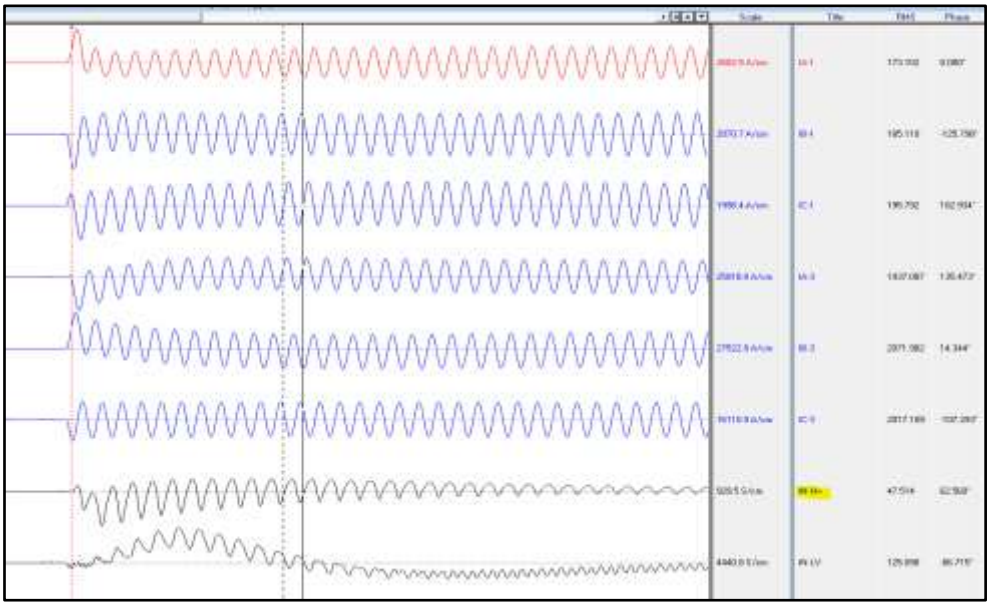

Figure 7 Current captured by relay on LV breaker closing (Transformer loading)

Fig 8 shows the transformer HV and LV current after magnitude and vector compensation. The relay uses these current to calculate the differential and bias currents. Comparing the HV A phase current with the LV A phase current and the HV B phase current with the LV B phase current indicates there is CT saturation on transformer loading. It could be due to a very high X/R ratio. Figure 8a shows the operation of the differential element in A and B phase where the transient bias in disabled. Figure 8b shows that the relay remains stable when the transient bias in enabled.

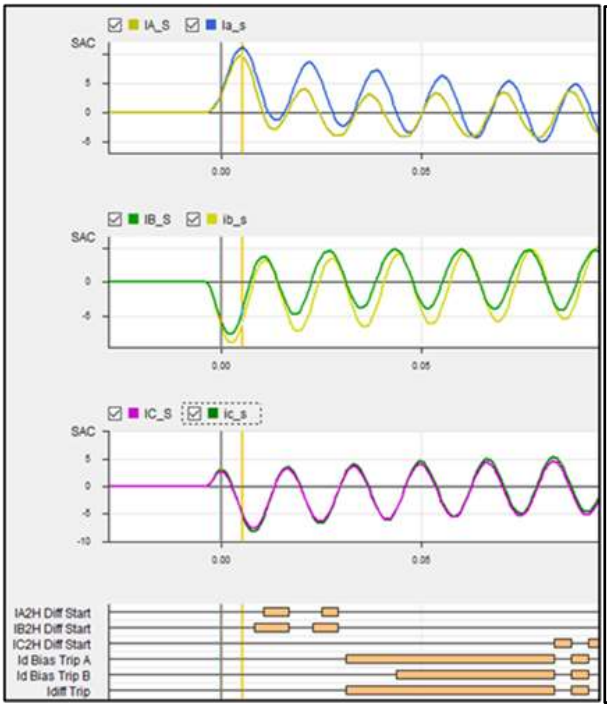

Fig 8a (Transient bias disabled)

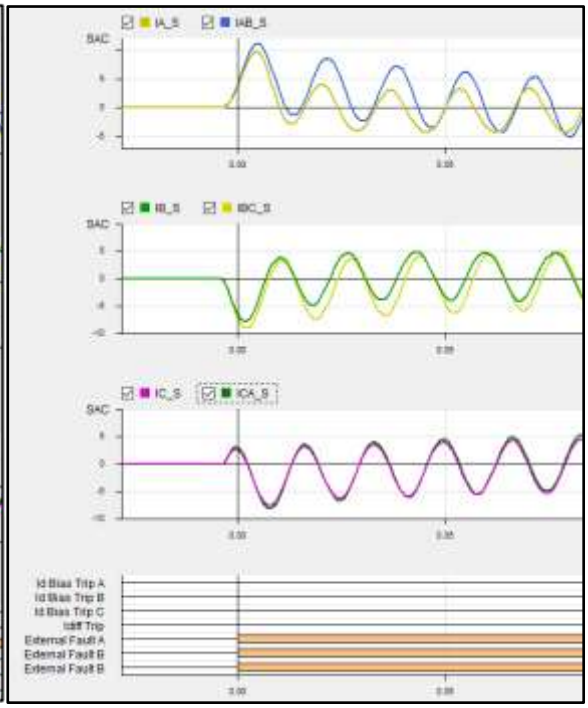

Fig 8b (Transient bias enabled)

Figure 8 Transformer HV and LV current after magnitude and vector compensation

4. Unblocking of the differential element for faster tripping

There are various methods used to stabilize the transformer differential element during inrush conditions. The focus of these methods is mainly on blocking or restraining the differential element during inrush conditions. However, during internal faults CT saturation can produce harmonics in the differential current which can slow down the biased differential element. It is equally important to unblock the differential element for faster operation during actual internal fault conditions. Unblocking has become even more critical due to reduction in the threshold of the 2nd harmonic for some of newly designed transformers. Figure 9 shows the differential trip logic and unblocking using no gap/CT saturation detection. As seen in the diagram unblocking is only active during internal fault scenarios.

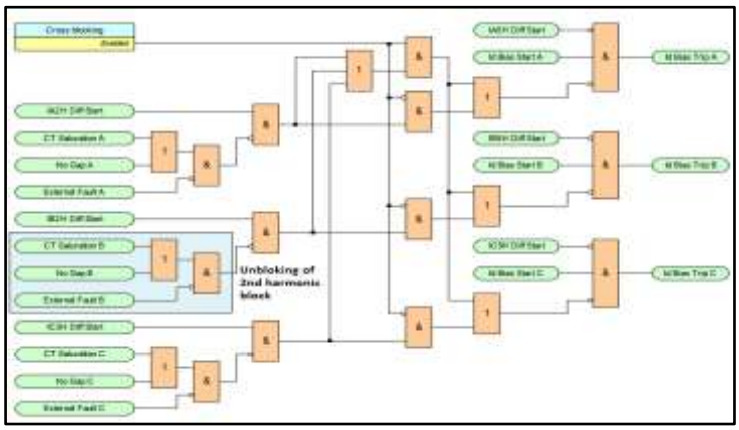

Figure 9 Transformer HV and LV current after magnitude and vector compensation

The no gap detection technique counts the numbers of consecutive samples below a dynamic threshold to determine the low current gap duration in the waveform. The gap is determined on a per phase basis of the differential current and if the gap is less than the defined duration, it considers this as a fault waveform and not an inrush condition. The no gap detection also complements the CT saturation condition during internal faults. Figure 10 shows an example of a 2nd harmonic current generated by a high offset transformer internal fault current. The harmonic bar shows the 2nd harmonic content of 16 % in A phase and 15.8 % in C. As the relay is set for 2nd harmonic blocking threshold of 10% with cross blocking functionality, without no gap detection it could have resulted in tripping only once the 2nd harmonic goes below the set value. The digital channels show activation of the no gap detection algorithm, indicating this is an internal fault, before dropping of the 2nd harmonic block signal, reducing the operating time for this fault.

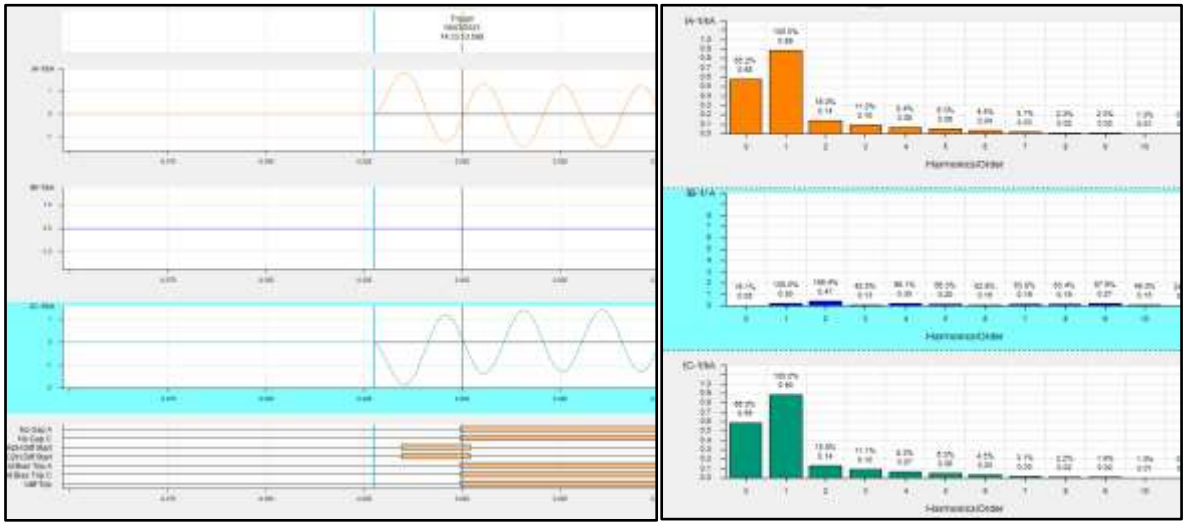

Figure 10 No Gap detection to reduce the operating time in the presence of 2nd harmonic above threshold

Figure 11 shows a fault in one phase during transformer energisation. The record shows a 2nd harmonic of 24.6 % and 11.2 % in B and C phase respectively. As the relay detects a No gap condition in A phase, it unblocks the differential and releases the trip for faster tripping of the biased differential element.

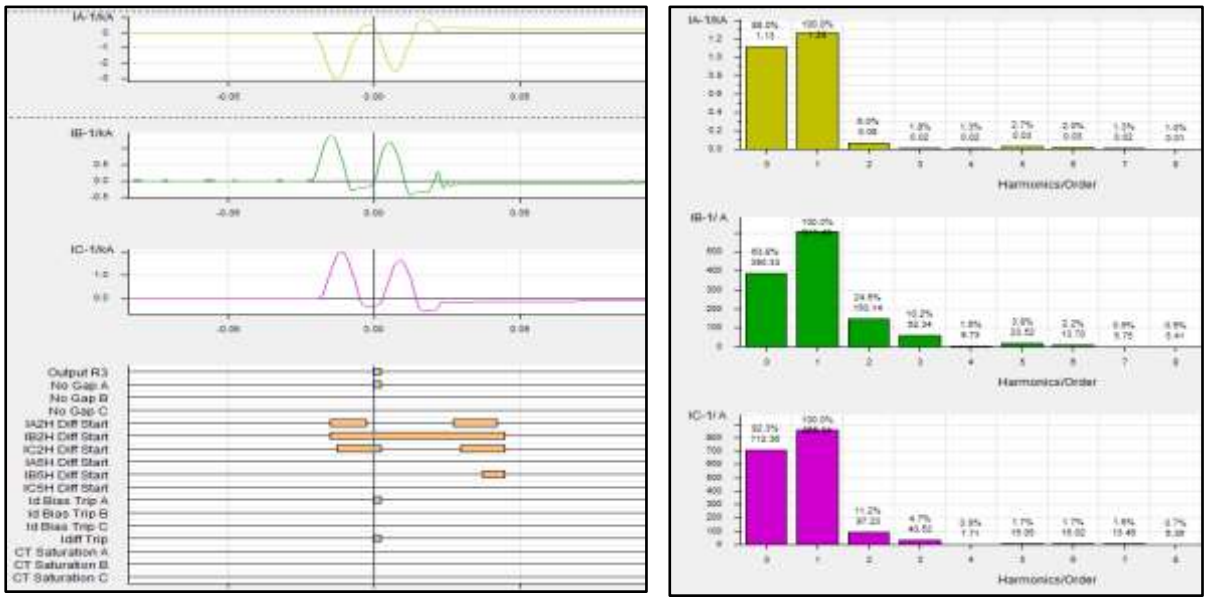

Figure 11 No Gap detection during fault on one phase on transformer energisation

The CT saturation detection technique is a complementary technique to the no gap technique to distinguish between magnetising inrush and CT saturation; to maintain relay stability during inrush conditions. To detect a CT saturation condition the differential current samples on a per phase basis are considered. The relay analyses the differential current waveforms considering their derivatives dynamically with fixed thresholds determined from RTDS (real time digital simulator) tests.

When a CT saturates, the second harmonic content may be above the second harmonic threshold used for blocking the biased differential protection. As a result, the biased differential element may be blocked during an internal fault. If the fault level is not high enough for the unrestrained differential element to operate this can result in slow tripping.

Figure 12a is a record of RTDS testing for a phase A-N internal fault and the relay operated in 57 ms when CT saturation and No gap detection is disabled. Figure 12b is the same fault scenario with CT saturation and No gap detection enabled and the operating time is 28 ms.

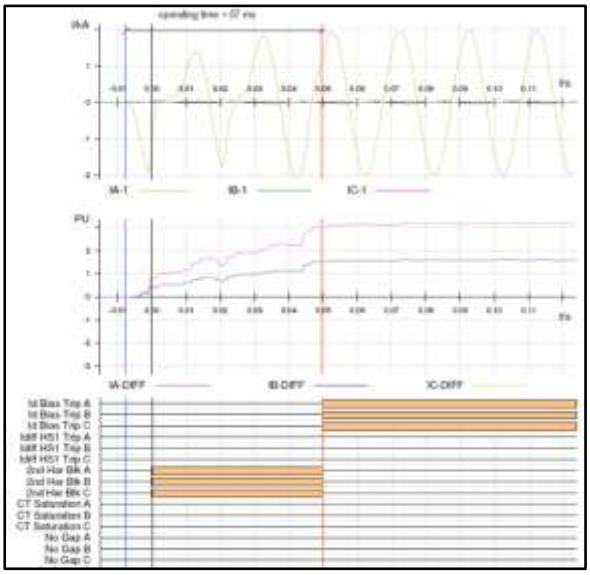

Figure 12a

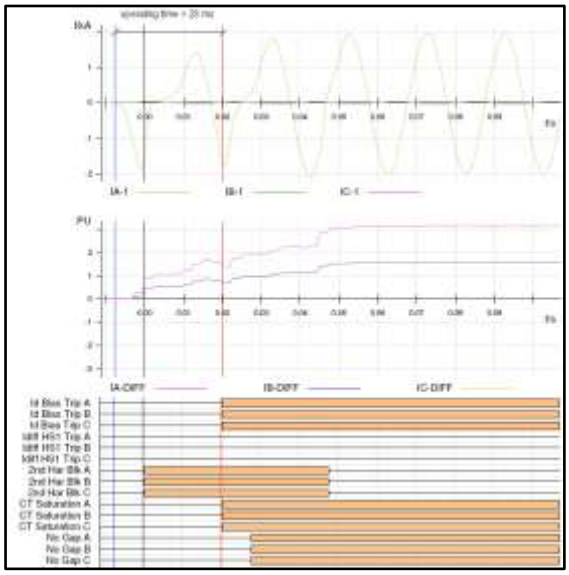

Figure 12b

Figure 12 CT saturation during an internal fault condition

5. Conclusion

From various field records and RTDS testing, it is evident that the adaptive transient bias algorithm improves the stability of the biased differential element during external fault scenarios. It is also evident that the CT saturation and no gap waveform recognition techniques reduce the operating time of the biased differential element during internal faults when there is CT saturation which produces 2nd harmonic above the set harmonic blocking values.

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