Cost and Time Efficient Methodologies for Evaluation of the CT Saturation Impact on Bus Differential Protection Using Real-Time Digital Simulator Testing

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I. INTRODUCTION

The conventional current transformers (CT) with iron core are still the most widely used components for protective relays measurements. Due to the non-linear magnetizing characteristics of the iron core, CTs are prone to saturation under heavy fault and transient conditions. Saturation levels depend on the fault current magnitude, CT burden, primary time constant of a DC offset current, level of CT core remanence, and dimensioning factor of the CT. When CT saturates, the primary currents cannot be reproduced correctly, leading to the misoperation of protection devices connected to the CT. These incidents are on the rise due to increased fault levels of the expanding power system. The saturation free time of the CT, which is the time elapsed for the CT to saturate from fault inception, plays a major role in the correct operation of protection relays. Utilities try to maximize this saturation-free time by specifying strict CT requirements when needed. However, with improved saturation detection algorithms in modern relays that require shorter saturation-free times, such requirements can be relaxed. These developments can enhance cost efficiencies through reduced CT dimensioning and less costly secondary circuit design.

Testing a wide variety of cases in a simulation platform similar to actual system conditions is the key for utilities to optimize the CT requirements. Real-time digital simulation (RTDS) testing provides the greatest tool to verify CT design requirements. Using the RTDS with the hardware in loop (HIL) testing replicates the actual system conditions to simulate protective devices' performance. This method offers several advantages compared to the conventional processes and tools utilized by most utilities to evaluate the relay behavior under CT saturation circumstances. Such processes and tools are developed based on simplified models and assumptions, which do not represent the true behavior of the system under the test. HIL testing using RTDS would allow engineers to understand the relay features thoroughly. However, the cost and time required to prepare the test plan and test setup to execute the simulations could hinder the engineers from moving forward with this testing approach.

We present methodologies that would help reduce the cost of RTDS testing of bus differential protection elements in the presence of CT saturation. We discuss how a 1-Amp relay input can be used instead of a 5-Amp input for testing to reduce the number of amplifiers required for testing. In addition, it is shown how to vary the CT saturation free time by changing the relay burden instead of requiring relatively high magnitude secondary test currents that exceed regular test set current limits. Automated test scripts have been used to run several test cases to reduce the test execution times and thoroughly test the relay behavior. Various test cases have been simulated, and the efficacy of the adopted methods is demonstrated.

II. PROBLEM DESCRIPTION

The focus of the procedure is to test the bus differential relay response to fault currents with the effect of CT saturation. The CT saturation free time is a test parameter varied to determine what saturation free time is required for the bus protection to operate reliably and securely.
Saturation in the CT occurs when the secondary fault current causes a flux in the core that exceeds the maximum flux for what the CT is dimensioned and designed. The CT's maximum flux is mainly a function of the size, the iron core's diameter, the iron material, and the number of turns.
Manufacturers and standards usually do not specify flux directly. Nevertheless, a "saturation voltage" is defined in IEEE C37.110- "The saturation voltage (Vx): The symmetrical voltage across the secondary winding of the CT for which the peak induction just exceeds the saturation flux density."

The integral of the voltage across the CT core is proportional to the flux. The voltage integral is used to calculate the saturation free time for the specified test cases. The following formula can, in approximation, describe a fault current of an LR circuit:

$$i_{(t)} = \sqrt{2} I_f (e^{-\frac{t}{T_P}} \cdot cos(\theta) - cos(\omega t + \theta)) \qquad [1.1]$$

With

I_f= Short circuit current

T_P= DC time constant calculated by L fault loop over R fault loop

$\alpha = \arctan(\frac{\omega L}{R})$

φ = angle of fault incidence on the voltage wave

$\Theta = \varphi - \alpha$

In the conducted tests, cases with a maximum DC offset and without DC offset were used.

A. Calculation of CT Saturation Free Time for Fault Currents with Maximum DC Offset

Maximum DC offset occurs when the switching angle on the voltage is selected, so that Θ is zero. It is typically close to the zero crossings of the voltage but with a difference of the angle α. In this case, the formula [1.1] can be written as:

$$i_{(t)} = \sqrt{2} I_f (e^{-\frac{t}{T_P}} - cos(\omega t)) \qquad [1.2]$$

By multiplying the current with the CT burden, we can calculate the saturation-free time through integrating the voltage of the secondary side of the CT and comparing it with the saturation voltage Vx of the CT:

$$V_x = I(R_{CT} + R_b)\left\{[-\omega T_p]\left(e^{-\frac{t_{sat}}{T_P}} - 1\right) - sin(\omega t_{sat})\right\} \qquad [1.3]$$

Figure 1 shows how the adjustment of the relay burden Rb was used to change the CT saturation free time for a specified test scenario. The y-axis shows the ratio between the saturation voltage Vx of the CT (given by the datasheet of the CT) and the product of secondary fault current and the total CT burden. This ratio, also specified in some standards as the over-dimension factor, is typically used by protection engineers to verify whether a given CT is dimensioned correctly.

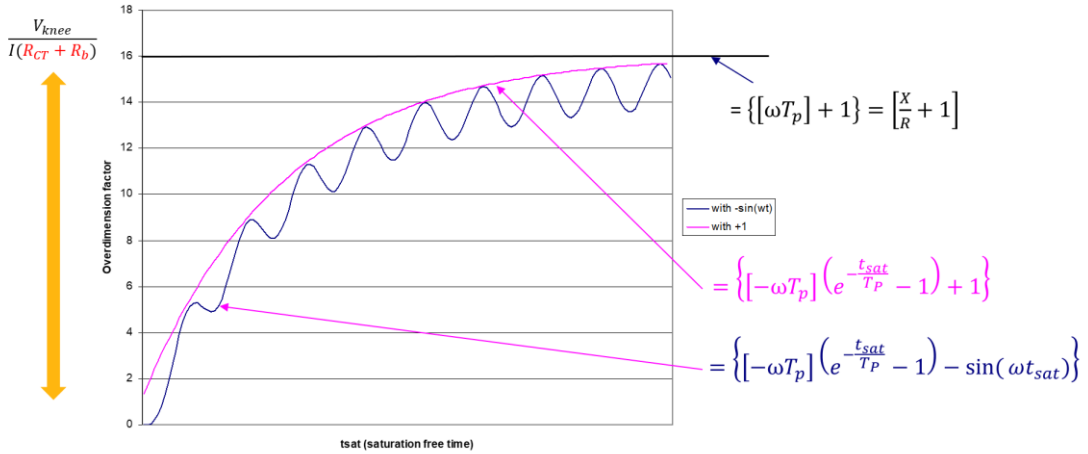

Figure 1. Calculation of CT Saturation Free Time

In Figure 1, the blue curve represents the over-dimension factor requirement to avoid CT saturation for a given time, based on the flux development in the CT core for a fault current with the maximum DC offset. For saturation free time requirements up to 8-10 milliseconds (ms), the blue curve and the associated formula must be used to determine the required over-dimension accurately. Once a

saturation free time > 10 ms is required, the blue curve cannot be used anymore since the core demagnetizes when the fault current has the opposite polarity. In such a case, using the blue curve could result in wrongly lower over dimensioning factors.
For saturation free times >10 ms, the red curve, which represents the maximum requirement regarding the over-dimensioning factor for a specified saturation free time, must be used. The black line represents the requirement when no saturation is allowed (t_{sat} = infinite).
For study purposes, saturation free times of <= 6ms were used. The relay burden (Rb) was calculated using the formula [1.3] (blue curve) to adjust the over-dimension factor so that the CT provides the specified saturation free time for the given fault current.

Figure 2 shows an example of secondary fault currents resulting from different CT burdens with the effect of maximum DC-offset.

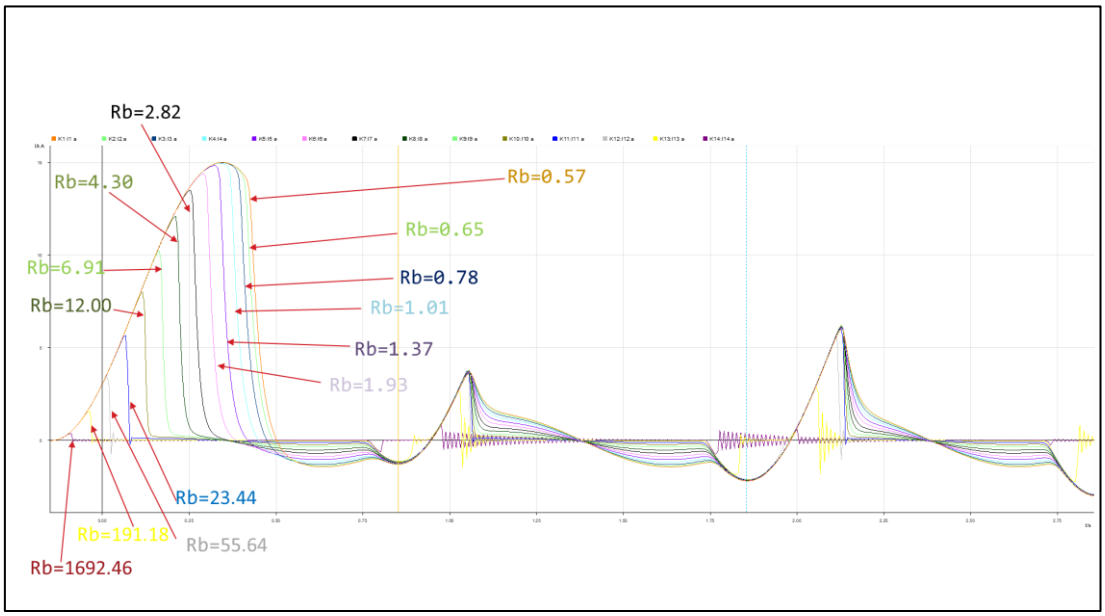

Figure 2. Curves with Different Saturation Free Time Based on Selected Burdens – with Maximum DC Offset

B. Calculation of CT Saturation Free Time for Fault Currents without DC Offset

The fault current will not show any DC offset if the fault is applied at a switching angle Θ=90 degrees. This fault current is typically close to the maximum voltage value but with a difference of the angle α. In such a case, formula [1.1] can be simplified as:

$$i_{(t)} = \sqrt{2} I_f \, sin(\omega t) \qquad [1.4]$$

By multiplying the current with the CT burden, we can calculate the saturation free time through integrating the voltage of the secondary side of the CT and comparing it with the saturation voltage Vx of the CT:

$$V_x = I_f (R_{CT} + R_b)\{1 - cos(\omega t_{sat})\} \qquad [1.5]$$

The variation of CT saturation free time can be achieved with the change of different test parameters.

- Fault current magnitude
- CT burden
- Time constant Tp = $\frac{L}{R}$
- Fault injection angle
- Remanence flux in the core
- Turn ratio

The CT burden, fault injection angle, and remanence flux were used to vary the saturation free time in the conducted tests. The fault current, CT burden, and turn ratio were produced by a software application and the test substation configuration. Figure 3 shows an example of secondary fault currents resulting from different CT burdens without the effect of DC-offset.

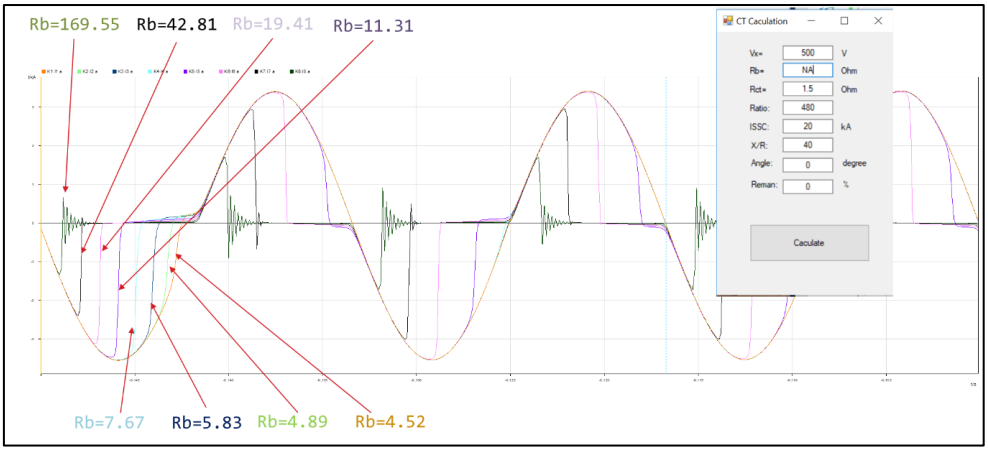

Figure 3. Curves with Different Saturation Free Time Based on Selected Burdens – without DC Offset

The burden used for the described test was calculated by the above formulas. Then, each test point was repeated five times to confirm a consistent tripping time or observe any deviations for the same test condition. In the summary results table, the columns Case1-Case5 report the tripping time on each test. Figure 4 shows the system modeled and used for RTDS testing of the bus differential relay.

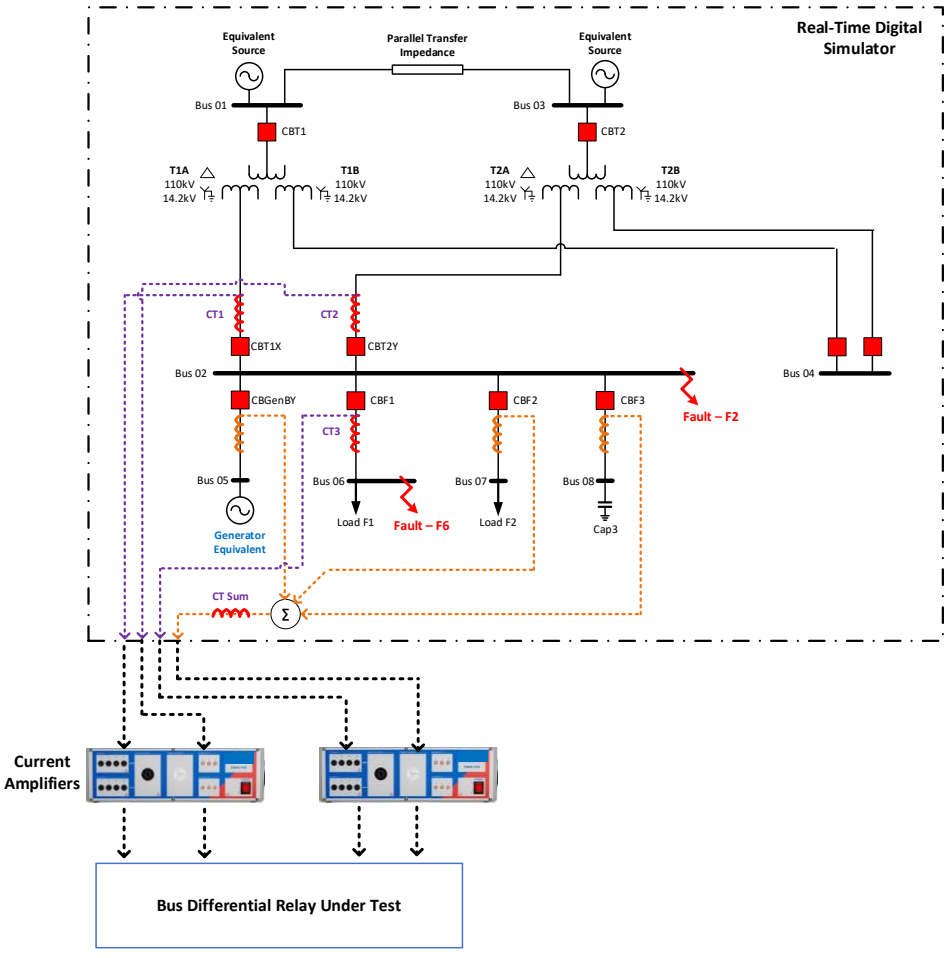

Figure 4. Test setup for bus differential relay testing.

The relay under test uses three different algorithms that are active under different conditions for different objectives as follows:

- The first algorithm is high-speed, which can issue a trip command based on two samples of current signal.

- The second algorithm comes into action when the first algorithm does not issue a trip signal and already has additional built-in security measures.
- The third algorithm uses Fourier Filter values and has additional stabilization means implemented. In practice, this algorithm could operate on complex faults with low fault currents.

III. TEST RESULTS

A. Test Results of Comparison between 1A and 5A Nominal Current Setting

It was proposed to conduct the test with a 1A nominal current input of the protection relay. This approach allows the use of a smaller number of amplifiers that would provide a maximum of 32A, thereby saving the total testing cost. It was essential to show that the 1A and 5A responses of the bus protection relay (the relay under test) were identical in response to internal and external single phase to ground faults under CT saturation.

In RTDS, the CTs were simulated with their selected CT ratios (2400/5 for transformer and 1200/5 for load feeder) and desired CT saturation behavior. Simulation and testing were done separately for the two nominal current values of the relay. When the simulated currents were applied to the relay via the amplifier, a dividing factor of 1 or 5 was used based on the relay's selected nominal current. By doing so, the relay algorithm theoretically sees the same current values internally.

The tests were conducted with two different fault current levels to challenge the relay characteristic at various points:

- Fault current level 1: 3.84 kA
- Fault current level 2: 8.85 kA

The fault current was changed by using a different transformer grounding reactance value in the RTDS simulation. Both the internal and external bus faults were simulated with only transformer T1 in service (see Figure 4).

The test results for 1A and 5A current inputs of the relay are collected and presented below.

In the below tables that include test results,

- *The burden is in ohm, the angle is in degrees, and t sat shows the saturation free time in (ms).*
- *The location of the fault can be identified in Figure 4.*
- *Cases 1-5 at the right-hand side of the table include the operation time of the relay for the same test that has been repeated five times.*
- *Full DC offset refers to the maximum DC offset value that is considered for simulation.*

1) Test Results for Internal Faults with Fault Current of 3.84 kA

a) Test Results with the Nominal Current Setting of 1A

Table 1. Internal Faults Tested with a 1A Nominal Current

Case	Burden	FaultType	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
In_1	887.2437	A-G	F2	90	1	No DC offset	16.2	No Op	No Op	No Op	No Op
In_2	399.3504	B-G	F2	210	1.5		16.8	8.4	8.2	8.4	8
In_3	228.6887	C-G	F2	330	2		8.6	8.4	9	8.6	8.8
In_4	149.8107	A-G	F2	90	2.5		8.6	8.8	8.4	8.8	8.2
In_5	107.0892	B-G	F2	210	3		7.8	8.4	8.8	8.6	8.2
In_6	81.46693	C-G	F2	330	3.5		8.6	8.8	8.4	9	8.4
In_7	64.98704	A-G	F2	90	4		8	8	8.8	8.4	8.6
In_8	53.85248	B-G	F2	210	4.5		8.2	8.4	8	8.4	8.8
In_9	46.06824	C-G	F2	330	5		8.8	8.4	8.6	8.8	9
In_10	40.50822	A-G	F2	90	5.5		8	8.6	8.6	8.2	8.8
In_11	36.50185	B-G	F2	210	6		8.8	8.8	9	9	9
In_34	8386.292	A-G	F2	0	1	Full DC Offset	No Op	No Op	No Op	No Op	No Op
In_35	2358.007	B-G	F2	120	1.5		No Op	No Op	No Op	No Op	No Op
In_36	977.7647	C-G	F2	240	2		No Op	No Op	No Op	No Op	No Op
In_37	499.5376	A-G	F2	0	2.5		No Op	No Op	No Op	No Op	No Op
In_38	290.9985	B-G	F2	120	3		125	60.6	60.8	122.8	9.4
In_39	185.5927	C-G	F2	240	3.5		9	9.8	9.6	10	9.4
In_40	126.5224	A-G	F2	0	4		9.2	9.2	9	9.2	9.8
In_41	90.79309	B-G	F2	120	4.5		9.6	9.8	8.8	9.6	9.2
In_42	67.87479	C-G	F2	240	5		9.4	9.6	9	9.4	9.4
In_43	52.47435	A-G	F2	0	5.5		9.6	9.2	9.6	9.4	8.8
In_44	41.72926	B-G	F2	120	6		9.8	9.4	9.2	9.2	9.4

b) Test Results with the Nominal Current Setting of 5A

Table 2. Internal Faults Tested with 5A Nominal Current

Case	Burden	FaultType	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
In_1	887.2437	A-G	F2	90	1	No DC offset	No Op	No Op	15.6	No Op	No Op
In_2	399.3504	B-G	F2	210	1.5		No Op	No Op	7.8	8	7.6
In_3	228.6887	C-G	F2	330	2		8	7.8	7.6	8	7.6
In_4	149.8107	A-G	F2	90	2.5		8.4	8.4	7.8	8.2	7.6
In_5	107.0892	B-G	F2	210	3		8.6	8.4	8.6	8.2	8.2
In_6	81.46693	C-G	F2	330	3.5		8.6	8.2	7.6	8.4	8.6
In_7	64.98704	A-G	F2	90	4		8.2	8.6	7.8	8	7.4
In_8	53.85248	B-G	F2	210	4.5		8	8.6	8.2	8.2	8.4
In_9	46.06824	C-G	F2	330	5		8.4	8.4	7.8	8.2	7.6
In_10	40.50822	A-G	F2	90	5.5		8	8	8	8.4	8
In_11	36.50185	B-G	F2	210	6		8.2	8	8	8.4	7.8
In_34	8386.292	A-G	F2	0	1	Full DC Offset	No Op	No Op	No Op	No Op	No Op
In_35	2358.007	B-G	F2	120	1.5		No Op	No Op	No Op	No Op	No Op
In_36	977.7647	C-G	F2	240	2		No Op	No Op	No Op	No Op	No Op
In_37	499.5376	A-G	F2	0	2.5		No Op	60.2	No Op	No Op	No Op
In_38	290.9985	B-G	F2	120	3		8.6	123.2	8.6	9	8.4
In_39	185.5927	C-G	F2	240	3.5		8.6	9.2	8.4	8.4	9.2
In_40	126.5224	A-G	F2	0	4		8.8	9.2	9.4	9	9.2
In_41	90.79309	B-G	F2	120	4.5		9.4	8.6	8.8	8.6	9
In_42	67.87479	C-G	F2	240	5		8.8	8.4	9.2	9.4	8.6
In_43	52.47435	A-G	F2	0	5.5		8.4	8.8	8.8	8.2	8.4
In_44	41.72926	B-G	F2	120	6		8.6	8.6	9.2	8.8	8.6

2) Test Results for External Faults with Fault Current of 3.84 kA

a) Test Results with the Nominal Current Setting of 1A

Table 3. External Faults Tested with 1A Nominal Current

Case	Burden	Fault Type	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
Ex_1	221.7664	A-G	F6	90	1	No DC offset	8.6	20	36.6	19.8	19.8
Ex_2	57.17397	B-G	F6	210	2		No Op	No Op	No Op	No Op	No Op
Ex_3	37.46002	C-G	F6	330	2.5		No Op	No Op	No Op	No Op	No Op
Ex_4	26.78265	A-G	F6	90	3		No Op	No Op	No Op	No Op	No Op
Ex_5	20.37889	B-G	F6	210	3.5		No Op	No Op	No Op	No Op	No Op
Ex_6	16.26008	C-G	F6	330	4		No Op	No Op	No Op	No Op	No Op
Ex_7	13.47722	A-G	F6	90	4.5		No Op	No Op	No Op	No Op	No Op
Ex_8	11.53171	B-G	F6	210	5		No Op	No Op	No Op	No Op	No Op
Ex_9	10.14209	C-G	F6	330	5.5		No Op	No Op	No Op	No Op	No Op
Ex_10	9.140783	A-G	F6	90	6		No Op	No Op	No Op	No Op	No Op
Ex_11	8.424144	B-G	F6	210	6.5		No Op	No Op	No Op	No Op	No Op
Ex_34	1928.933	A-G	F6	0	1	Full DC Offset	9.2	9.8	9.4	9.4	8.8
Ex_35	220.5786	B-G	F6	120	2		9.8	9.8	148.6	148.6	10
Ex_36	112.3042	C-G	F6	240	2.5		No Op	No Op	No Op	No Op	No Op
Ex_37	65.27226	A-G	F6	0	3		No Op	No Op	No Op	No Op	No Op
Ex_38	41.56012	B-G	F6	120	3.5		No Op	No Op	No Op	No Op	No Op
Ex_39	28.29518	C-G	F6	240	4		No Op	No Op	No Op	No Op	No Op
Ex_40	20.28222	A-G	F6	0	4.5		No Op	No Op	No Op	No Op	No Op
Ex_41	15.1475	B-G	F6	120	5		No Op	No Op	No Op	No Op	No Op
Ex_42	11.69982	C-G	F6	240	5.5		No Op	No Op	No Op	No Op	No Op
Ex_43	9.295859	A-G	F6	0	6		No Op	No Op	No Op	No Op	No Op
Ex_44	7.566945	B-G	F6	120	6.5		No Op	No Op	No Op	No Op	No Op

b) Test Results with the Nominal Current Setting of 5A

Table 4. External Faults Tested with 5A Nominal Current

Case	Burden	FaultType	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
Ex_1	221.7664	A-G	F6	90	1	No DC offset	19.2	19.6	36	8	7.8
Ex_2	57.17397	B-G	F6	210	2		No Op	No Op	No Op	No Op	No Op
Ex_3	37.46002	C-G	F6	330	2.5		No Op	No Op	No Op	No Op	No Op
Ex_4	26.78265	A-G	F6	90	3		No Op	No Op	No Op	No Op	No Op
Ex_5	20.37889	B-G	F6	210	3.5		No Op	No Op	No Op	No Op	No Op
Ex_6	16.26008	C-G	F6	330	4		No Op	No Op	No Op	No Op	No Op
Ex_7	13.47722	A-G	F6	90	4.5		No Op	No Op	No Op	No Op	No Op
Ex_8	11.53171	B-G	F6	210	5		No Op	No Op	No Op	No Op	No Op
Ex_9	10.14209	C-G	F6	330	5.5		No Op	No Op	No Op	No Op	No Op
Ex_10	9.140783	A-G	F6	90	6		No Op	No Op	No Op	No Op	No Op
Ex_11	8.424144	B-G	F6	210	6.5		No Op	No Op	No Op	No Op	No Op
Ex_34	1928.933	A-G	F6	0	1	Full DC Offset	8.6	8.6	8.4	8.4	8.8
Ex_35	220.5786	B-G	F6	120	2		No Op	9.4	9.6	9.4	9.4
Ex_36	112.3042	C-G	F6	240	2.5		No Op	No Op	No Op	No Op	No Op
Ex_37	65.27226	A-G	F6	0	3		No Op	No Op	No Op	No Op	No Op
Ex_38	41.56012	B-G	F6	120	3.5		No Op	No Op	No Op	No Op	No Op
Ex_39	28.29518	C-G	F6	240	4		No Op	No Op	No Op	No Op	No Op
Ex_40	20.28222	A-G	F6	0	4.5		No Op	No Op	No Op	No Op	No Op
Ex_41	15.1475	B-G	F6	120	5		No Op	No Op	No Op	No Op	No Op
Ex_42	11.69982	C-G	F6	240	5.5		No Op	No Op	No Op	No Op	No Op
Ex_43	9.295859	A-G	F6	0	6		No Op	No Op	No Op	No Op	No Op
Ex_44	7.566945	B-G	F6	120	6.5		No Op	No Op	No Op	No Op	No Op

3) Test Results for Internal Faults with Fault Current of 8.85 kA

a) Test Results with the Nominal Current Setting of 1A

Table 5. Internal Faults Tested with 1A Nominal Current

Case	Burden	FaultType	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
In_1	384.9633	A-G	F2	90	1	No DC offset	7.8	7.6	16	7	15.6
In_2	172.7757	B-G	F2	210	1.5		7.6	8	7.6	7.2	8
In_3	98.55388	C-G	F2	330	2		7.6	8.2	7.4	7.2	8
In_4	64.2494	A-G	F2	90	2.5		8.4	7.6	7.2	7.2	7.6
In_5	45.66957	B-G	F2	210	3		8.2	8	7.4	7.4	7.8
In_6	34.52629	C-G	F2	330	3.5		7.4	8.4	7.4	7.8	7.4
In_7	27.35909	A-G	F2	90	4		8.4	7.8	7.4	7	8.2
In_8	22.51661	B-G	F2	210	4.5		8.2	7.6	7.8	7.4	7
In_9	19.1312	C-G	F2	330	5		8	8.4	7.2	7.8	7.6
In_10	16.71311	A-G	F2	90	5.5		8.4	8.2	7.4	7.2	7.2
In_34	3646.343	A-G	F2	0	1	Full DC Offset	No Op	No Op	No Op	No Op	No Op
In_35	1024.607	B-G	F2	120	1.5		No Op	70.8	No Op	No Op	No Op
In_36	424.3314	C-G	F2	240	2		8.6	No Op	7.8	103.4	54.4
In_37	216.3477	A-G	F2	0	2.5		8.6	8.6	8.4	8.2	7.8
In_38	125.6528	B-G	F2	120	3		9	8.6	8.6	7.6	8
In_39	79.81121	C-G	F2	240	3.5		8.8	8.6	8.2	8.4	8.2
In_40	54.12118	A-G	F2	0	4		8.4	8.6	8.4	7.4	7.4
In_41	38.5823	B-G	F2	120	4.5		8	8.8	8.6	8.4	8.4
In_42	28.61499	C-G	F2	240	5		8.6	8.8	8.4	7.8	8.4
In_43	21.91725	A-G	F2	0	5.5		8.4	8	7.8	8.4	8.4
In_44	17.24415	B-G	F2	120	6		8	8.8	7.8	8.6	8.4

b) Test Results with the Nominal Current Setting of 5A

Table 6. Internal Faults Tested with 5A Nominal Current

Case	Burden	FaultType	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
In_1	384.9633	A-G	F2	90	1	No DC offset	7	7.4	7.2	16	16.4
In_2	172.7757	B-G	F2	210	1.5		7.2	7.2	7.4	8	7.2
In_3	98.55388	C-G	F2	330	2		7.4	7.6	7	7.4	7.6
In_4	64.2494	A-G	F2	90	2.5		7.8	7	7.8	7.4	7.6
In_5	45.66957	B-G	F2	210	3		7.2	7.8	7.6	7	7.2
In_6	34.52629	C-G	F2	330	3.5		7.2	7.8	7.2	7.6	8
In_7	27.35909	A-G	F2	90	4		7.2	7.6	7	7.6	7.6
In_8	22.51661	B-G	F2	210	4.5		7.6	7.2	7.4	7.6	7.4
In_9	19.1312	C-G	F2	330	5		7.8	7.8	7	8	7.2
In_10	16.71311	A-G	F2	90	5.5		7.4	7.2	7.8	7	7.4
In_34	3646.343	A-G	F2	0	1	Full DC Offset	No Op	No Op	No Op	No Op	No Op
In_35	1024.607	B-G	F2	120	1.5		No Op	70.2	22	No Op	No Op
In_36	424.3314	C-G	F2	240	2		7.8	54.4	38.4	7.6	8
In_37	216.3477	A-G	F2	0	2.5		8.4	7.8	8.4	8.4	8
In_38	125.6528	B-G	F2	120	3		8.4	7.8	8.6	8.2	7.8
In_39	79.81121	C-G	F2	240	3.5		8.6	8.2	8.6	7.6	8
In_40	54.12118	A-G	F2	0	4		8.4	7.6	7.6	7.6	7.6
In_41	38.5823	B-G	F2	120	4.5		8.4	7.8	7.8	7.6	8
In_42	28.61499	C-G	F2	240	5		7.8	8	8	8.4	8.6
In_43	21.91725	A-G	F2	0	5.5		8	7.6	8	8.8	7.8
In_44	17.24415	B-G	F2	120	6		8.2	8.4	7.8	7.8	8.6

4) Test Results for External Faults with Fault Current of 8.85 kA

a) Test Results with the Nominal Current Setting of 1A

Table 7. External Faults Tested with 1A Nominal Current

Case	Burden	FaultType	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
Ex_1	96.25883	A-G	F6	90	1	No DC offset	No Op	8.2	8.2	19.8	20
Ex_2	43.21192	B-G	F6	210	1.5		20.4	37.6	20.6	37.4	9
Ex_3	24.65647	C-G	F6	330	2		No Op	No Op	No Op	No Op	No Op
Ex_4	16.08035	A-G	F6	90	2.5		No Op	No Op	No Op	No Op	No Op
Ex_5	11.43539	B-G	F6	210	3		No Op	No Op	No Op	No Op	No Op
Ex_6	8.649573	C-G	F6	330	3.5		No Op	No Op	No Op	No Op	No Op
Ex_7	6.857774	A-G	F6	90	4		No Op	No Op	No Op	No Op	No Op
Ex_8	5.647153	B-G	F6	210	4.5		No Op	No Op	No Op	No Op	No Op
Ex_9	4.800799	C-G	F6	330	5		No Op	No Op	No Op	No Op	No Op
Ex_10	4.196277	A-G	F6	90	5.5		No Op	No Op	No Op	No Op	No Op
Ex_11	3.76068	B-G	F6	210	6		No Op	No Op	No Op	No Op	No Op
Ex_34	851.4998	A-G	F6	0	1	Full DC Offset	8.4	8.4	8.8	8.6	8.8
Ex_35	234.7597	B-G	F6	120	1.5		9	8.6	9.2	8.6	8.6
Ex_36	96.39252	C-G	F6	240	2		8.8	8.8	9.2	9.6	No Op
Ex_37	48.90284	A-G	F6	0	2.5		157.8	158	168.2	No Op	141.2
Ex_38	28.30758	B-G	F6	120	3		No Op	No Op	No Op	No Op	No Op
Ex_39	17.93492	C-G	F6	240	3.5		No Op	No Op	No Op	No Op	No Op
Ex_40	12.13653	A-G	F6	0	5		No Op	No Op	No Op	No Op	No Op
Ex_41	8.635778	B-G	F6	120	4.5		No Op	No Op	No Op	No Op	No Op
Ex_42	6.393408	C-G	F6	240	5		No Op	No Op	No Op	No Op	No Op
Ex_43	4.88827	A-G	F6	0	5.5		No Op	No Op	No Op	No Op	No Op
Ex_44	3.839054	B-G	F6	120	6		No Op	No Op	No Op	No Op	No Op

b) Test Results with the Nominal Current Setting of 5A

Table 8. External Faults Tested with 5A Nominal Current

Case	Burden	FaultType	Location	angle	t sat		Case 1	Case 2	Case 3	Case 4	Case 5
Ex_1	96.25883	A-G	F6	90	1	No DC offset	19.4	8.4	8	19.6	8.2
Ex_2	43.21192	B-G	F6	210	1.5		37.4	20.4	37.6	37	20
Ex_3	24.65647	C-G	F6	330	2		No Op	No Op	No Op	No Op	No Op
Ex_4	16.08035	A-G	F6	90	2.5		No Op	No Op	No Op	No Op	No Op
Ex_5	11.43539	B-G	F6	210	3		No Op	No Op	No Op	No Op	No Op
Ex_6	8.649573	C-G	F6	330	3.5		No Op	No Op	No Op	No Op	No Op
Ex_7	6.857774	A-G	F6	90	4		No Op	No Op	No Op	No Op	No Op
Ex_8	5.647153	B-G	F6	210	4.5		No Op	No Op	No Op	No Op	No Op
Ex_9	4.800799	C-G	F6	330	5		No Op	No Op	No Op	No Op	No Op
Ex_10	4.196277	A-G	F6	90	5.5		No Op	No Op	No Op	No Op	No Op
Ex_11	3.76068	B-G	F6	210	6		No Op	No Op	No Op	No Op	No Op
Ex_34	851.4998	A-G	F6	0	1	Full DC Offset	8.4	8	8.2	7.8	8.2
Ex_35	234.7597	B-G	F6	120	1.5		7.8	7.8	8.2	8.2	8.4
Ex_36	96.39252	C-G	F6	240	2		157	8.2	98.2	8.6	98.4
Ex_37	48.90284	A-G	F6	0	2.5		169	157.2	157.2	168	No Op
Ex_38	28.30758	B-G	F6	120	3		No Op	No Op	No Op	No Op	No Op
Ex_39	17.93492	C-G	F6	240	3.5		No Op	No Op	No Op	No Op	No Op
Ex_40	12.13653	A-G	F6	0	5		No Op	No Op	No Op	No Op	No Op
Ex_41	8.635778	B-G	F6	120	4.5		No Op	No Op	No Op	No Op	No Op
Ex_42	6.393408	C-G	F6	240	5		No Op	No Op	No Op	No Op	No Op
Ex_43	4.88827	A-G	F6	0	5.5		No Op	No Op	No Op	No Op	No Op
Ex_44	3.839054	B-G	F6	120	6		No Op	No Op	No Op	No Op	No Op

5) Conclusion of Test Results for Comparison between 1A and 5A Settings

The test results in Table 1 - Table 8 show that the relay responds to different test cases independent of the relay's selected value for the nominal fault current. The results indicate statistical differences for faults on the same location and the selected nominal current. Faults were repeated five times to reveal the relay behavior under different alignments of the fault initiation and the internal relay sampling rate. Each case could activate a different processing path in the relay algorithm. While the relay shows different operation times under 1A and 5A settings, such differences are deemed acceptable and should not cause concerns.

Similar statistical differences were observed by comparing the test results between the 1A and 5A nominal current test cases. It can be concluded that the relay algorithm operated similarly under both the 1A and 5A settings. The test with a nominal current of 1A provides valid results that can be used to evaluate the relay characteristic also for the 5A nominal current version. Further tests were conducted with a nominal relay current of 1A and presented and discussed hereunder.

B. Internal Faults with and without Remanence

This test's focus was to show the impact of different levels of saturation of CT1 (see Figure 4) on the relay operation for internal faults to the bus. The system only included the infeed via transformer T1; this is considered the most plausible scenario where the fault current on CT1 will have the highest value. Based on the simulated system in Figure 4, for faults where both the transformers T1 and T2 would provide fault currents, the fault current through CT1 would be smaller than only having transformer T1 feeding the fault current. The test results are given in tables below, where If shows the fault current in kA, and fault location is shown in Figure 4.

1) Test Results for Internal Faults without DC Offset

Table 9. Results for Internal Faults with and without Remanence without DC Offset

								Negative Remanence=-60%					No Remanence					Positive Remanence = 60%				
Case	Burden [Ohm]	Fault Type	Location	angle	t sat [ms]	If [kA]		Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5
In_1	889.73	A-G	F2	90	1	3.85	single phase to ground faults	No Op	No Op	8.4	8.2	No Op	No Op	No Op	No Op	No Op	16.4	No Op	No Op	No Op	15.8	No Op
In_2	400.47	B-G	F2	210	1.5	3.85		No Op	No Op	No Op	No Op	No Op	8.2	8.4	No Op	8.4	8	7.6	16.4	7.8	16.4	16.6
In_3	229.33	C-G	F2	330	2	3.85		No Op	No Op	No Op	No Op	7.8	8.4	9	8.4	8.6	8.8	8.2	7.6	8	8.4	7.6
In_4	150.23	A-G	F2	90	2.5	3.85		8	8.4	7.6	7.6	8.2	8.2	9	8.8	8.8	8.2	8.2	8.2	8.2	8	8
In_5	107.39	B-G	F2	210	3	3.85		8.2	8.2	7.8	7.6	7.6	8.8	8.4	8.8	8.4	8	7.8	7.4	8.2	8.4	7.6
In_6	81.699	C-G	F2	330	3.5	3.85		7.6	7.6	7.8	8	8.4	8.2	8.6	8.4	8.4	8.8	7.6	7.8	8.2	7.8	7.8
In_7	65.173	A-G	F2	90	4	3.85		7.8	8.4	8.4	7.8	8	9	8	8.6	8.8	8.4	7.8	8.2	8.2	8.4	8.4
In_8	54.007	B-G	F2	210	4.5	3.85		7.6	7.8	7.8	8	8.4	8.2	8.2	8.2	8.4	8.4	7.8	8.2	8	8.6	8.8
In_9	46.201	C-G	F2	330	5	3.85		8	8.2	8	8.2	8.2	8.6	8.2	9	8	8.4	7.8	8.2	8.4	7.8	8.2
In_10	40.626	A-G	F2	90	5.5	3.85		8.2	7.6	8	7.6	7.4	8.2	8.8	9	8.6	8	8.4	8	8.2	8	8.2
In_11	36.608	B-G	F2	210	6	3.85		8.6	7.8	8.4	7.8	8.2	8.4	8.4	8.4	8.8	8.4	8.4	8.4	8.4	7.4	8.4
In_12	425.82	AB	F2	60	1	8.09	Phase to phase faults	7.2	15.2	15.4	7	7.4	7.6	7.6	8.2	14.6	8	7.6	8.4	7	8	7.4
In_13	191.21	BC	F2	180	1.5	8.09		7.8	8.2	7.8	8.6	7.6	7.2	7.4	8.4	7.2	7.6	8	7.2	8	7.2	8.2
In_14	109.14	CA	F2	300	2	8.09		8.4	7.8	8	7.4	8.2	7.8	7.6	8	8	7.6	7.2	8	8.2	7.2	8
In_15	71.209	AB	F2	60	2.5	8.09		7.4	7.8	7.4	7.6	7.2	7	8	7.4	7.4	8.4	7.2	8.6	7.6	7.4	8
In_16	50.666	BC	F2	180	3	8.09		7.6	7.8	7.4	8.2	7.6	7.4	7.6	7.2	8.4	7.8	7.6	8	8	7.6	7.4
In_17	38.345	CA	F2	300	3.5	8.09		7.8	7	8.2	7	7.6	8	7.4	7.6	8	7.8	7.4	7.8	7.8	8.2	7.8
In_18	30.42	AB	F2	60	4	8.09		7.8	7.8	7.2	8	7.8	8	7.4	8.2	8.2	7	7.4	7.4	7.8	7.8	8
In_19	25.066	BC	F2	180	4.5	8.09		7.6	8.4	8.2	7.2	8.6	7.8	7.6	8	8.6	8	8	7.4	7.8	8.4	7.8
In_20	21.322	CA	F2	300	5	8.09		8.4	7.2	8	7.2	8	7.6	7.4	8.2	7.6	8	7.8	7.6	8.6	7.6	7.8
In_21	18.649	AB	F2	60	5.5	8.09		7.6	7.6	7.8	7.6	7.8	8	8.2	7.4	7.6	7.4	7.8	8	8.4	7.4	8.2
In_22	16.722	BC	F2	180	6	8.09		8.2	7.8	8	7.8	8.6	8	7.2	8.2	7.2	7	7.2	7.8	8	7.4	7.6
In_23	368.56	ABC	F2	90	1	9.34	3 phase faults	8.4	8	7.4	8.2	7.2	8.2	7.8	7.4	7.2	7.8	7.8	7.8	7.4	8.4	11.4
In_24	165.37	ABC	F2	90	1.5	9.34		8.2	7.6	8.2	8.4	7	7.4	8.4	7.4	8.2	7.6	8.2	7.6	8.2	7.4	8.2
In_25	94.303	ABC	F2	90	2	9.34		8.2	7.8	8	8.4	8.2	7.8	7.8	8.4	8	8	8	8.4	7	7.4	8.4
In_26	61.455	ABC	F2	90	2.5	9.34		7	7.6	7	7.6	7.8	7.2	8.2	7.2	7.4	8.2	7	7.6	7.8	8	8.4
In_27	43.663	ABC	F2	90	3	9.34		8.2	7	7.8	8.4	7.8	8.2	7.6	7	7.4	7.6	7.4	8.2	7.8	8.2	7.6
In_28	32.993	ABC	F2	90	3.5	9.34		7.4	8.2	8.2	7.2	8.2	7.6	8.6	8	7.4	7	7.2	7.2	7.8	8.2	7.4
In_29	26.13	ABC	F2	90	4	9.34		7.6	7.2	7.6	7.6	8.2	7.6	8	8.2	8.2	8	7.4	7.2	7	8	7.2
In_30	21.493	ABC	F2	90	4.5	9.34		8.2	6.8	7.4	7.6	7	7.4	7.8	8.2	8.2	7.4	7.8	8.4	7.6	8	7.8
In_31	18.251	ABC	F2	90	5	9.34		7.8	7.4	8	8.2	8.4	8.4	8.2	8.4	8.4	8	8	7.6	7.2	8	7
In_32	15.936	ABC	F2	90	5.5	9.34		7.2	8	8.4	7.6	7.2	8.4	8	7.6	7.6	7.4	7.4	8.2	8.4	8	7.8
In_33	14.267	ABC	F2	90	6	9.34		8.4	7.2	7.6	7.2	7.4	7.4	7.6	7.4	7.6	8	7.8	7.8	8.6	8	8.2

2) Test Results for Internal Faults with Maximum DC Offset

Table 10. Results for Internal Faults with and without Remanence with Maximum DC Offset

								Negative Remanence=-60%					No Remanence					Positive Remanence = 60%				
Case	Burden [Ohm]	Fault Type	Location	angle	t sat [ms]	If [kA]		Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5
In_34	8297.4	A-G	F2	0	1	3.85	single phase to ground faults	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
In_35	2344.5	B-G	F2	120	1.5	3.85		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
In_36	974.36	C-G	F2	240	2	3.85		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
In_37	498.43	A-G	F2	0	2.5	3.85		No Op	No Op	No Op	9	No Op	No Op	No Op	No Op	No Op	60	No Op	60.2	No Op	No Op	No Op
In_38	290.59	B-G	F2	120	3	3.85		9	9	60.6	60.6	9	9	8.4	8.2	60.2	8.4	9	8.8	8.8	8.6	9
In_39	185.43	C-G	F2	240	3.5	3.85		9.8	9	9.8	9.6	9.6	9.2	8.4	8.8	8.8	8.4	9.4	8.8	9	8.6	8.8
In_40	126.46	A-G	F2	0	4	3.85		9.8	8.8	9	9.4	9.2	9.2	8.6	9.4	8.4	9.2	9	9	9	8.8	9
In_41	90.777	B-G	F2	120	4.5	3.85		9.6	9.8	9.2	9.2	9.6	8.4	9.6	9.4	8.4	8.8	8.8	9.2	8.8	9.4	9
In_42	67.878	C-G	F2	240	5	3.85		9.4	9.8	9.6	9	9.2	8.6	8.6	9.4	9.2	8.6	9.2	9.2	8.6	9.2	9.2
In_43	52.486	A-G	F2	0	5.5	3.85		9.8	9.4	9	9.8	8.8	9.4	8.2	8.4	8.6	8.8	9.2	9	8.8	8.4	9
In_44	41.744	B-G	F2	120	6	3.85		9.2	9.8	9.8	9.6	9.4	8.6	8.4	8.6	8.4	9.2	8.4	8.4	8.8	9.2	8.8
In_45	5271.9	AB	F2	150	1	8.09	Phase to phase faults	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
In_46	1330.5	BC	F2	270	1.5	8.09		22.8	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	43	No Op	No Op	No Op
In_47	526.92	CA	F2	390	2	8.09		11.6	8	11.8	11.4	11.6	11.2	11	No Op	9.8	11.2	8.2	10	10	8.2	8.2
In_48	262.27	AB	F2	150	2.5	8.09		9	8.6	8	7.6	8	7.8	8.2	8.2	8.6	8.6	9	8.8	8.6	8.6	9
In_49	150.12	BC	F2	270	3	8.09		8	8.2	8.4	9.2	7.4	8.8	8	8.2	8.8	8.2	9	8.2	8.4	8.2	8.8
In_50	94.467	CA	F2	390	3.5	8.09		7.8	8.2	9.4	8	10.4	7.6	9.4	7.6	8.4	10.4	7.6	10.2	10.2	9.8	10.2
In_51	63.671	AB	F2	150	4	8.09		7.4	8.2	8.4	8.4	8.2	8	7.8	8.6	9.2	9	8	8.4	8.6	8.6	8
In_52	45.216	BC	F2	270	4.5	8.09		7.8	8.8	8	8.2	8.6	8	8.2	8.8	8	7.6	7.8	8.4	8.4	8.2	8.4
In_53	33.461	CA	F2	390	5	8.09		10.2	8	8.4	11	7.8	10.4	9.6	7.4	8.6	8.4	9.4	7.8	10.4	10.2	10.2
In_54	25.606	AB	F2	150	5.5	8.09		8.6	8.6	8.4	8	7.6	9	7.8	8.2	8.6	8.8	8.4	8.6	8.6	8.6	9
In_55	20.149	BC	F2	270	6	8.09		8.4	8.2	8.8	8.8	8.6	8.6	8.4	8.8	7.8	8.4	7.8	8.2	9	8.2	7.8
In_56	4565.4	ABC	F2	0	1	9.34	3 phase faults	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
In_57	1152.1	ABC	F2	0	1.5	9.34		22.4	7.4	18.2	13	40.4	13	7.6	12.4	12.8	21.8	13	13	22.2	No Op	13
In_58	456.11	ABC	F2	0	2	9.34		8.2	7.4	8	7.6	7.8	13	7.6	7.8	7.2	7.6	8	7.4	8.2	7.8	12.8
In_59	226.92	ABC	F2	0	2.5	9.34		7.2	8.2	7.6	7.8	7.8	8	7.4	7.8	7	7.6	7.6	7.8	7.4	8.2	7.6
In_60	129.8	ABC	F2	0	3	9.34		7.4	7.6	7.4	8.4	7.8	7.6	8.2	7	7.6	7.8	8.2	7.6	8	7.2	7.2
In_61	81.597	ABC	F2	0	3.5	9.34		7.4	7.8	7.6	8.4	8	7.6	8	7.8	7.8	7	8.2	7.6	8.2	7.6	7.2
In_62	54.926	ABC	F2	0	4	9.34		7.6	7.2	7.8	7.4	7.6	7.4	7.6	7.2	7.6	8	7.8	7.8	7.4	7.6	7.2
In_63	38.944	ABC	F2	0	4.5	9.34		7.6	7.8	7.4	8.2	8.4	7.8	7.4	7.2	7.2	8	8.4	8.2	7	8.4	8
In_64	28.764	ABC	F2	0	5	9.34		7.8	7.8	7.2	7.2	7.6	8.4	7	7.8	7.8	7.8	7	7.8	7.2	7.6	7.6
In_65	21.961	ABC	F2	0	5.5	9.34		7	7.4	7.4	8	7.6	7.6	8	7.8	7.4	8.4	8.2	7.8	7.4	8	7
In_66	17.235	ABC	F2	0	6	9.34		7.8	7	8.4	7.8	7.6	8.4	7.2	7.6	7.8	7.6	7.6	7.8	8.2	7.2	8

3) Conclusion of Internal Faults Tests

The results reported in Table 9 and Table 10 show that the relay cleared internal fault reliably for saturation-free times of >= 3ms. The relay was affected by DC-offset and needed a more prolonged saturation-free time (>=3ms) than the cases without DC-offset, requiring a saturation time of >=2.5 ms. It is worth noting that the maximum DC-offset has been considered for simulation with the definition given in Section II.

In some fault scenarios, the remanence would affect the fault clearing time and required saturation-free time if its polarity was equal to the fault current polarity (for the case study here, it would be negative remanence). Statistical differences on the fault clearing time for the five times repetition of each case are acceptable.

C. External Faults with and without Remanence

This test's focus was to show the impact of different levels of saturation of CT3 (feeder CT) on the relay security for external faults to the bus (see Figure 4). The fault was fed by both transformers T1 and T2. During this test, the cap bank and the generator on the distribution feeder were connected to the bus. The test results are given in tables below.

1) Test Results for External Faults without DC Offset

Table 11. Results for External Faults with and without Remanence and No DC Offset

								Negative Remanence=-60%					No Remanence					Positive Remanence = 60%				
Case	Burden [Ohm]	Fault Type	Location	angle	t sat [ms]	If [kA]		Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5
Ex_1	108.43	A-G	F6	90	1	7.86	single phase to ground faults	8	55	7.8	8.4	8.4	7.8	8.4	No Op	8.6	8	7.8	7.8	7.8	8.4	8.2
Ex_2	27.81	B-G	F6	210	2	7.86		37.8	38	8.6	8.6	54.8	No Op	No Op	No Op	No Op	54.8	No Op	71.4	No Op	8.6	No Op
Ex_3	18.154	C-G	F6	330	2.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_4	12.924	A-G	F6	90	3	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_5	9.7871	B-G	F6	210	3.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_6	7.7697	C-G	F6	330	4	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_7	6.4065	A-G	F6	90	4.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_8	5.4536	B-G	F6	210	5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_9	4.7729	C-G	F6	330	5.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_10	4.2825	A-G	F6	90	6	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_11	3.9314	B-G	F6	210	6.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_12	45	AB	F6	60	1	16.73	Phase to phase faults	8.8	8	8.4	8.2	7.8	8	7.8	7.8	7.6	8.4	8.2	8.2	8.2	7.4	8.8
Ex_13	11.376	BC	F6	180	2	16.73		21.2	21.6	20.4	No Op	21.4	8.2	No Op	No Op	8	8.2	No Op	No Op	20.8	No Op	No Op
Ex_14	7.3486	CA	F6	300	2.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_15	5.1673	AB	F6	60	3	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_16	3.8591	BC	F6	180	3.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_17	3.0177	CA	F6	300	4	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_18	2.4492	AB	F6	60	4.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_19	2.0518	BC	F6	180	5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_20	1.7679	CA	F6	300	5.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_21	1.5634	AB	F6	60	6	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_22	1.417	BC	F6	180	6.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_23	38.92	ABC	F6	90	1	19.34	3 phase faults	8.2	7.6	8.4	8.4	8.6	19.4	8.2	7.8	7.8	8.4	19.6	8.6	7.8	7.8	37.4
Ex_24	9.8006	ABC	F6	90	2	19.34		No Op	No Op	No Op	No Op	No Op	No Op	8.2	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_25	6.3129	ABC	F6	90	2.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_26	4.4239	ABC	F6	90	3	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_27	3.2909	ABC	F6	90	3.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_28	2.5622	ABC	F6	90	4	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_29	2.0699	ABC	F6	90	4.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_30	1.7257	ABC	F6	90	5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_31	1.4799	ABC	F6	90	5.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_32	1.3027	ABC	F6	90	6	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_33	1.1759	ABC	F6	90	6.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op

2) Test Results for External Faults with Maximum DC Offset

Table 12. Results for External Faults with and without Remanence and Maximum DC Offset

								Negative Remanence=-60%					No Remanence					Positive Remanence = 60%				
Case	Burden [Ohm]	Fault Type	Location	angle	t sat [ms]	If [kA]		Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5
Ex_34	944.64	A-G	F6	0	1	7.86	single phase to ground faults	17.6	17.6	17.8	9.4	9	9.4	17.6	18	8.8	17.4	9	9.2	18.2	17.6	17.6
Ex_35	107.85	B-G	F6	120	2	7.86		9.4	17.8	9.2	9.2	9.2	9.2	17.6	9.2	9	17.6	17.6	17.6	17.6	9.6	17.6
Ex_36	54.814	C-G	F6	240	2.5	7.86		167.2	168.2	18	18	17.6	169.2	169.4	18	18	168.4	17.8	17.6	17.6	168.4	17.8
Ex_37	31.777	A-G	F6	0	3	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_38	20.162	B-G	F6	120	3.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_39	13.665	C-G	F6	240	4	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_40	9.7398	A-G	F6	0	4.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_41	7.2247	B-G	F6	120	5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_42	5.5359	C-G	F6	240	5.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_43	4.3584	A-G	F6	0	6	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_44	3.5116	B-G	F6	120	6.5	7.86		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_45	675.93	AB	F6	150	1	16.73	Phase to phase faults	No Op	8.4	8.6	8.6	8.6	8	8	8	8.2	7.8	8.2	8.2	8.6	8.4	82.2
Ex_46	59.835	BC	F6	270	2	16.73		107	8.8	107.2	106.8	9.4	9.2	8.4	8	17.8	8.8	106.8	8.4	81.8	81.6	8
Ex_47	29.196	CA	F6	390	2.5	16.73		143.2	110	10.6	10.8	10.6	92.8	126.6	109.8	143	11	93.2	83.4	66.2	11.2	10.8
Ex_48	16.458	AB	F6	150	3	16.73		141.8	125	125	125.8	142.6	9.8	141.8	9.4	142.6	184.2	166.4	182.8	209	225.6	126
Ex_49	10.212	BC	F6	270	3.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	10.2	No Op	No Op	No Op	No Op	No Op	No Op
Ex_50	6.7831	CA	F6	390	4	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_51	4.7401	AB	F6	150	4.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_52	3.4446	BC	F6	270	5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_53	2.5817	CA	F6	390	5.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_54	1.9839	AB	F6	150	6	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_55	1.5563	BC	F6	270	6.5	16.73		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_56	585.32	ABC	F6	0	1	19.34	3 phase faults	8	7.8	7.6	7.2	8.4	18.2	8.2	7	7.8	8.4	7.8	7	17.2	8.4	8.4
Ex_57	51.767	ABC	F6	0	2	19.34		18	7.8	8.6	17.6	7.8	7.8	7.8	9	7.2	7.2	7.6	7.4	8.6	18.2	8
Ex_58	25.233	ABC	F6	0	2.5	19.34		18.2	18.2	8.4	8	17.4	94.2	94.2	94.2	8	8.4	18	8.4	8.2	17.8	18.2
Ex_59	14.202	ABC	F6	0	3	19.34		88.8	8.2	114.4	111.4	89	8.6	8.6	95	8.8	9	111.6	128	128	166.8	No Op
Ex_60	8.7925	ABC	F6	0	3.5	19.34		No Op	No Op	No Op	No Op	No Op	8.8	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_61	5.8231	ABC	F6	0	4	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_62	4.0539	ABC	F6	0	4.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_63	2.9319	ABC	F6	0	5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_64	2.1846	ABC	F6	0	5.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_65	1.6669	ABC	F6	0	6	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op
Ex_66	1.2966	ABC	F6	0	6.5	19.34		No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op	No Op

3) Conclusion of External Faults Tests

The results in Table 11 and Table 12 show that the relay is stable for all external faults with saturation free times >= 4 ms. The relay was affected by DC-offset and needed a more prolonged saturation free time (>= 4 ms) as compared to the cases without DC-offset (>= 2.5 ms). It is worth noting that the maximum DC-offset has been considered for simulation with the definition given in Section II.
In some fault scenarios, the remanence would affect the fault clearing time and the required saturation-free time if its polarity was equal to the fault current polarity (for the case study here, it would be negative remanence).
The fault clearing times in the five repeated cases for three-phase faults with the maximum DC-offset and a saturation free time of 3ms with negative remanence are found to be in a range from 8.2ms to 114.4ms.

D. Evolving Faults

This test focused on showing the relay's ability to detect and reliably clear faults evolving from external into an internal one on a different phase or onto the same phase. The test system included the infeed via transformers T1 and T2. During this test, the generator on the distribution feeder was connected to the bus (see Figure 4). The test results are given in tables below, where the evolving time shows the time in ms it takes for the fault to evolve from the 1st location to the 2nd location. The location of the fault can be identified in Figure 4.

1) Faults Evolving into a Different Phase

The results shown in Table 13 are based on a fault that starts as an external one (1st) and evolves into a second fault location on a different phase (2nd) after the specified evolving time. In this case, the first fault is present and continues while the second fault is applied to a different phase.

Table 13. Results of Faults Evolving into a Different Phase

Case	Burden [Ohm]	1st Fault Type	1st Location	angle	2nd Fault Type	2nd Location	t sat [ms]	Evolving Time [ms]	Case 1	Case 2	Case 3	Case 4	Case 5
Ev_1	6.752966	A-G	F6	90	B-G	F2	4	10	18.4	18.6	19.2	19.2	18.6
Ev_2	3.700708	B-G	F6	210	C-G	F2	6	30	37.4	37.6	36.8	37.8	37.4
Ev_3	6.752966	C-G	F6	330	A-G	F2	4	60	69.4	69.6	69.4	69	69
Ev_4	3.700708	A-G	F6	90	B-G	F2	6	100	107	108	107.8	107.4	107
Ev_5	6.752966	B-G	F6	210	C-G	F2	4	150	157.8	157	157.6	157.6	157.6
Ev_6	3.700708	C-G	F6	330	A-G	F2	6	10	19	19.4	18.8	19	19
Ev_7	6.752966	A-G	F6	90	B-G	F2	4	30	37.4	37.2	37	37	37.8
Ev_8	3.700708	B-G	F6	210	C-G	F2	6	60	69.4	68.6	68.8	68.6	68.6
Ev_9	6.752966	C-G	F6	330	A-G	F2	4	100	107.2	107.2	107.2	107.8	107.4
Ev_10	3.700708	A-G	F6	90	B-G	F2	6	150	157	157	157	157.2	157.2

2) Fault Evolving into the Same Phase

The results shown in Table 14 are based on a fault that starts as an external fault (1st) and evolves into a second fault location on the same phase (2nd) after the specified evolving time. The first fault is still present and is not removed until 5 ms or 10 ms from the inception time of the second fault is passed.

Table 14. Results of Faults Evolving into the Same Phase

									5ms overlap					15 ms overlap				
Case	Burden [Ohm]	1st Fault Type	1st Location	angle	2nd Fault Type	2nd Location	t sat [ms]	Evolving Time [ms]	Case 1	Case 2	Case 3	Case 4	Case 5	Case 1	Case 2	Case 3	Case 4	Case 5
Ev_1	6.75297	A-G	F6	90	A-G	F2	4	10	38	37.4	37	38.2	46	45.4	45.6	46.2	45.4	95
Ev_2	3.70071	B-G	F6	210	B-G	F2	6	30	71.4	70.6	71.4	70.8	71.4	70.8	70.6	71	71.2	71
Ev_3	6.75297	C-G	F6	330	C-G	F2	4	60	96	96	96.4	95.8	96.2	95.8	96.2	96.4	95.8	95.6
Ev_4	3.70071	A-G	F6	90	A-G	F2	6	100	138	138	138	138	138	137.4	138	137.2	138	138.2
Ev_5	6.75297	B-G	F6	210	B-G	F2	4	150	182.4	183	183.2	182.2	183.2	187.4	187.2	187.4	187.8	188
Ev_6	3.70071	C-G	F6	330	C-G	F2	6	10	38	37.6	46	38	46.2	45.6	46.2	45.8	45.8	46.2
Ev_7	6.75297	A-G	F6	90	A-G	F2	4	30	70.4	71.4	70.8	71.6	79.2	70.6	71.4	79.2	70.4	79.2
Ev_8	3.70071	B-G	F6	210	B-G	F2	6	60	96.2	96.4	96.4	96.4	96	96	96.2	95.4	96	95.8
Ev_9	6.75297	C-G	F6	330	C-G	F2	4	100	137.6	137.8	137.2	138.2	138	138	137.2	138	137.4	137.8
Ev_10	3.70071	A-G	F6	90	A-G	F2	6	150	184	182.4	184.2	182.6	183.8	188	187.6	187.6	187.2	188

3) Conclusion of Evolving Faults Tests

The results reported in Table 13 and Table 14 show that the relay cleared all tested evolving faults reliably and was stable during the external fault period. It is worth noting that only the saturation-free times of 4ms and 6ms were considered for this test.

The tripping times were off by +/- 8ms compared to the expected value; this was caused by the alignment of the fault injection regarding the sampling inside the relay and when the second algorithm can confirm an internal fault was present. This algorithm requires that the trip condition is fulfilled for two half cycles. Therefore, based on the fault initiation alignment, a shift of half a cycle can be expected and was observed.

IV. SUMMARY AND CONCLUSIONS

In this paper, we presented methodologies that would help reduce the cost for RTDS testing of bus differential protection elements in the presence of CT saturation. We indicated how a 1-Amp relay input can be used instead of a 5-Amp input for testing to reduce the number of amplifiers required for testing. We also demonstrated how to vary the CT saturation free time by changing the relay burden instead of requiring relatively high magnitude secondary test currents that exceed regular test set current limits. We utilized automated test scripts to run several test cases to reduce the test execution times and thoroughly test the relay behavior.

The test results indicated that the tested bus differential relay can tolerate some levels of CT saturation. The relay revealed a reliable and secure operation for all the faults with a saturation free time >= 4 ms for the internal and external tests. The relay was able to detect and clear internal faults instantaneously either through the first [<10 ms] or via the second [<20 ms] algorithm.

If an evolving fault is applied to the same phase, the relay could detect and clear the internal fault after the external fault was removed. If both the internal and external faults are present, only a portion of the fault current is seen by the relay as the internal fault current since the external fault provides a parallel path for the fault current, thereby reducing the fault current seen by the relay. With a stabilization factor of 0.65, the differential current is not high enough to overcome the stabilization current. After the external fault is removed, the relay can see the fault and clears it using the second algorithm.

REFERENCES

[1] Juergen Holbach, "Modern Solutions to Stabilize Numerical Differential Relays for Current Transformer Saturation during External Faults, *32nd Annual Western Protective Relay Conference, Washington State University Spokane*, Washington October 25-27, 2005