Webinar and Demo: Enhanced IEC 61850 Sampled Values streaming with the RTDS Simulator's GTFPGA Unit

Wednesday, September 29, 2021

Questions and Answers

Q1: Will the webinar recording and slides be made available?

Yes. The webinar recording and slides are available to all registrants. A link has been included with this document in the post-webinar email. If you would like to refer a colleague to this webinar, it can be accessed later On Demand, after having been aired, at https://www.rtds.com/events/iec-61850-gtfpga/.

Q2: Can GTFPGA-SV be implemented in a PRP or HSR topology?

Currently, PRP/HSR topologies are not supported. These topologies are currently under consideration by our development team and will likely be supported in the future.

Q3: Is the GTFPGA Unit capable of transmitting/receiving GOOSE Messages as well?

No, there is not currently an IEC 61850 GOOSE Messages firmware for the GTFPGA Unit. The RTDS Simulator can send and receive GOOSE Messages via the GTNETx2 card hardware. We recently increased our GOOSE capabilities in the GSEv7 component – please see the component manual for details on capabilities.

Q4: In the demo, is the slight offset between the publisher and subscriber sine waves due to the propagation delay of the SV protocol?

The delay contains two parts: the physical delay through the network, and the internal delay, which can be controlled via a setting in the component.

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Q5: Why is the delay setting limited to 3000 microseconds? It would be good to be able to increase the delay beyond this limit.

The delay parameter is restricted by the buffer size on the FPGA hardware, as all packets must be buffered during the delay manipulation. We are currently investigating whether we can increase the delay setting, so this may be a future development if the buffer can be increased.

Q6: What is the SimFlag parameter for? How is it used?

SimFlag is the simulation flag, which is mapped to the highest bit of the Reserved 1 segment of each SV packet, according to the IEC 61850 standard. Simulation flag is used for testing or commissioning. When the receiving IED detects that the simulation flag is high, the IED knows someone is just testing, therefore there is no need to generate a trip signal (for example) to actually open a circuit breaker.

Q7: In the new GSEv7 component, is the limit for XCBR logical node still 32 positions with Quality? Is the total limit of 512 logical nodes limited to one IED?

The XCBR node (used for switchgear circuit breaker operations in the IEC 61850 standard) still contains 32 bits – however, the overall XCBR capability is significantly increased. There is no rigid limit on the number of logic nodes (LN), but the total number of data items inside all the logical nodes (can be spread across multiple IEDs) are limited to 512 per GSEv7 component. The total data model memory limit is 4096 bytes = 512 x 4 bytes (publisher) + 512 x 4 bytes (subscriber).

If you have any further questions, please contact marketing@rtds.com.

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