EVALUATE HVDC PROTECTION AND CONTROL SCHEMES USING HIGH SPEED PROCESS BUS TECHNOLOGY

Shane X. Jin[1*], Tim J. Stott[2]

[1]RTDS Technologies Inc., Winnipeg, Canada
[2]GE Grid Integration Solutions, Stafford, UK
**shane@rtds.com*

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Abstract

The correct operation and control of an HVDC system greatly depends on the quality of voltage and current measurements. The feasibility and benefits of high-speed measurements (process bus) are analysed from three perspectives: voltage and current sensor technologies, data communication structure, and various HVDC applications. It is found that the recommended sampling frequency of 96 kHz by IEC 61896-9 is adequate for most HVDC protection and valve controls. However, for fault location applications, a higher sampling frequency beyond 200 kHz is preferred. In this paper, a high-speed process bus technique is presented. An HVDC control system testbed is developed using the high-speed process bus technique, featuring 250 kHz Sampled Value (SV) communication, which is more than double the highest sampling rate from the standard. An in-service HVDC control and protection scheme associated with an offshore to onshore wind connection, rated at 900 MW, is investigated on the testbed with a Real Time Digital Simulator (RTDS). HVDC protection and control applications are studied. The results indicate that the high sampling rate allows some protections to act faster, ensuring that expensive primary equipment can be better protected leading to a reduction in size, providing further cost and installation benefits.

1 Introduction

To meet the ever-growing demand for sustainable and uninterrupted supply of electricity, as well as the growing need to transport bulk electricity over long distances, HVDC energy highways are increasingly relied upon to efficiently deliver power to millions across the globe.

Protection and control of an HVDC system is more difficult compared to AC system due to its low impedance and no zero crossing of DC current. DC fault current typically has a high rate of rise and a large steady-state value [1]. Power electronics have limited overload capability, therefore, HVDC protection and control must act several orders magnitude faster compared to its AC counterpart. The window for fault detection and interruption is typically in the order of several milliseconds. Thus, DC faults must be detected and isolated during the transient phase of the fault, which is characterized by travelling wave behaviour [2]. High-speed and high-quality voltage and current measurements are essential for such stringent requirements.

The technology presented below represents an enhancement and modernization of HVDC protection and control equipment as well as the simulator equipment used to test it, in an effort to overcome the aforementioned challenges and provide a reliable and stable HVDC system operation.

2. DC Voltage and Current Measurements

The correct operation and control of an HVDC system greatly depends on the quality of voltage and current measurements, which may be obtained from merging units. A merging unit is a physical device that performs the time-coherent combination of multiple analogue Current Transformer (CT) and Voltage Transformer (VT) signals into a standards-compliant digital output. IEC 61850-9-2 [3] and IEC 61869-9 [4] specify that the Sampled Values (SV) protocol should be used by merging units for data communication. Merging units have gained popularity in AC digital substations. In recent years, DC merging units have emerged for HVDC substations. The SV protocol is also recommended for use in HVDC substations [5]. Unlike the AC merging units, the DC merging units must restructure their design to meet the challenging requirements for HVDC applications. Three factors constrain the DC voltage and current measurements: 1) HVDC voltage and current sensor technologies, 2) data communication structure, 3) HVDC applications such as protection, valve control, fault location, etc.

2.1 Voltage and Current Sensor Technologies

Voltage and current measurements in HVDC transmission systems must support a wide frequency range so that sufficient fault transients can be captured for the high-speed protection, control and fault location algorithms.

There are two main types of voltage sensors for HVDC grids: Resistive-Capacitive (RC) voltage dividers [6] and optical voltage sensors [7]. RC voltage dividers support accurate voltage measurement from DC to 500 kHz [6] [8]. Reference [7] proposed an optical voltage sensor based on Pockels effect. Even though this sensing technology supports a wider frequency range up to 30 MHz, some technical challenges need to be resolved [8]. As a well-established technology with good transient response and significantly smaller size, the RC voltage divider is the preferred option.

DC current measurement possesses great importance for HVDC protection and control applications. There are several current sensing technologies available for HVDC grids: simple shunt resistors, zero flux CTs, fluxgate transducers, optical current sensors, and hybrid optical sensors [9] [10] [11] [12]. The maximum supported frequencies span from several kHz to several MHz. Among them, the optical current sensor has increasingly gained interest due to its inherent isolation, great measuring capability and compact footprint.

2.2 Data Communication

The digital output of the DC merging unit is transmitted using the SV protocol. In IEC 61869-9 [4], a sampling rate of 96 kHz is selected for high bandwidth DC instrument transformers, aiming to satisfy HVDC protection, control and fault location applications. In case of a communication link failure, zero recovery time is required to ensure time-critical operations. Therefore, redundant networks are needed. IEC 61850 requires High-availability Seamless Redundancy (HSR) or Parallel Redundancy Protocol (PRP) for the SV process bus network [13]. Time-synchronized measurements are essential for merging units. IEEE 1588 Precision Time Protocol (PTP) [14] defines a network-based time synchronization technique. PTP can achieve sub-microsecond timing accuracy and is, therefore, the chosen option for DC merging units.

2.3 HVDC Applications

DC voltage and current measurements need to meet the requirements for various HVDC applications. Among them, protection, fault location and valve control are the top priorities.

Various methods have been proposed for HVDC protection. For non-unit protection, over-current, under-voltage, voltage derivative, or current derivative are often selected as fault detection criterions [2] [15]. A sampling rate between several kHz and 100 kHz is often sufficient for these algorithms. Another category of methods use current and voltage measurements sampled at higher frequencies between 500 kHz ~ 1 MHz, and applies Discrete Wavelet Transformation (DWT) analysis (or its variants) to identify the faulted pole [16] [17]. High resistance DC faults can also be detected with these methods for fault resistance up to several hundred ohms for both Pole-To-Pole (PTP) and Pole-To-Ground (PTG) faults. For unit protection, a communication link between two terminals is required. The current or voltage from both ends are sampled at around 100 kHz or lower for polarity comparison or similarity comparison [18]. DWT and its variants are often utilized to extract the desired characteristic for fault discrimination between internal and external faults [19].

Fault location possesses significant importance alongside protection in that it speeds up line restoration and reduces downtime and recovery costs, which enhances the overall system availability and reliability. Among the various fault location methods, travelling wave (TW) based algorithms gain the most attention and interest. Reference [20] proposed a TW-based algorithm using time-synchronized current measurements from both ends of the scheme. A 2 MHz sampling frequency was used, and Continuous Wavelet Transformation (CWT) was applied to determine the accurate arrival time of travelling waves. In [21], a single-ended TW-based algorithm is proposed. A fitting method based on a generalized logistic function was used to estimate the fault location. The sampling rate was set to 200 kHz. There are several other TW-based algorithms published, but most of these algorithms require a high sampling rate between 200 kHz and 2 MHz to get an accurate fault location.

In Voltage-Sourced Converter (VSC) systems, the Valve Based Electronics (VBE) controller is the bridge between the HVDC control systems and the Insulated Gate Bipolar Transistor (IGBT) valves. The VBE must send the switching commands to the valves quickly (often in less than 100 us [22]) to ensure the simultaneous capacitor voltage balance between the hundreds of valve submodules (SM). Assuming the fault judgement of valve controllers requires at least 4 sample periods, then the sampling rate should be greater than 40 kHz (sample period $\leq$ 25 us) [23].

In summary, for voltage measurements, an RC voltage divider can satisfy most HVDC applications. For current measurements, current sensors need to be selected carefully to meet the various requirements such as frequency range, accuracy, cost, footprint, etc. for the desired HVDC applications. The majority of the HVDC protection and valve controls require a sampling frequency between several kHz and 100 kHz, so the sampling frequency of 96 kHz recommended by IEC 61896-9 is adequate. However, for fault location applications, a sampling frequency between 200 kHz and 2 MHz is desired. The performance and suitability of the 96 kHz sampling rate is limited. It is likely that a higher sampling rate for HVDC instrument transformers will be adapted by the IEC 61869 standard in the future. Note that, as the sampling frequency goes higher, the requirements for the related parts are also increased, such as data processing units, network bandwidth, I/O throughput, cost, etc. A design balance needs to be achieved with careful investigation of the HVDC system.

3. High Speed HVDC Control System Testbed

To meet the requirements of HVDC applications as discussed in Section 2, a high-speed process bus technique has been developed, featuring 250 kHz SV communication. Fig. 1 illustrates the HVDC control system testbed using the high-speed process bus. The following section will describe each component in detail.

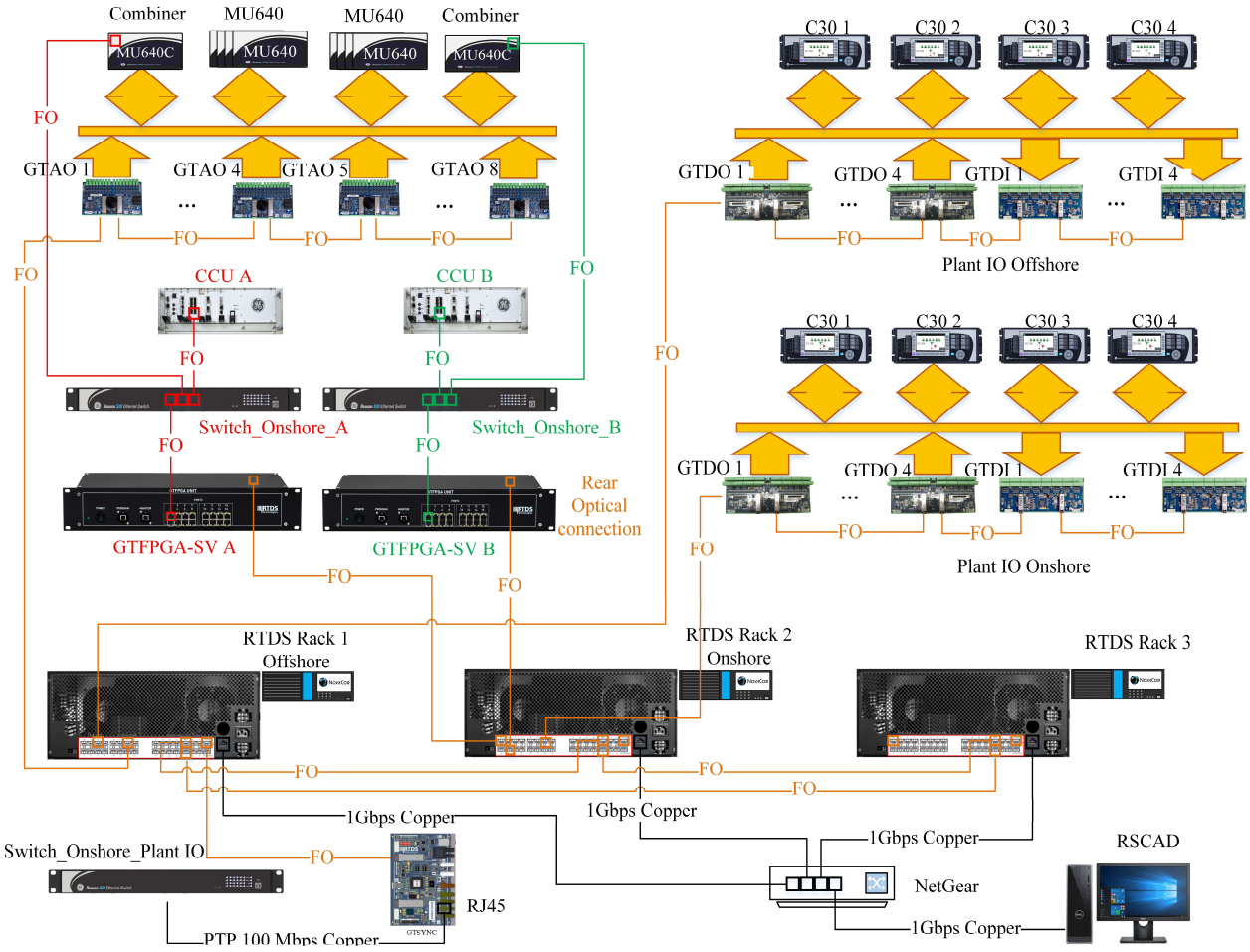

Fig. 1 Testbed for high-speed HVDC control system.

3.1 High Speed Merging Unit

In a HVDC substation, the secondary outputs of High Voltage (HV) current and voltage measurements (and other) analogue sensors are wired to Merging Units, in our case referred to as MU640s [24]. A Merging Unit is a robust, multi-channel, fast Analogue to Digital convertor that synchronously samples, converts and transmits the measured values to other systems using the IEC 61850-9-2 protocol. The messages from each set of merging units are combined into one larger IEC 61850-9-2 packet (containing up to 48 channels) before being optically transmitted to HVDC control and protection systems.

In the testbed, merging units are connected to a Real Time Digital Simulator via a set of Gigabit Transceiver Analogue Output (GTAO) interface cards. The AC and DC system under study is simulated in a RTDS simulator. The secondary voltage and currents within the simulation can be sent to the input of merging units through a group of +/- 10 volts electrical interfaces provided by GTAO cards.

In the switchyard, the MU640 Merging Units are housed within Remote Interface Cabinets (RICs) which are physically located within the HVDC substation close to concentrations of HV Sensors, as shown in Fig. 2.

All Merging units and RICs are fully duplicated to avoid single-point failures and permit maintenance of one system while the other is in full service.

Utilisation of the RICs dispersed within the converter station effectively eliminates the need for long lengths of high gauge 1 Amp or 5 Amp CT and VT cables and their associated large cable trenches and cable support trays, replacing them with a simple, easy to install optical fibre.

This approach:

- Offers considerable site installation time and material cost savings.
- Facilitates much shorter overall site installation times, as the local electrical connection between the RIC and the local sensor can be fully commissioned independently of the installation of the core HVDC control system.
- Improves the safety of the delivered system as the VT and CT terminations are now restricted to small well-defined areas of the sub-station away from the main control building.

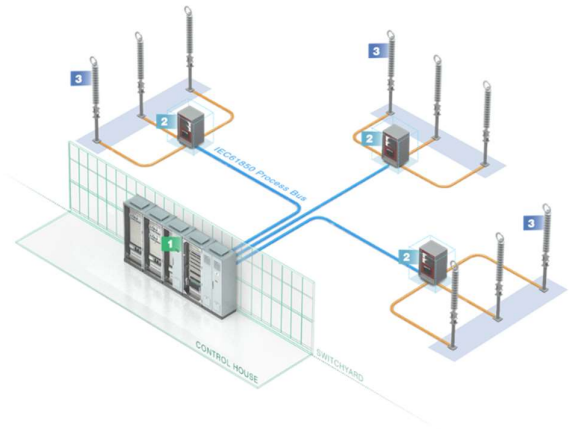

Fig. 2 Short local electrical connection of the primary sensors ③ to the RIC ② and connection of the RIC to the eLumina™ HVDC control system ① via optical fibres using the IEC 61850 protocols.

- Provides inherent measurement accuracy benefits as both the susceptibility of long cable runs to electrical noise and the multiple Analog to Digital to Analog conversion sometimes required by galvanic isolation are eliminated.
- Reduces the number of measurement signals needing to be connected to the control system as it is no longer necessary to provide duplicates of the same primary measurement with different scaling to overcome the conflicting needs of high accuracy for the normal control range and the ability for the signal to be able to represent values 20 to 30 times the normal range via the same +/- 10V input range.

3.2 Core Computing Unit

The eLumina™ Core Computing Unit (CCU) provides the high-performance, real-time computing platform needed to execute HVDC control and protection applications. It is connected to the digital inputs, outputs and analogue measurement it requires to execute its HVDC control and protection algorithms by a small number of duplicated, standard optical Ethernet connections. These optical communication connections are used to carry the IEC 61850 suite of protocols that exchange the required status, commands, and measurements between the HVDC control and protection system and the switchyard devices.

3.3 GTFPGA-SV

The GTFPGA-SV hardware unit provides IEC 61850-9-2/IEC 61869-9 SV communication for RTDS simulators [25]. The unit is capable of publishing and subscribing up to sixteen SV streams simultaneously. It supports all the sample rates defined in the standards plus a high sampling frequency of 250 kHz. For 250 kHz, each SV packet can contain up to 48 measurements. A single 250 kHz SV stream takes close to 1 Gbps network bandwidth, thus a high-throughput network is required. The GTFPGA-SV hardware unit can be used together with a GTSYNC synchronization card to synchronize the timestamps of the SV packets to an external time reference.

The GTFPGA-SV supports several types of data manipulations and stream manipulations to evaluate the impact of poor measurements on the critical HVDC protection and control algorithms. Fig. 3 shows the segments (highlighted) that can be manipulated inside an SV packet during real-time simulation. This feature can facilitate various system-level integrity tests, including:

- loss of synchronization
- sample count discontinuity
- modified SV stream identifier
- modified synchronization status
- incorrect packet length
- other data segment manipulations as desired

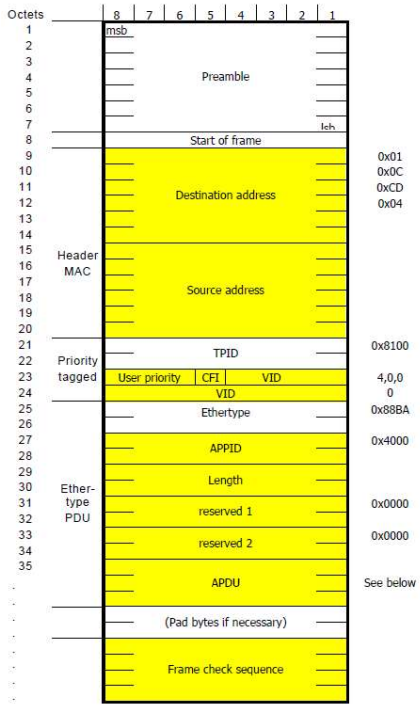

Fig. 3 Segments that can be manipulated in an SV packet.

Five types of stream manipulations are developed to test against non-ideal SV streams due to network disruptions:

- stop/resume stream publishing to simulate the loss of packets on the network
- duplicate packets to simulate a problematic redundant network topology
- swap the order of two packets to simulate non-sequential arriving of packets
- delay stream publishing to mimic unwanted latency
- add positive/negative jitter to simulate latency variance

The GTFPGA-SV is connected to the RTDS simulator through a single fibre optic cable. It can generate the same high-speed IEC 61850 compliant SV streams as the MU640 merging units, so it eliminates the need for merging units, as well as any analogue interfaces between the simulator and the merging

units. This greatly reduces the test system setup time and significantly increases the reliability of the physical test system. The measurement and digital I/O interface between the RTDS and the HVDC control system can now be connected by a small number of optical fibres rather than several hundred, less reliable and time-consuming to install, wired connections. In particular, the ability of the RTDS system to provide exactly the same combined, synchronously sampled optical IEC 61850-9-2 stream at the same rate as the MU640 units, eliminates a large number of +/-10V and/or current and voltage interfaces. This direct connection approach provides a test system that is both more representative of the final site installation as well as faster to set up and configure.

The setup of the test system is further simplified (and the setup time hence further reduced), by the ability of RTDS to configure its IEC61850 interfaces using the same type of automatically generated IEC 61850 configuration files as are downloaded the physical equipment on site. These system-wide, automatically generated configuration files provide a system-wide definition of how the data is mapped to the communicating packets, which standard features are being used, and defines their default behaviour etc.

3.4 Other devices

Digital inputs and contact outputs are connected to high-density I/O controller C30's, and further connected to the RTDS simulator through a group of Gigabit Transceiver Digital Input (GTDI) and Output (GTDO) cards.

Several high-throughput industrial switches are used to build the high-speed process bus. The switches are PTP and IEC 61850 compliant. All connections from the HVDC control system to IEDs provide redundancy using PRP as specified in IEC 62439-3.

All merging units, CCUs and IEDs are synchronized to the duplicated satellite clocks using PTP. A GTSYNC synchronization card is synchronized to the same PTP master clock. Moreover, the GTSYNC clock is used to generate the RTDS simulation time-step and provide accurate timestamps for the published 250 kHz SV packets. Thus, a system-wide synchronization is achieved.

3.5 Summary

The high sample rate provided by the MU640 and supported by the RTDS FPGA system, can be used to speed up certain functions which can then be implemented to take full advantage of the control systems architecture. The high sample rate allows some protections to act faster ensuring that expensive primary equipment can be better protected leading to a reduction in size, providing further cost and installation benefits. The ability for the MU640 measurement system to provide coherent sets of rapidly sampled, low latency, accurate measurements that are synchronously sampled across the complete HVDC link, provides a high degree of control precision and future-proofing of the control system that allows implementations of several anticipated future applications.

Within the Factory Acceptance Test (FAT) laboratory the RTDS system is used to fully prove the HVDC control system and the control and protection applications before it is shipped to site for final commissioning. The clear simplification and contract timescale reduction advantages of an IEC 61850 connected control system described would be diminished if they were not equally matched by the ability of the RTDS system to fully test them. The flexibility of the IEC 61850-9-2 interface provided by the RTDS system and its ability to inject IEC 61850 specific related faults, allows the essential negative test coverage to be provided without needing the measurement systems to have special test modes or code.

While it is still a pragmatic precaution to retain some HVDC test setups with physical MU640 systems in the measurement path to provide a facility to re-create any unexpected site-specific issues, it is envisaged that the number of signals interfaced in this way will over time reduce to zero in favour of the direct IEC 61850 interfaces to the RTDS system.

4 Case Study

An in-service HVDC control and protection application associated with an offshore to onshore wind connection, rated at 900 MW, has recently been ported to the eLumina™ fully-digital, high-speed HVDC control system. The system has been installed within GE's laboratories in Stafford and connected to the testbed shown in Fig 1.

The testbed was configured with both physical MU640 merging units, (interfaced to the RTDS system in the conventional way via GTAO card) and the GTFPGA-SV which was automatically configured to send the measurements at the same rate and in the same format as the MU640s.

Key FATs were repeated, and their results compared to the original contract's test results. An excellent correlation between the two sets of results was demonstrated. The equivalence of the two measurement signal paths was verified.

5 Conclusion

The architecture of the eLumina HVDC control system and its use of the high-speed process bus technology provide significant reliability. These advances are perfectly matched and further enhanced by the simplicity and depth of the test facilities provided by the GTFPGA-SV unit. The study indicates that the high sampling rate meets the requirements of some HVDC applications such as fault location, and allows certain protections to act faster, ensuring that expensive primary equipment can be better protected, providing further cost reduction.

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