WEBINAR AND DEMO: Power-Hardware-in-the-Loop Testing Fundamentals

RTDS Technologies

AGENDA

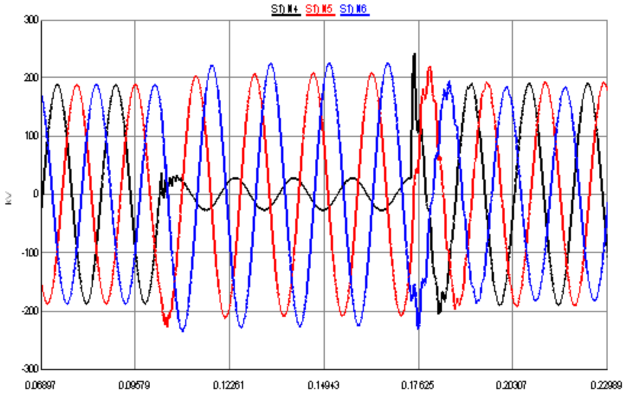
- Brief overview of real-time simulation and HIL testing
- Presentation on PHIL theory and considerations
- Demonstration
  - Hardware overview video
  - RSCAD software screenshare with video overlay
- Q&A

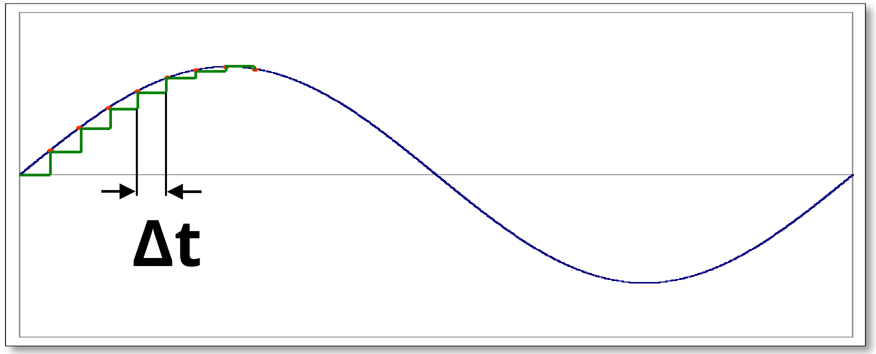
ABOUT RTDS TECHNOLOGIES

- Headquarters in Winnipeg, Canada
- Pioneered real-time power system simulation in the 1980s
- The RTDS Simulator is the industry standard for real-time simulation and closed-loop testing, used by utilities, manufacturers, research and educational institutions, and consultants worldwide
- Learn more at www.rtds.com or the large library of videos on the RTDS Technologies YouTube channel

WHAT IS EMT SIMULATION?

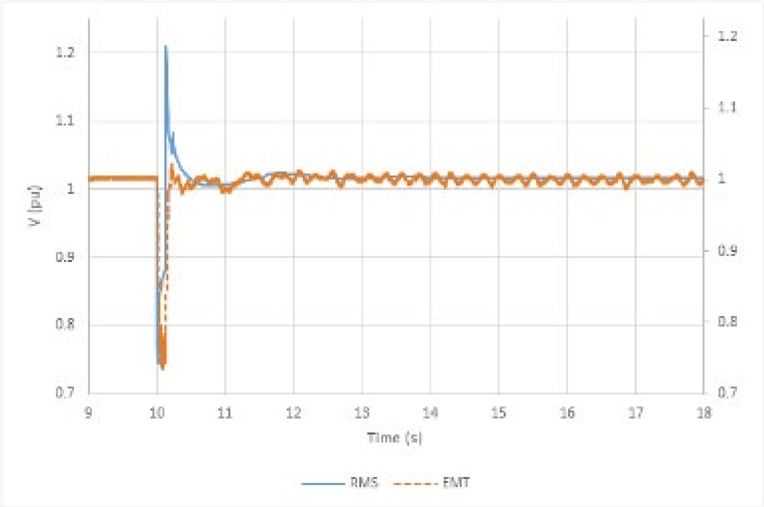
Type of Simulation	Load Flow	Transient Stability Analysis (TSA)	Electromagnetic Transient (EMT)
Typical timestep	Single solution	~ 8 ms	~ 2 - 50 µs
Output	Magnitude and angle	Magnitude and angle	Instantaneous values
Frequency range	Nominal frequency	Nominal and off-nominal frequency	0 – 3 kHz (<15 kHz)

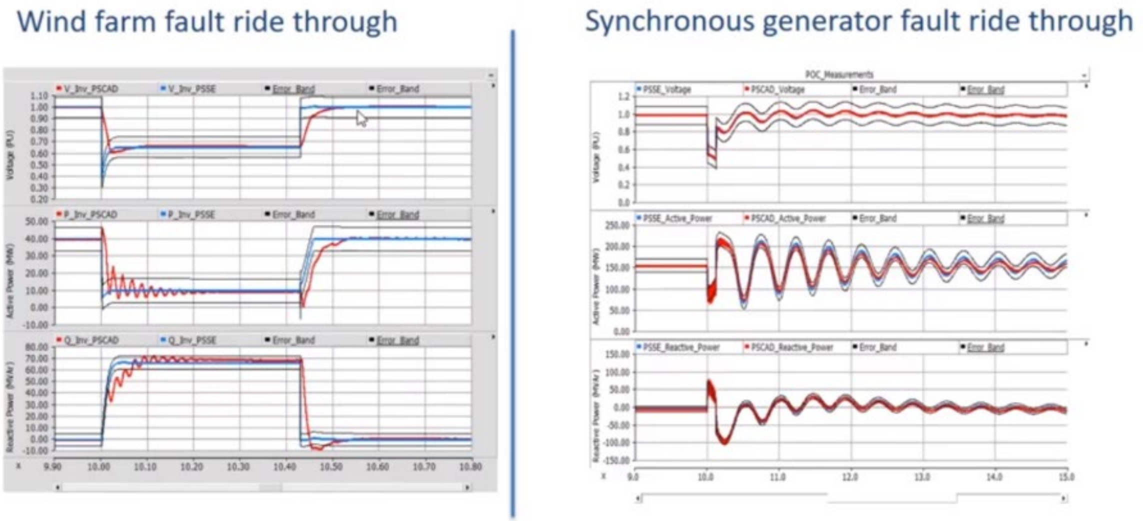




ADVANTAGES OF EMT SIMULATION

- Allows for a greater depth of analysis than phasor domain (RMS) representations
- RMS models lack the ability to capture fast network dynamics during transient conditions and may provide optimistic results
- Important for modern systems with many power electronic converters (more likely to predict control instability)





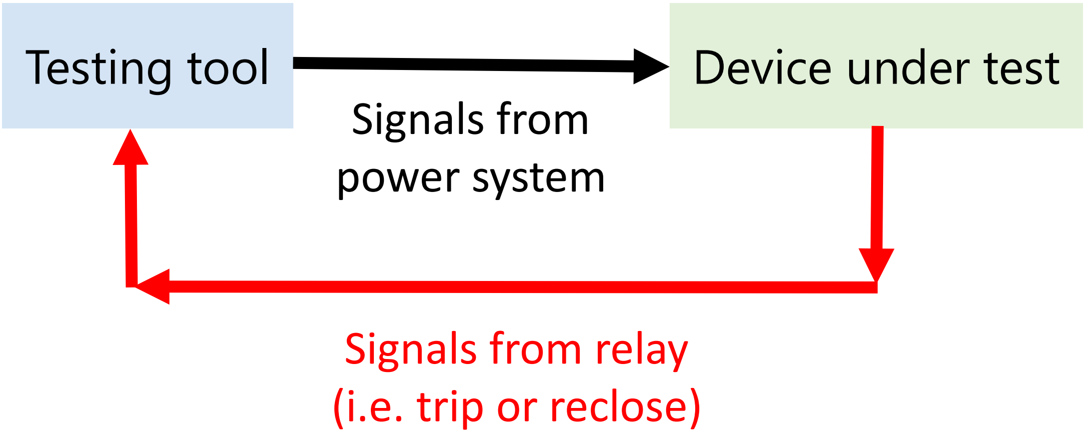
WHAT IS REAL TIME?

- **Real time it takes for an event to occur = Simulation time of an event.**
  - E.g. 3 cycle fault for 60Hz system = 0.05 seconds. RTDS simulates this fault in real time i.e. 0.05 seconds
  - Non-real-time simulations will simulate events faster or slower than real time depending on case complexity
- **Values updated each timestep**
  - All calculations and servicing I/O completed within a timestep.
  - Every timestep has same duration and is completed in real time
- **Requires dedicated parallel processing hardware**

ADVANTAGES OF CLOSED-LOOP (HIL) TESTING

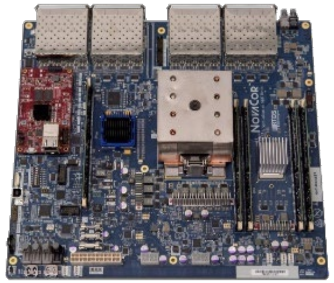
Real time operation is what allows us to connect physical devices in a **closed loop** with the simulated environment **(hardware-in-the-loop HIL)**

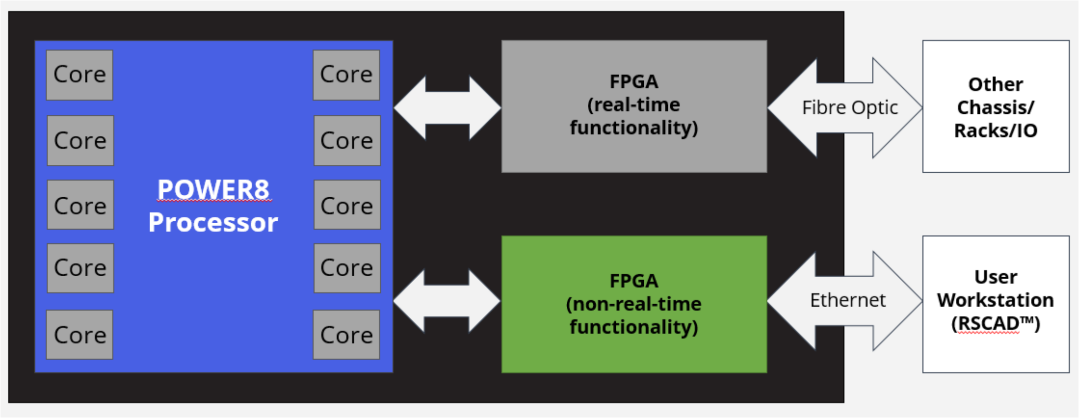
- Test continues after the action of the protection/control device, showing dynamic response of the system
- Test multiple devices (and entire schemes) at once
- Much more detailed system representation than open-loop test systems provide (e.g. modelling power electronics)



HARDWARE REQUIRED FOR REAL-TIME SIMULATION AND HIL TESTING

Parallel processing hardware

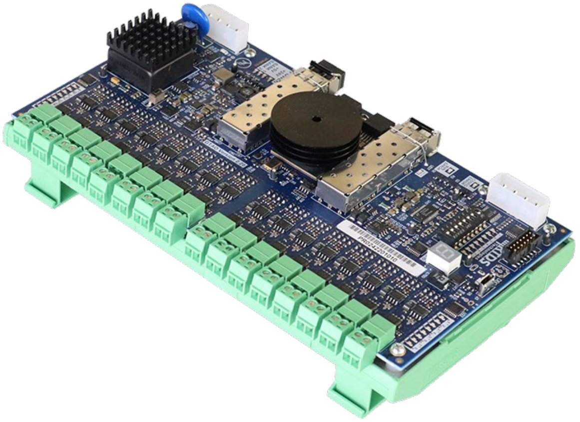




Input/output devices

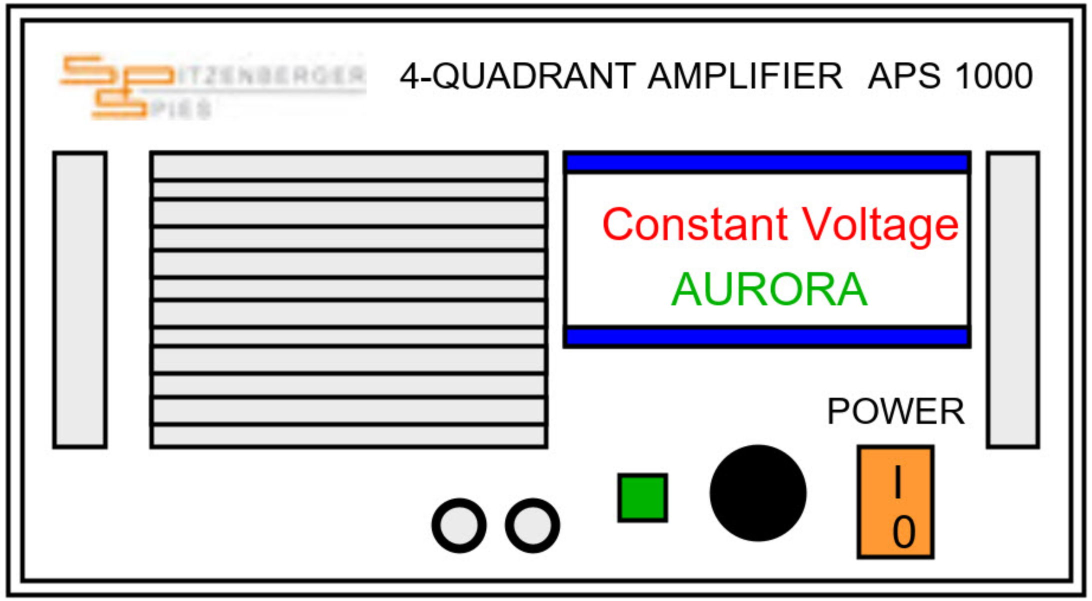
Communication protocol based

Analogue/digital



AURORA PROTOCOL

- High speed serial interface directly to external devices via optical fibre
- Direct digital link eliminates need for conventional I/O in PHIL application
- RTDS Technologies has worked with a few four-quadrant amplifier manufacturers to develop an Aurora interface



Thank you!

RTDS Technologies

RTDS.COM

Webinar and Demo: PHIL Testing Fundamentals

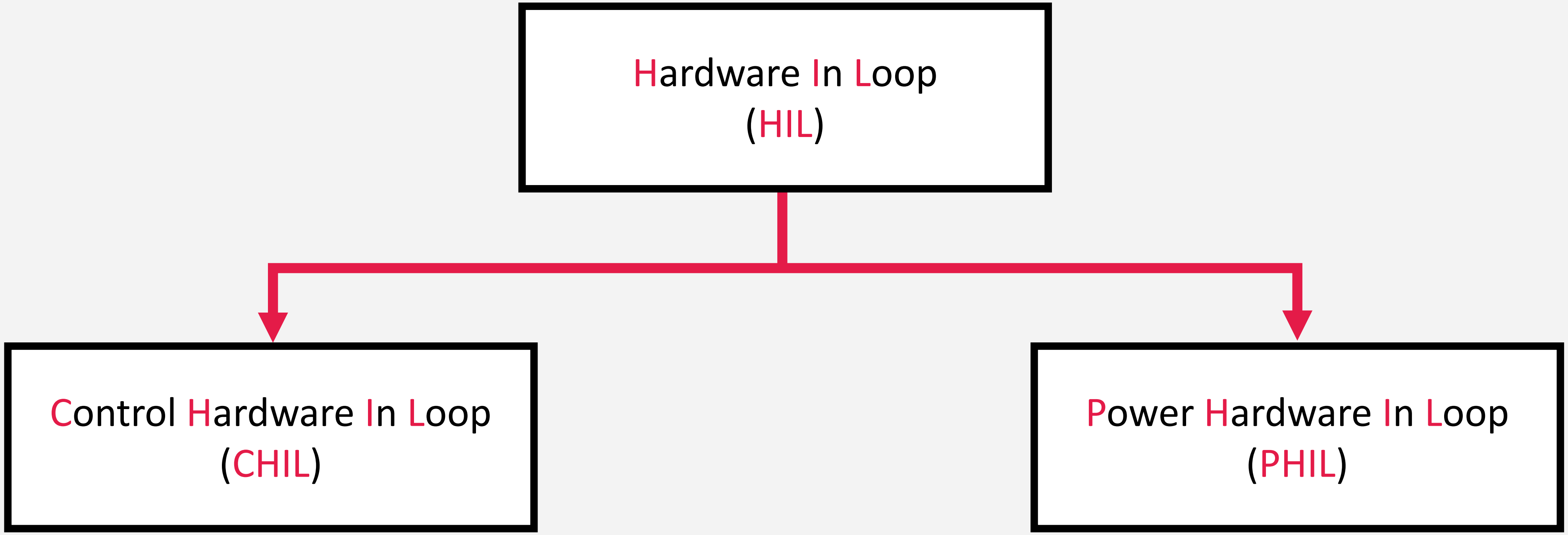
Christian Jegues

RTDS Technologies

AGENDA

- Overview of HIL (CHIL vs PHIL)
- Open Loop vs Closed Loop
- Motivation Behind PHIL
- Key Factors for PHIL Simulation
- Digital Interface
- PHIL Components
- Demonstration

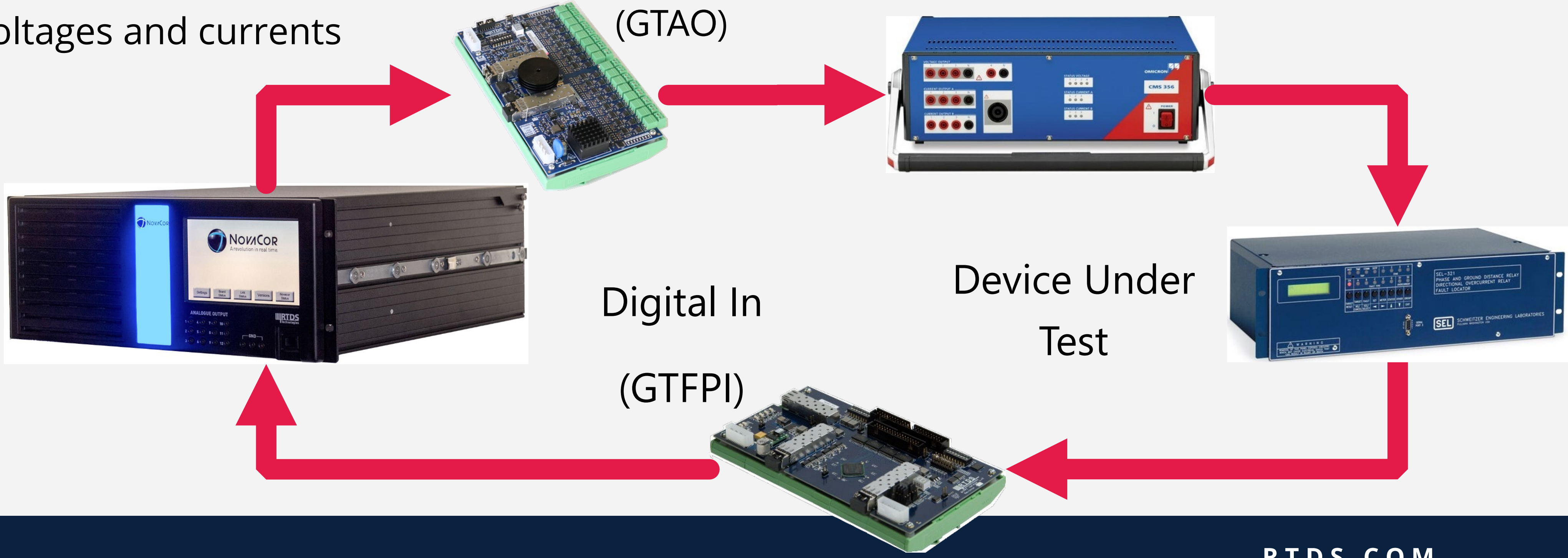
Control Hardware In Loop (CHIL) vs Power Hardware In Loop (PHIL)



Control Hardware In Loop

In CHIL,

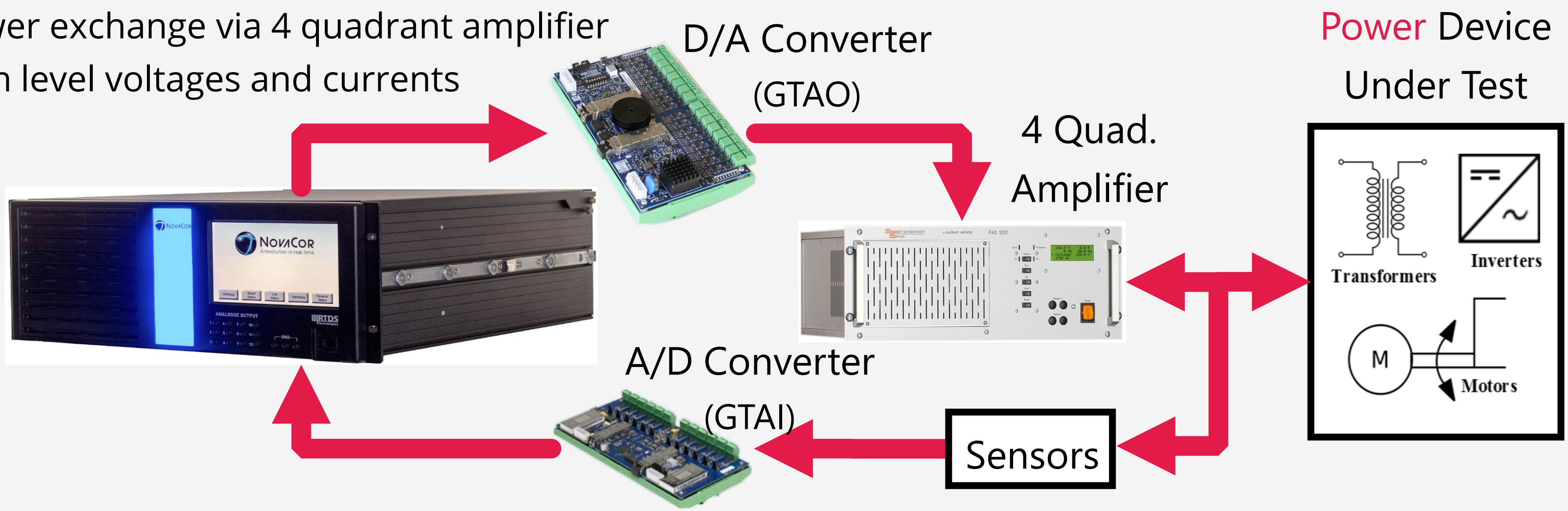
- Entire power system is modeled in RTDS
- No power exchanged over interface
- Low level voltages and currents



Power Hardware In Loop (PHIL)

In PHIL,

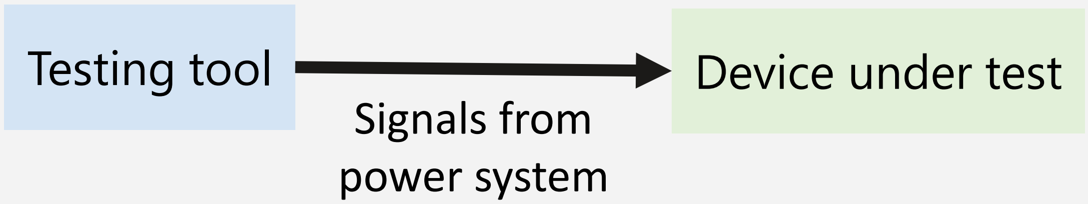
- A portion of the power system is modeled in RTDS
- Power exchange via 4 quadrant amplifier
- High level voltages and currents



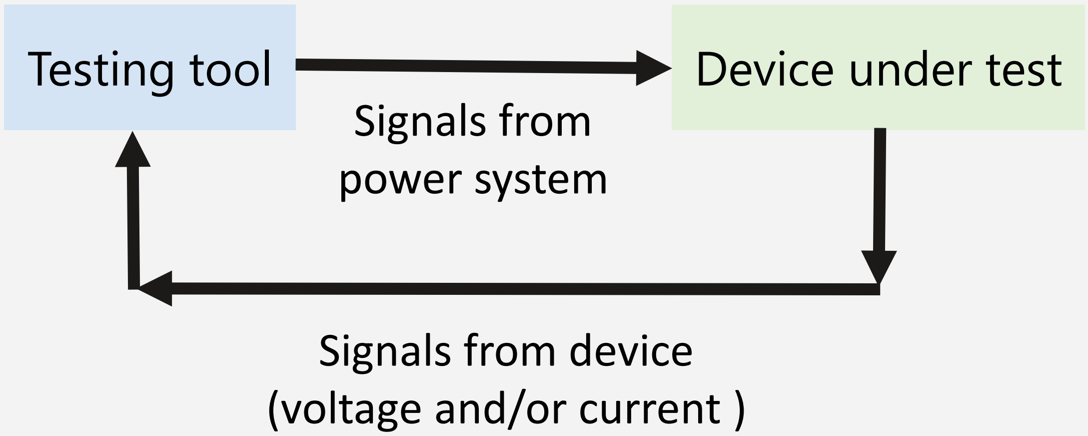
Open Loop vs Closed Loop PHIL

- Some applications might consider open loop as PHIL
- Challenge comes from closing the loop for kW to MW range
- All further discussions are referring to **Closed Loop** PHIL

Open Loop

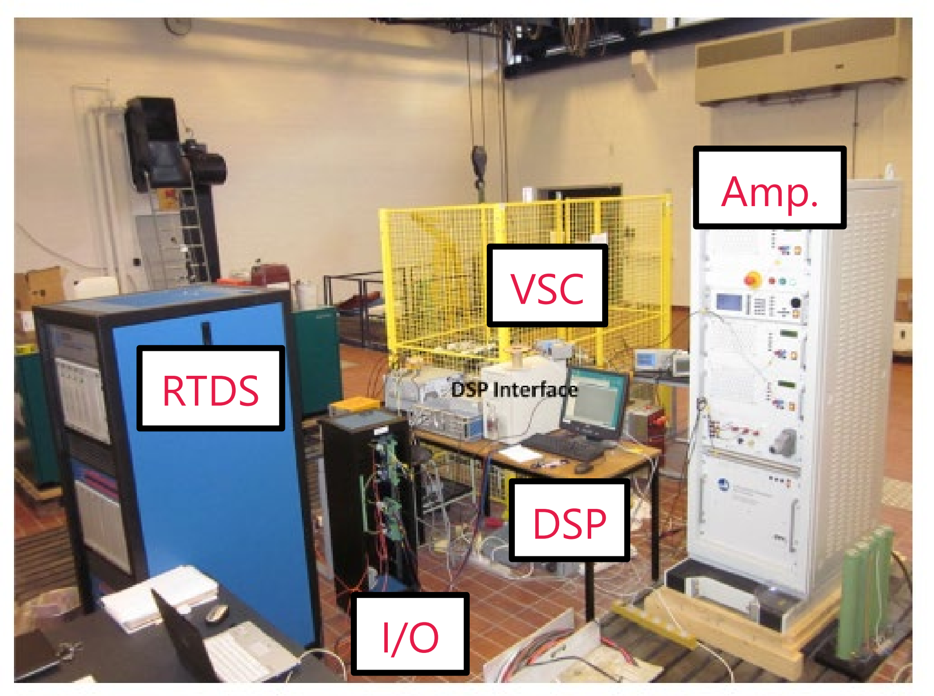


Closed Loop



Motivation behind PHIL

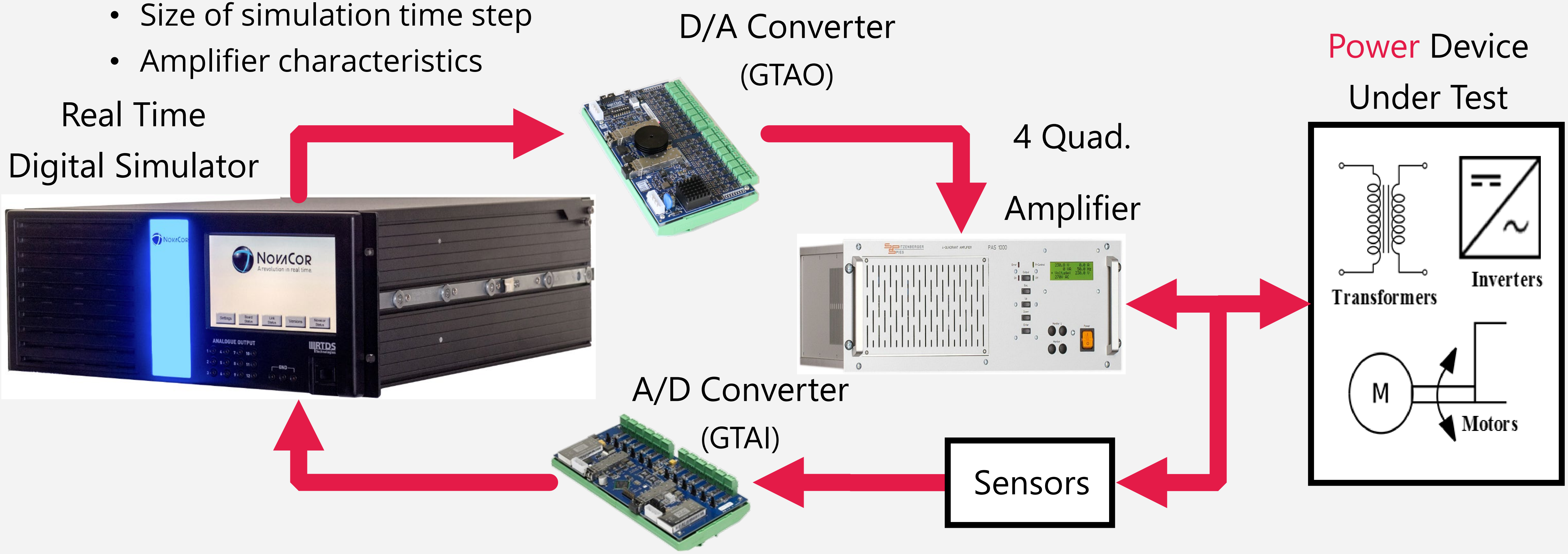
- Power device under test is a “black box”
- Difficult to obtain model for power device under test
- Testing increasingly complex control circuits
- Current PHIL Applications
  - Power converter testing (VSC, MMC etc.)
  - Distributed & Renewable Energy Integration
  - Microgrids
  - Shipboard Machine Drives



Power hardware in the loop validation of fault ride through of VSC HVDC connected offshore wind power plants
SHARMA, Ranjan ; WU, Qiuwei ; CHA, Seung ; JENSEN, Kim ; RASMUSSEN, Tonny ; ØSTEGAARD, Jacob
Journal of Modern Power Systems and Clean Energy, 2014, Vol.2(1), pp.23-29 [Peer Reviewed Journal]Springer Science & Business Media B.V.

Key Factors for PHIL Simulation

- Delays in the PHIL interface affect simulation accuracy and stability
- Size of simulation time step
- Amplifier characteristics



PHIL Report

- PHIL Report documenting our experiences
- Freely Available on our website (https://knowledge.rtds.com/hc/en-us/article_attachments/360049451353/RTDS_PHIL_Report-2-1.pdf)
- Discusses key factors for PHIL simulation
- Interface Algorithms
- 4 Quadrant Amplifiers
- Characterizing PHIL Interface
- Stability and Accuracy of PHIL Interface
- PHIL Applications (e.g. PV Panel & Microinverter)

Digital Interface

- Aurora Communication Protocol
- Reduced loop delay & noise
- Improved stability & accuracy

RTDS

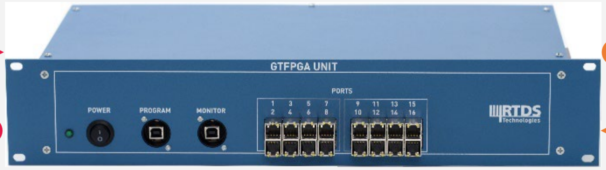
Aurora Interface

SPS APS Amplifier

RTDS

GTFPGA Interface

GTFPGA Unit



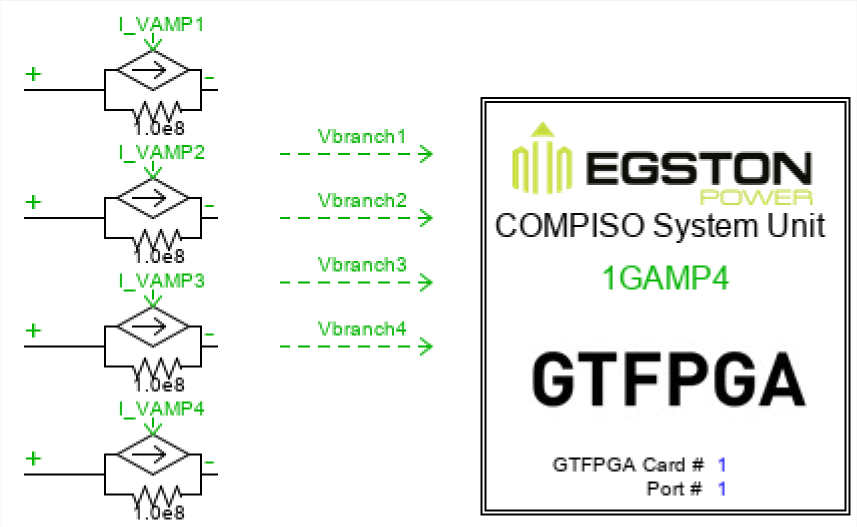
Aurora Interface

EGSTON COMPISO System

PHIL Components

EGSTON GTFPGA Component

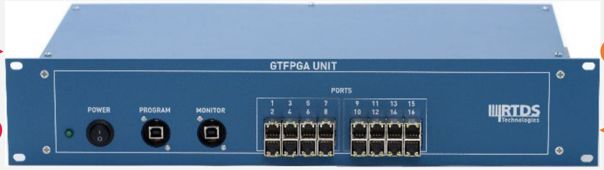
- Digital interface and source embedded into a single component
- Optimized timing for data exchanges to further reduce loop delay
- User controlled feedback switch for open/closed loop operation



RTDS

GTFPGA Interface

GTFPGA Unit



Aurora Interface

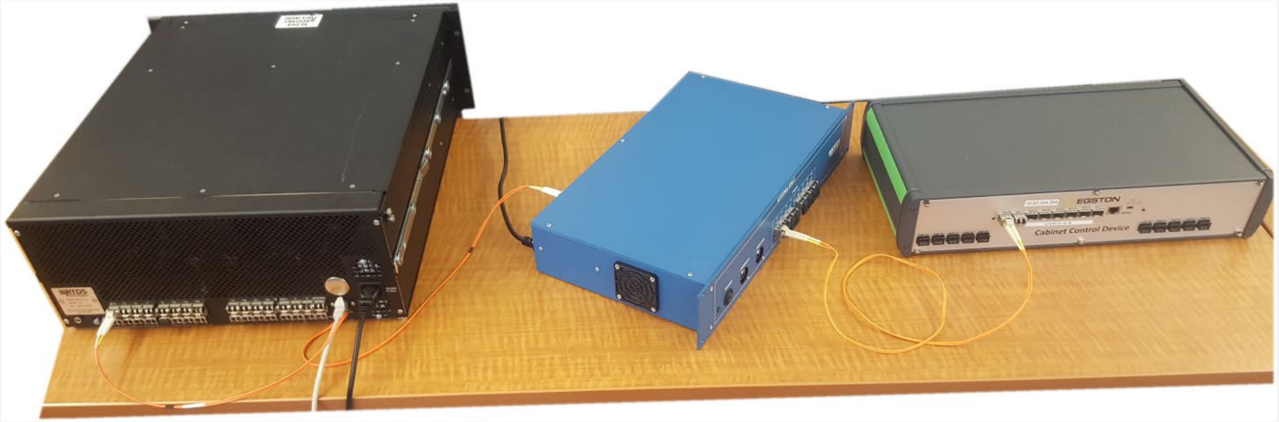
EGSTON COMPISO System

PHIL Components

EGSTON GTFPGA Component Hardware Connections

- Requires a GTFPGA Unit with EGSTON Firmware and either a PB5 or NovaCor based RTDS
- Simplifies wiring and eliminates possibility of user error when wiring

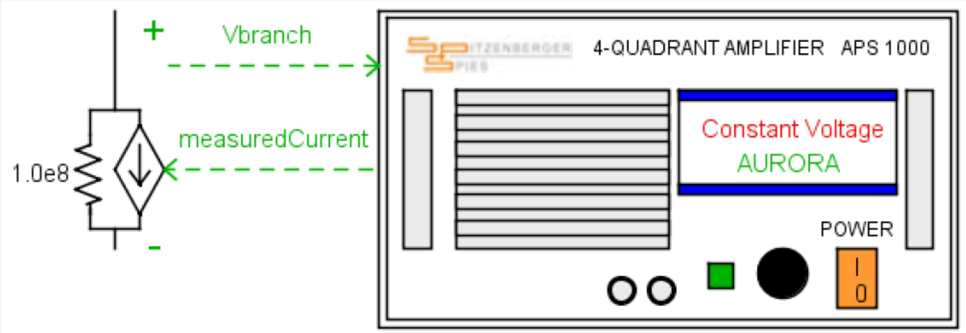
RTDS GTFPGA EGSTON CCD



PHIL Components

SPS Component

- Digital interface and source embedded into a single component
- Optimized timing for data exchanges to further reduce loop delay
- Automatic or user defined scaling factors for over 12 SPS amplifier models
- User controlled feedback switch for open/close loop operation



RTDS

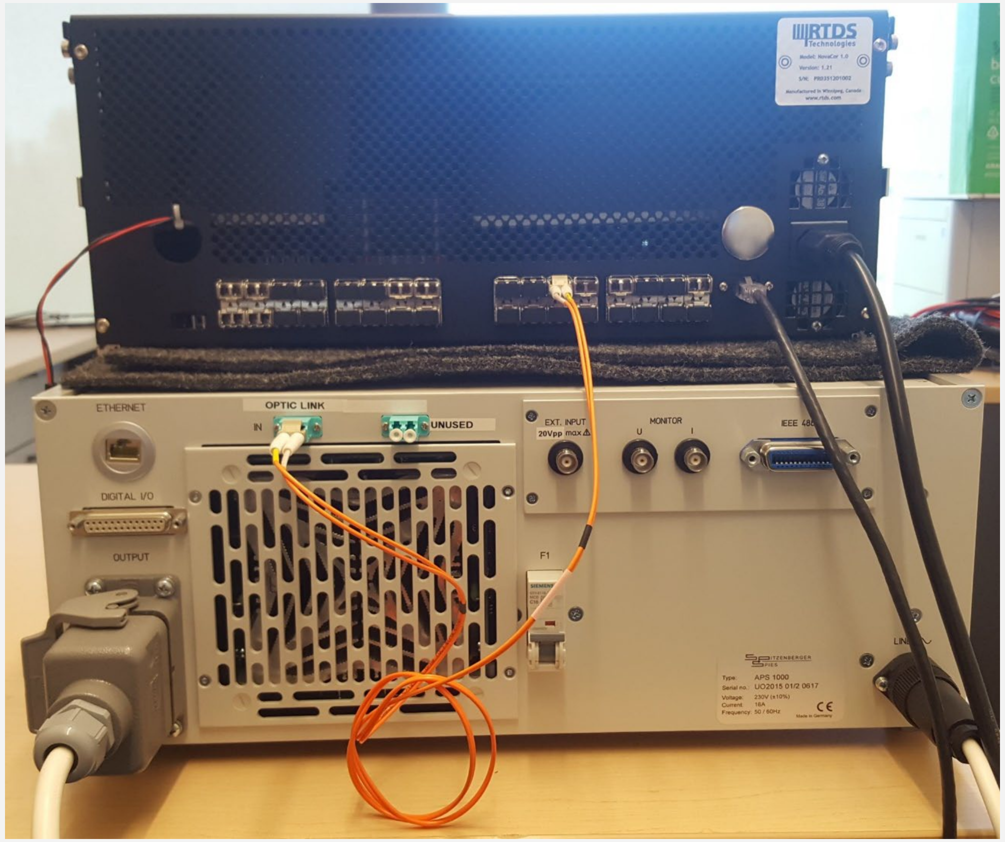
Aurora Interface

SPS APS Amplifier

PHIL Components

SPS Component Hardware Connections

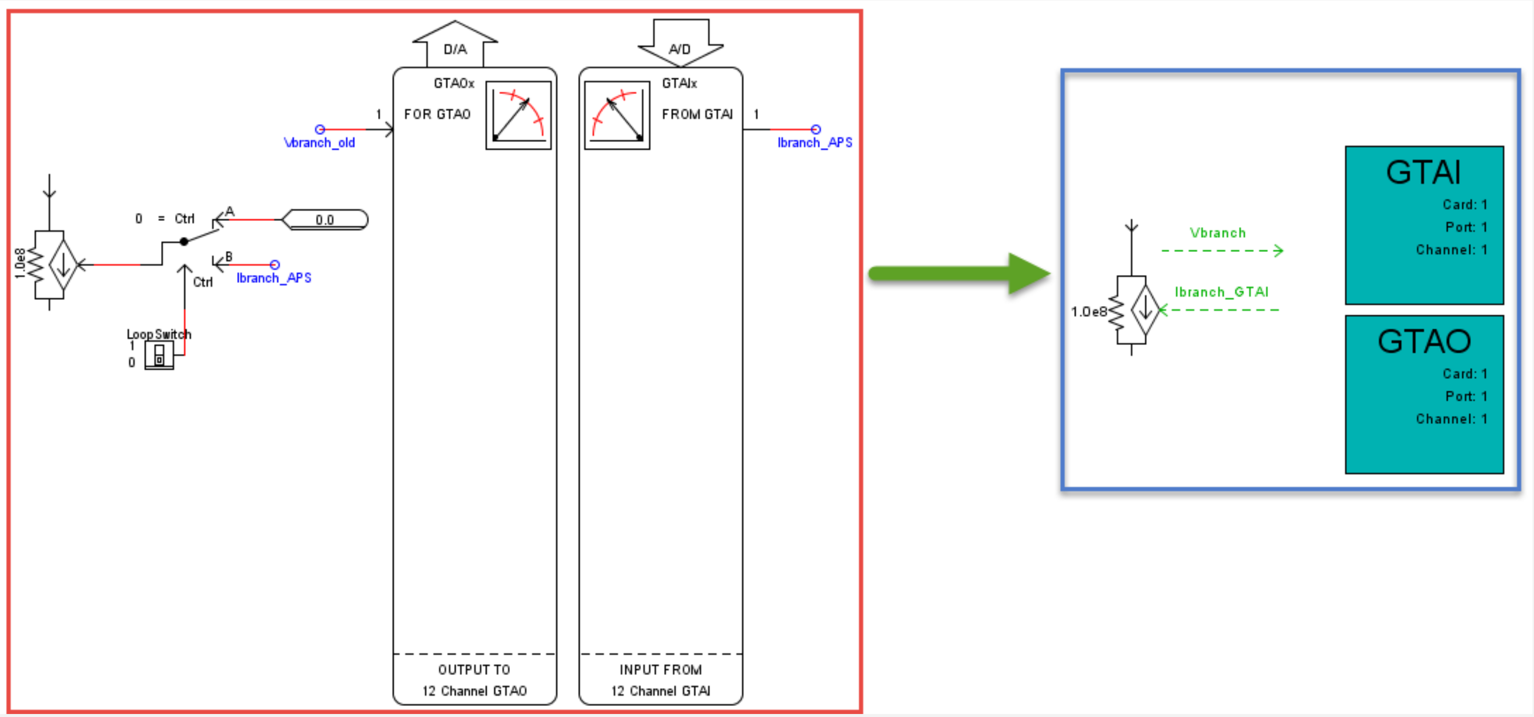
- Requires a licensed Aurora Port on either PB5 or NovaCor based RTDS
- Eliminates use of Analog Output/Input cards in PHIL interface
- Simplifies wiring and eliminates possibility of user error when wiring



PHIL Components

PHIL GTAO/GTAI Component

- Combines GTAO, GTAI and Current Source into a single Power System Component
- Eliminates unnecessary delays when transferring signals between GTAO/GTAI and the current source

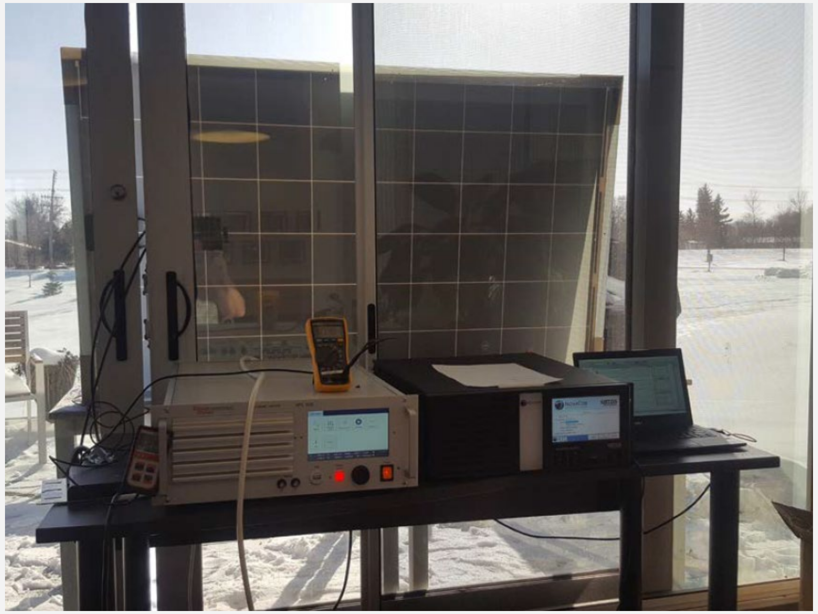


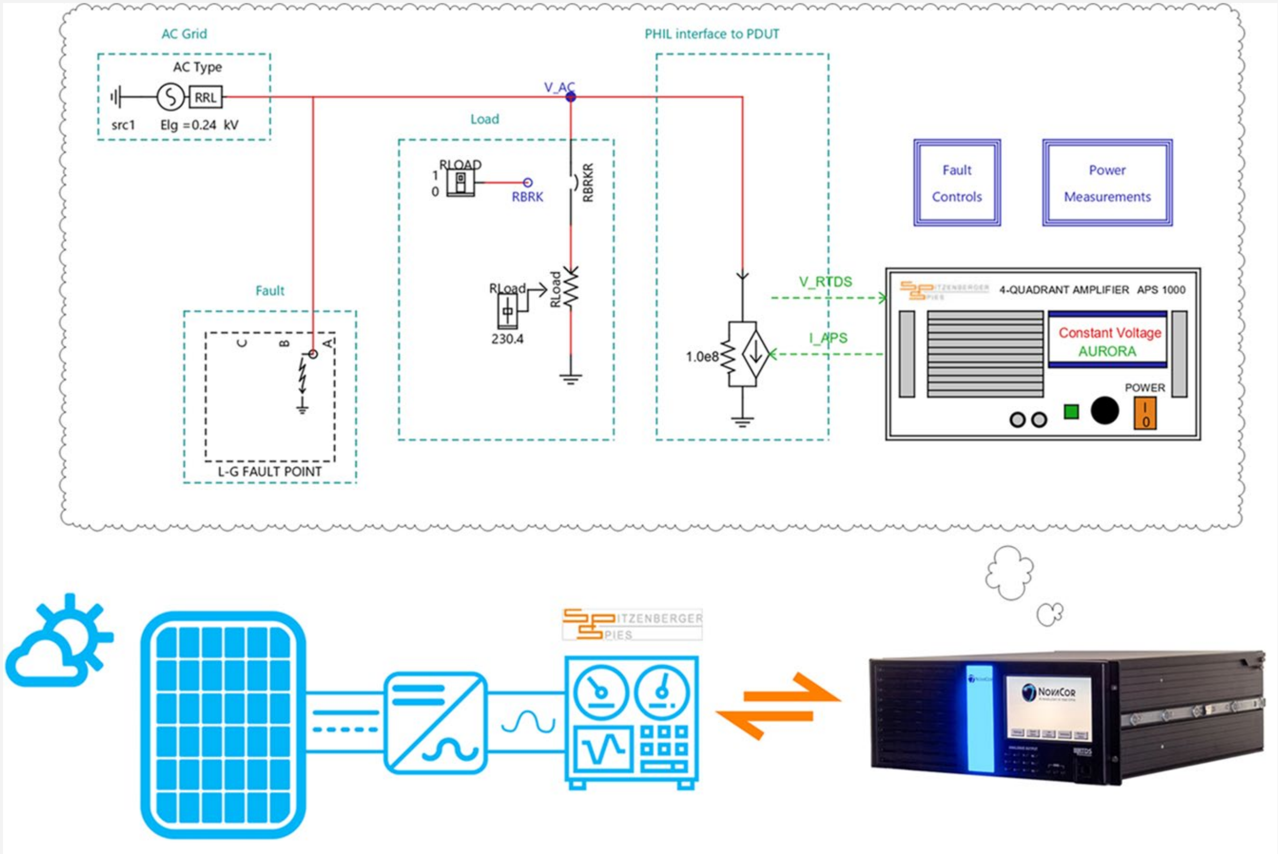
Demonstration: PHIL with a PV Panel & Micro Inverter

Demonstration

PHIL with a PV Panel & Micro Inverter

- 255W PV Panel
- 225W Micro Inverter





Thank you!

RTDS Technologies

RTDS.COM