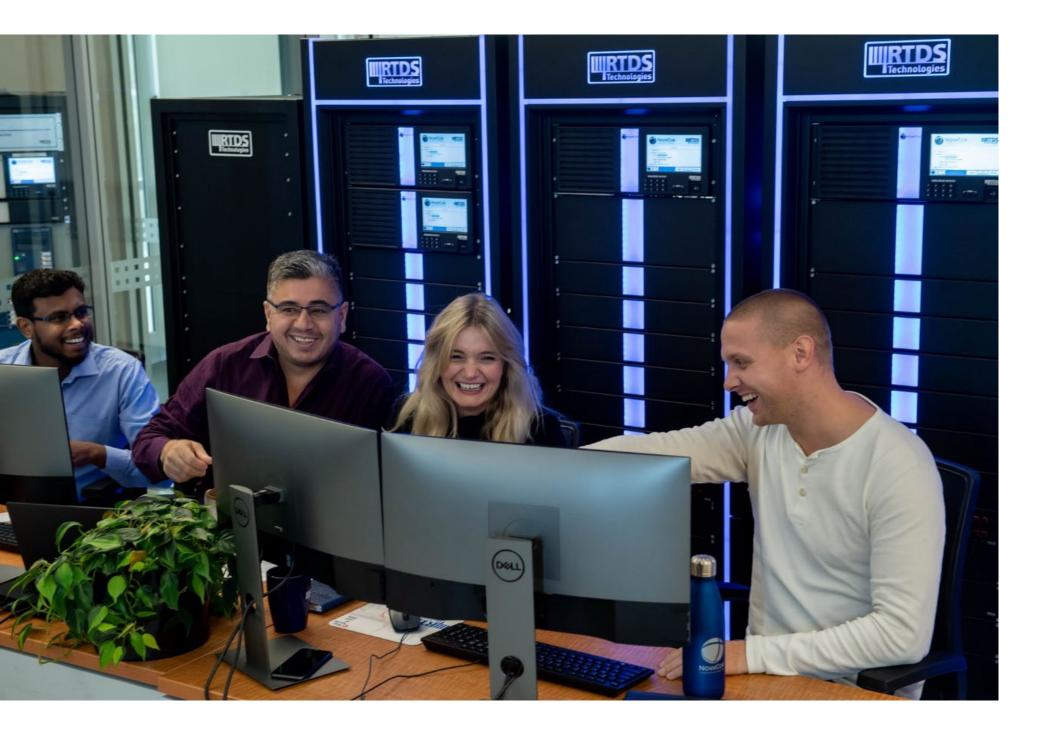


WEBINAR AND DEMO: **Modelling Protection & Control for** IEEE 1547[™]-Compliant **DER Interconnection**

IIIRTDS Technologies

About RTDS Technologies



- Pioneered real-time power system simulation in the 1980s
- The RTDS Simulator is the industry standard
 - testing, used by utilities, manufacturers,

 - research and educational institutions, and consultants worldwide
- Learn more at <u>www.rtds.com</u> or the large library of videos on the RTDS Technologies YouTube channel

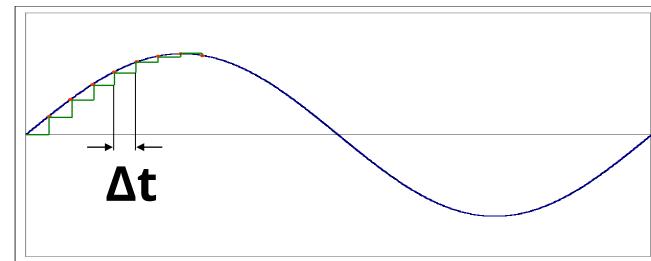


• Headquarters in Winnipeg, Canada

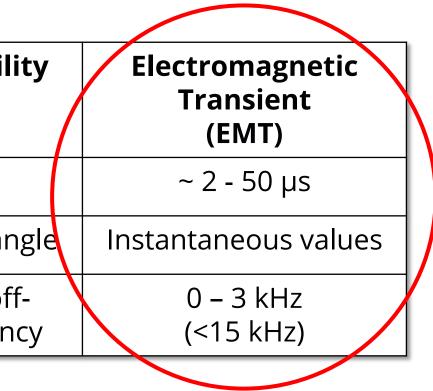
for real-time simulation and closed-loop

EMT SIMULATION

Type of Simulation	Load Flow	Transient Stabili Analysis (TSA)
Typical timestep	Single solution	~ 8 ms
Output	Magnitude and angle	Magnitude and an
Frequency range	Nominal frequency	Nominal and of nominal frequen



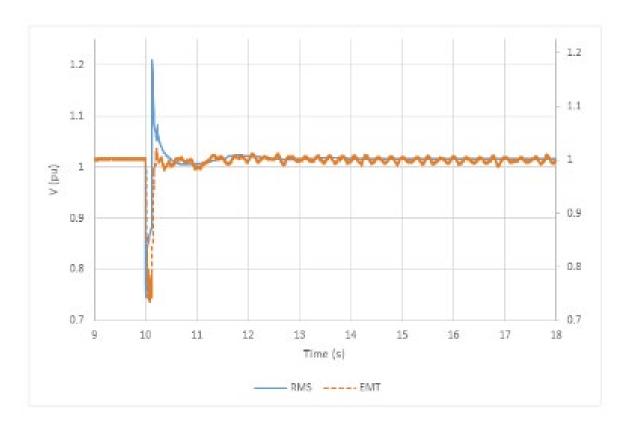


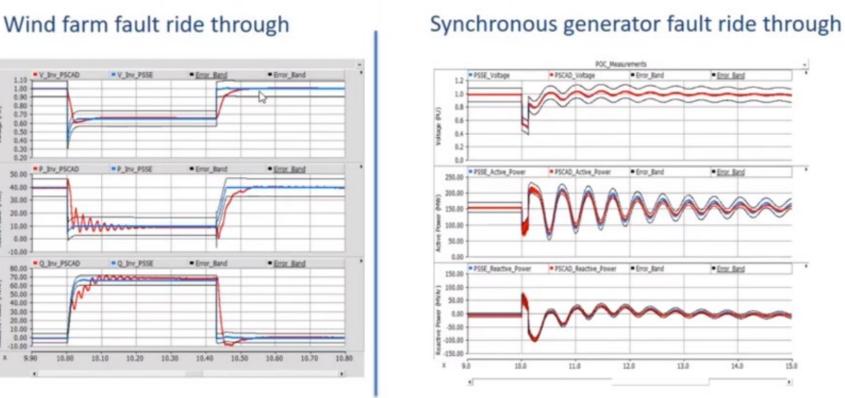


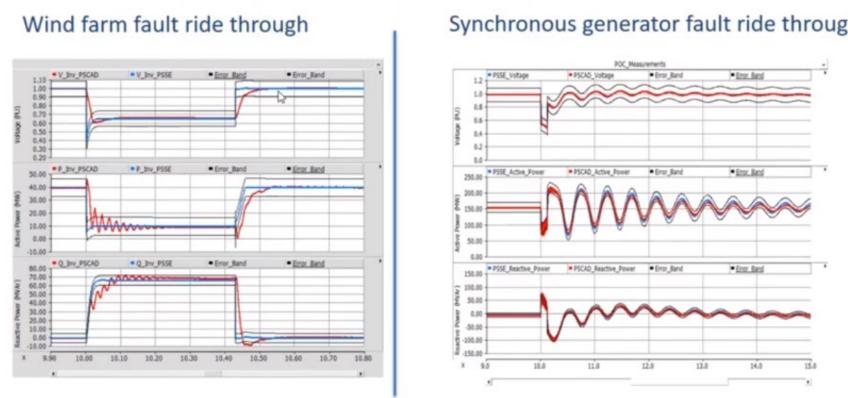
Dommel algorithm of nodal analysis used in RTDS, PSCAD, EMTP, etc.

ADVANTAGES OF EMT SIMULATION

- Allows for a greater depth of analysis than phasor domain (RMS) representations •
- RMS models lack the ability to capture fast network dynamics during transient conditions and may provide • optimistic results
- Important for modern systems with many power electronic converters (more likely to predict control • instability)



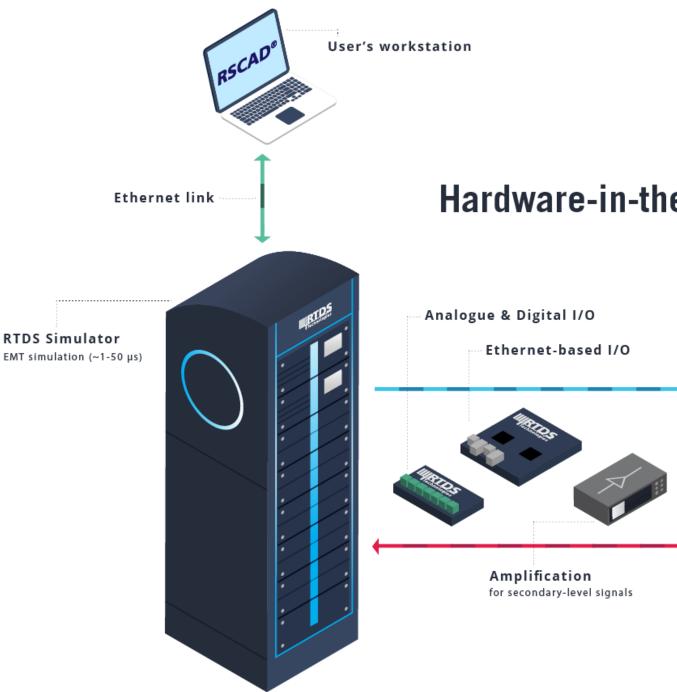






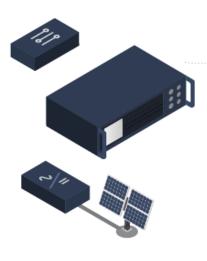
WHAT IS REAL TIME?

- **Real time operation** is what ● allows us to connect physical devices in a closed loop with the simulated environment (hardware-in-the-loop)
- True closed-loop testing is only ● possible with a real time simulator





Hardware-in-the-loop interface



Device(s) under test

Protective relays Automation controllers PMUs and PDCs Power electronic controls Power hardware SCADA and visualization tools

DER MODELLING AND TESTING APPLICATIONS

- DER integration studies
 - Black box control model integration
- Impacts/interactions of DERs with existing automation
- Grid-forming control testing
- Inverter testing
- PPC testing
- Replica testing



Quanta Technology's testbed for studying impacts of DER on protection for a utility customer



GTSOC – BLACK BOX CONTROL INTEGRATION

- Features a powerful FPGA board with multi-processor system-on-a-chip technology to facilitate the integration of black box control models into the real-time simulation
- Vendor can provide DER control model to customer while protecting IP
- Similar to .dll files (PSCAD), but uses .a files to achieve deterministic real-time operation



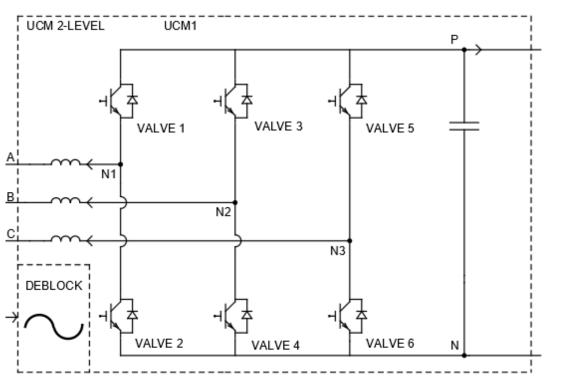


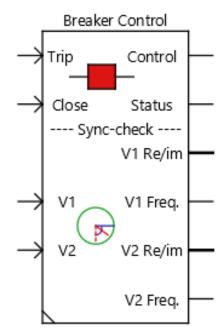


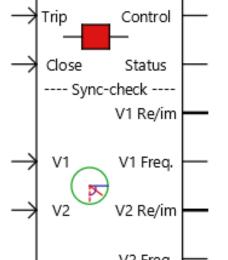
FEATURES OF TODAY'S CASE

- New Sample Case available in RSCAD FX 1.2 and up •
- Compiles on one core of NovaCor •
- Protection & control modelled in RSCAD I/O could be ۲ added for external P&C testing
- 2-level Universal Converter Model with Modulation • Waveform input – Mainstep environment









UNIVERSAL CONVERTER MODEL

- Model VSCs in both the Substep (1-10 us) and Mainstep (typically 25-50 us) environments •
- Simulation environment (i.e. timestep) and model input determine **performance** and processing load of converter model
- Modulation Wave Input: no detailed switching (average value model) ullet
- Improved Firing Input: ullet
 - Substep (1-10 us): Accurately represents switching frequencies up to ~150 kHz
 - Mainstep (25-50 us): Accurately represents switching frequencies up to **10 kHz**

Note: Both Mainstep options require 10 load units per converter. Using Improved Firing does not increase the processing load.







Thank you! kati@rtds.com



WEBINAR

MODELLING PROTECTION AND CONTROL FOR IEEE 1547[™]–COMPLIANT DER INTERCONNECTION



OUTLINE

- Introduction.
- Protection and Control Modelling.
- Demonstration.
- Questions and Answers.





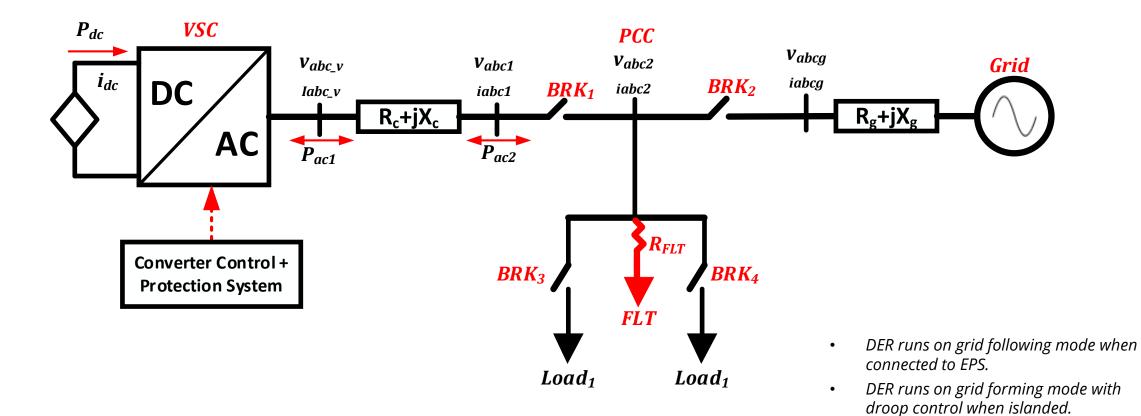
INTRODUCTION

• IEEE Std 1547[™]-2018 -

- IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources (DER) with Associated Electric Power Systems Interfaces.
- Addresses consensus standard technical requirements for DER interconnection by providing uniform criteria and requirements relevant to the performance, operation, and testing of the interconnection.
- Key criteria
 - Synchronization of the DER to an Area Electric Power System (EPS).
 - Response to the Area EPS abnormal conditions
 - > Undervoltage (UV), Overvoltage (OV), and Voltage Disturbance Ride-Through.
 - Underfrequency (UF), Overfrequency (OF), and Frequency Disturbance Ride-Through.

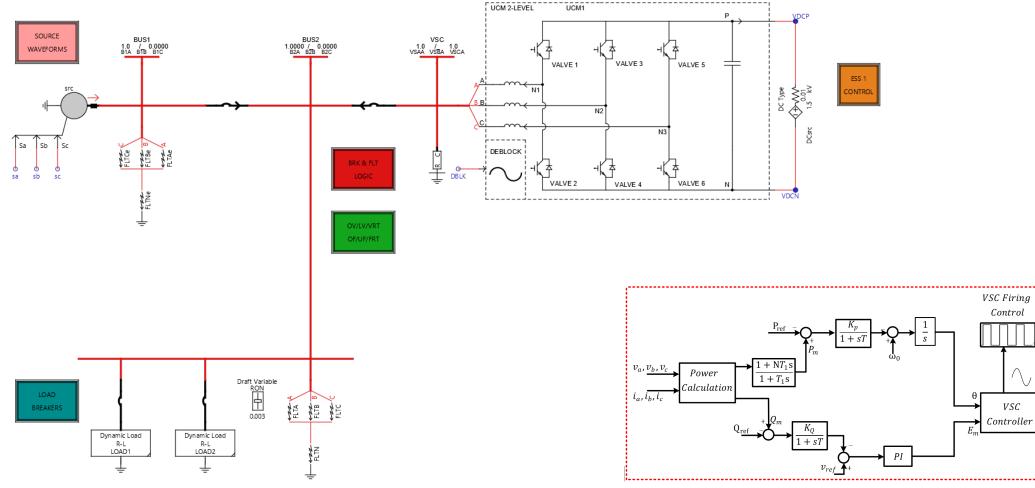


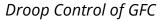
POWER SYSTEM NETWORK





SIMULATION MODELING

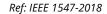






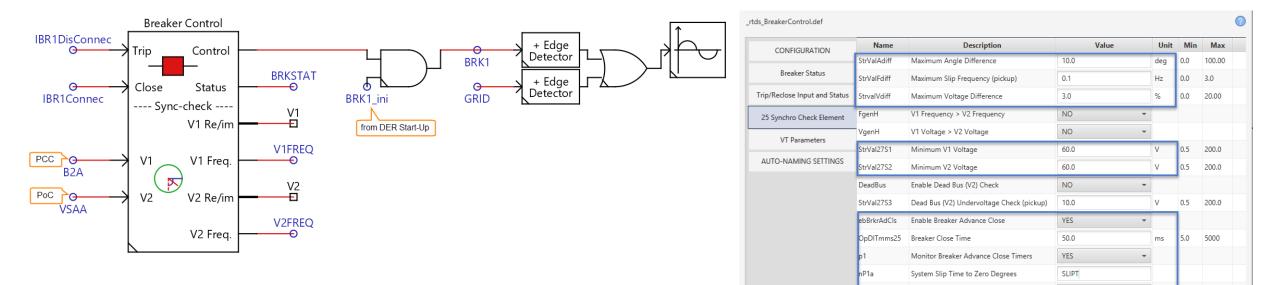
SYNCHRONIZATION OF DER TO GRID

Rating of DER	Frequency Difference	Voltage Difference	Phase Angle Difference
Units (kVA)	(Δf, Hz)	(ΔV, %)	(Δφ, °)
> 1500	0.1	3	



nP1b

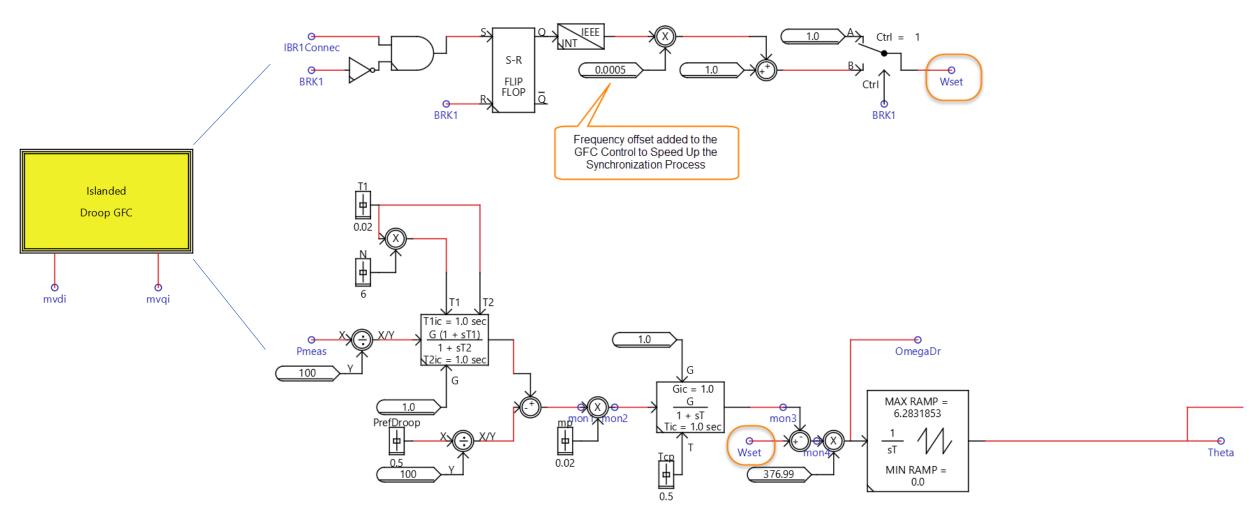
Breaker Close Time





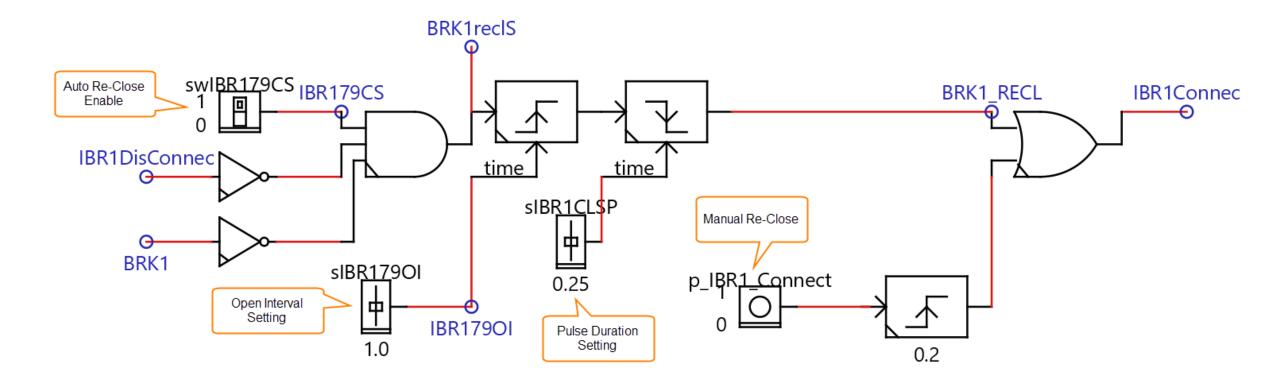
CLST

SYNCHRONIZATION OF DER TO GRID





RECLOSING LOGIC



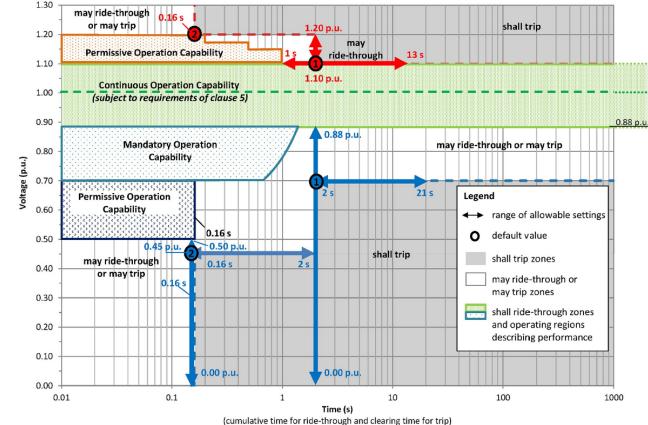


VOLTAGE DISTURBANCES – TRIP/LVRT/OVRT

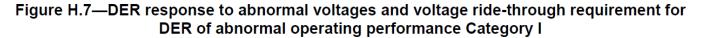
Voltage range (p.u.)	Operating mode/response	Minimum ride-through time (s) (design criteria)	Maximum response time (s) (design criteria)
V > 1.20	Cease to Energize ^a	N/A	0.16
$1.175 < V \le 1.20$	Permissive Operation	0.2	N/A
$1.15 < V \le 1.175$	Permissive Operation	0.5	N/A
$1.10 < V \le 1.15$	Permissive Operation	1	N/A
$0.88 \le V \le 1.10$	Continuous Operation	Infinite	N/A
$0.70 \le V \le 0.88$	Mandatory Operation	Linear slope of 4 s/1 p.u. voltage starting at 0.7 s @ 0.7 p.u.:	N/A
		$T_{\rm VRT} = 0.7 \text{ s} + \frac{4 \text{ s}}{1 \text{ p.u.}} (V - 0.7 \text{ p.u.})$	
$0.50 \le V \le 0.70$	Permissive Operation	0.16	N/A
V < 0.50	Cease to Energize ^a	N/A	0.16

Table 14—Voltage ride-through requirements for DER for abnormal operating performance

Category I (see Figure H.7)



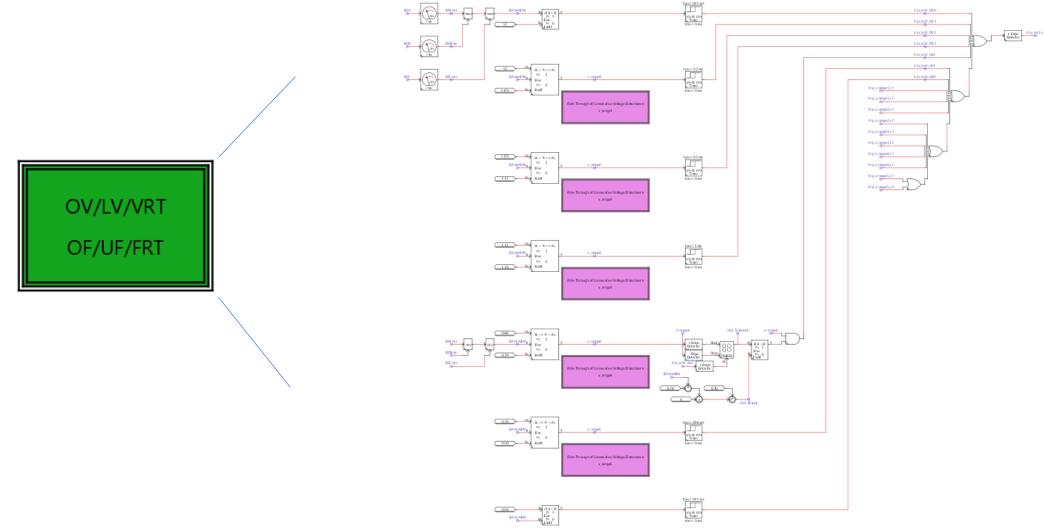
Category I



Ref: IEEE 1547-2018



VOLTAGE DISTURBANCES – MODELING





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RIDE-THROUGH OF CONSECUTIVE VOLTAGE DISTURBANCE

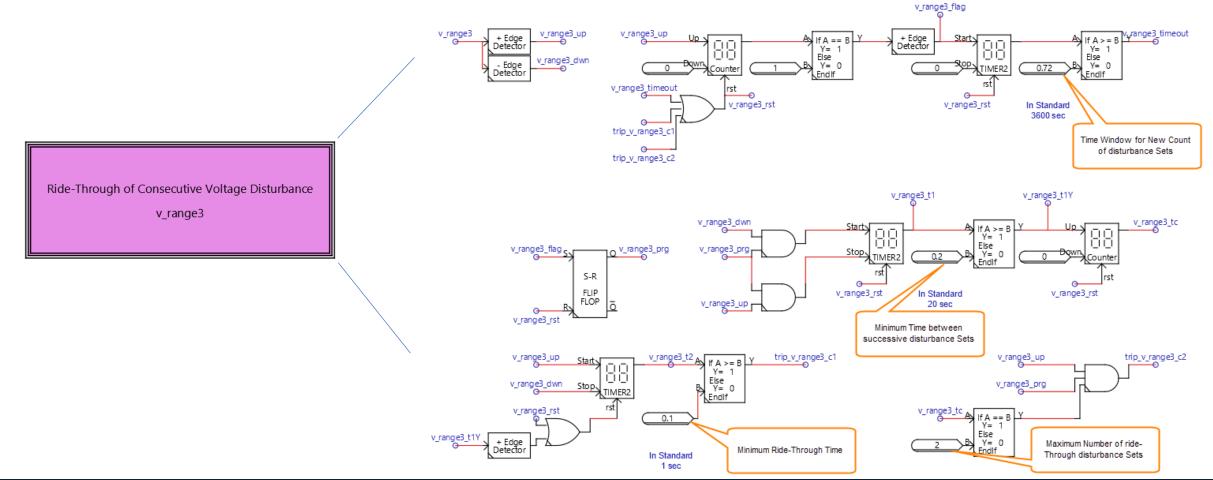
Table 17 —Voltage ride-through requirements for consecutive temporary voltage disturbances caused by unsuccessful reclosing for DER of abnormal operating performance Category I, Category II, and Category III

Col. 1	Col. 2	Col. 3	Col. 4
Category	Maximum number of ride- through disturbance sets	Minimum time between successive disturbance sets (s)	Time window for new count of disturbance sets (min)
Ι	2	20.0	60
II	2	10.0	60
III	3	5.0	20

Ref: IEEE 1547-2018



RIDE-THROUGH OF CONSECUTIVE VOLTAGE DISTURBANCE - MODELING





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FREQUENCY DISTURBANCES – TRIP/LFRT/OFRT



Frequency range (Hz)	Operating mode	Minimum time (s) (design criteria)
f > 62.0	No ride-through requirements apply to this range	
$61.2 < f \le 61.8$	Mandatory Operation ^a	299
$58.8 \le f \le 61.2$	Continuous Operation ^{a,b}	Infinite ^c
57.0 ≤ <i>f</i> < 58.8	Mandatory Operation ^b	299
f< 57.0	No ride-through requirements apply to this range	

Table 21—Rate of change of frequency (ROCOF) ride-through requirements for DER of abnormal operating performance Category I, Category II, and Category III

Category I	Category II	Category III
0.5 Hz/s	2.0 Hz/s	3.0 Hz/s

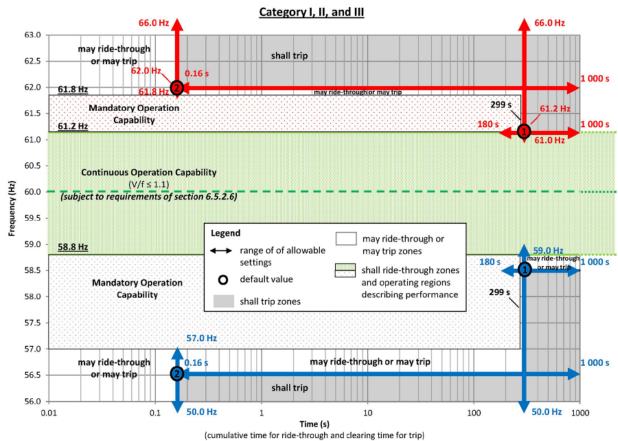
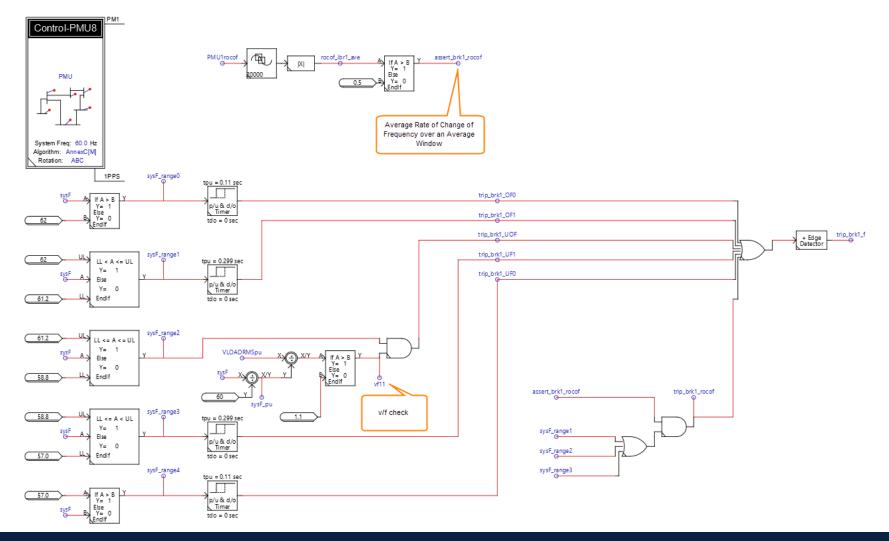


Figure H.10—DER default response to abnormal frequencies and frequency ride-through requirements for DER of abnormal operating performance Category I, Category II, and Category III

Ref: IEEE 1547-2018



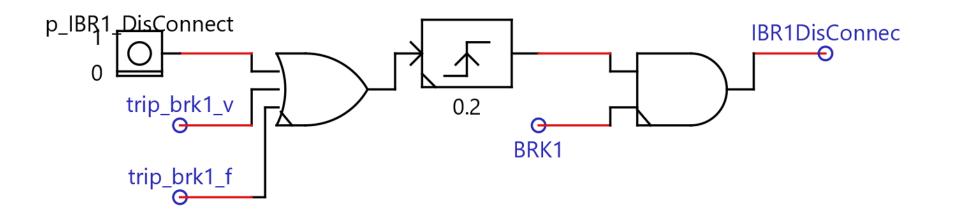
FREQUENCY DISTURBANCES – MODELING





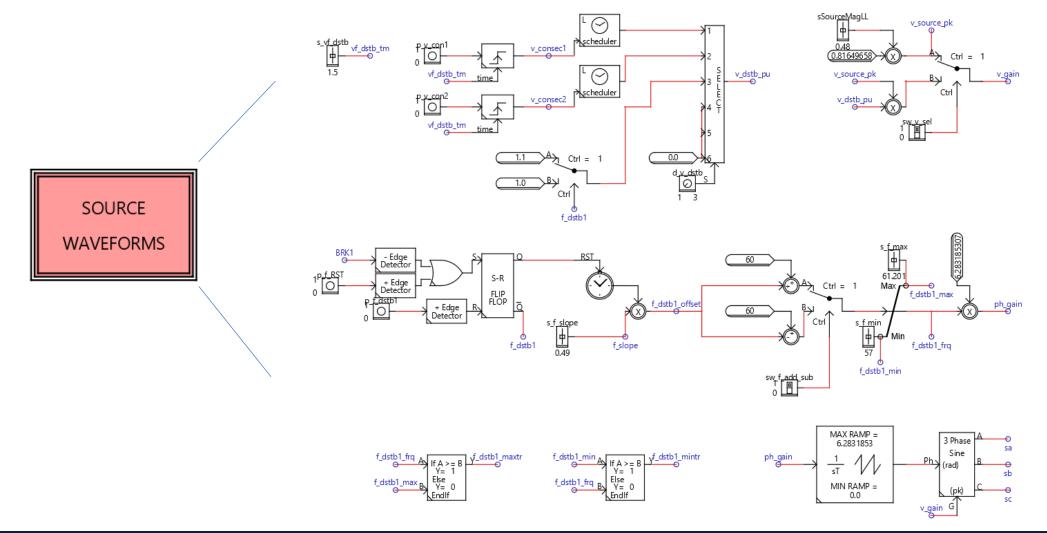
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TRIP LOGIC





CONTROLLABLE SOURCE WAVEFORM





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RUNTIME DEMO





